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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	8064
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	115
Number of Gates	500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax500-pq208i

1 – General Description

Axcelerator devices offer high performance at densities of up to two million equivalent system gates. Based upon the Microsemi AX architecture, Axcelerator has several system-level features such as embedded SRAM (with complete FIFO control logic), PLLs, segmentable clocks, chip-wide highway routing, and carry logic.

Device Architecture

AX architecture, derived from the highly-successful SX-A sea-of-modules architecture, has been designed for high performance and total logic module utilization (Figure 1-1). Unlike in traditional FPGAs, the entire floor of the Axcelerator device is covered with a grid of logic modules, with virtually no chip area lost to interconnect elements or routing.

Programmable Interconnect Element

The Axcelerator family uses a patented metal-to-metal antifuse programmable interconnect element that resides between the upper two layers of metal (Figure 1-2 on page 1-2). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on traditional FPGAs) and enables the efficient sea-of-modules architecture. The antifuses are normally open circuit and, when programmed, form a permanent, passive, low-impedance connection, leading to the fastest signal propagation in the industry. In addition, the extremely small size of these interconnect elements gives the Axcelerator family abundant routing resources.

The very nature of Microsemi's nonvolatile antifuse technology provides excellent protection against design pirating and cloning (FuseLock technology). Typical cloning attempts are impossible (even if the security fuse is left unprogrammed) as no bitstream or programming file is ever downloaded or stored in the device. Reverse engineering is virtually impossible due to the difficulty of trying to distinguish between programmed and unprogrammed antifuses and also due to the programming methodology of antifuse devices (see "Security" on page 2-108).

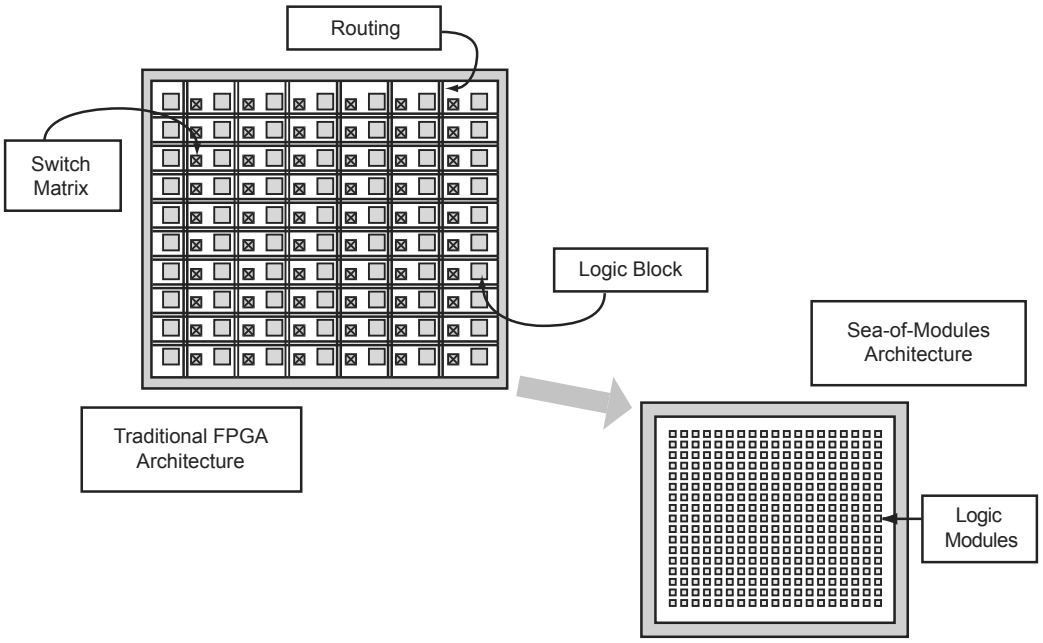

Figure 1-1 • **Sea-of-Modules Comparison**

Design Environment

The Axcelerator family of FPGAs is fully supported by both Microsemi's Libero® Integrated Design Environment and Designer FPGA Development software. Libero IDE is an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment (see the *Libero IDE Flow* diagram located on the Microsemi SoC Products Group website). Libero IDE includes Synplify® Actel Edition (AE) from Synplicity®, ViewDraw® AE from Mentor Graphics®, ModelSim® HDL Simulator from Mentor Graphics, WaveFormer Lite™ AE from SynaptiCAD®, and Designer software from Microsemi.

Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes the following:

- Timer – a world-class integrated static timing analyzer and constraints editor which support timing-driven place-and-route
- NetlistViewer – a design netlist schematic viewer
- ChipPlanner – a graphical floorplanner viewer and editor
- SmartPower – allows the designer to quickly estimate the power consumption of a design
- PinEditor – a graphical application for editing pin assignments and I/O attributes
- I/O Attribute Editor – displays all assigned and unassigned I/O macros and their attributes in a spreadsheet format

With the Designer software, a user can lock the design pins before layout while minimally impacting the results of place-and-route. Additionally, Microsemi's back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Microsemi's integrated verification and logic analysis tool. Another tool included in the Designer software is the SmartGen core generator, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Designer software is compatible with the most popular FPGA design entry and verification tools from EDA vendors, such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

Programming

Programming support is provided through Silicon Sculptor II, a single-site programmer driven via a PC-based GUI. In addition, BP Microsystems offers multi-site programmers that provide qualified support for Microsemi devices. Factory programming is available for high-volume production needs.

In-System Diagnostic and Debug Capabilities

The Axcelerator family of FPGAs includes internal probe circuitry, allowing the designer to dynamically observe and analyze any signal inside the FPGA without disturbing normal device operation (Figure 1-9).

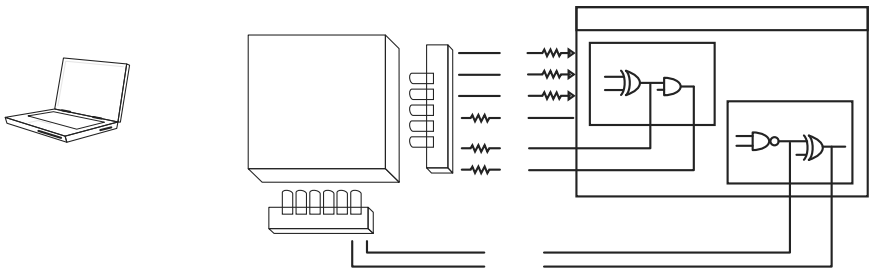

Figure 1-9 • **Probe Setup**

Up to four individual signals can be brought out to dedicated probe pins (PRA/B/C/D) on the device. The probe circuitry is accessed and controlled via Silicon Explorer II, Microsemi's integrated verification and logic analysis tool that attaches to the serial port of a PC and communicates with the FPGA via the JTAG port (See "Silicon Explorer II Probe Interface" on page 2-109).

Summary

Microsemi's Axcelerator family of FPGAs extends the successful SX-A architecture, adding embedded RAM/FIFOs, PLLs, and high-speed I/Os. With the support of a suite of robust software tools, design engineers can incorporate high gate counts and fixed pins into an Axcelerator design yet still achieve high performance and efficient device utilization.

Related Documents

Application Notes

Simultaneous Switching Noise and Signal Integrity
http://www.microsemi.com/soc/documents/SSN_AN.pdf
Axcelerator Family PLL and Clock Management
http://www.microsemi.com/soc/documents/AX_PLL_AN.pdf
Implementation of Security in Actel Antifuse FPGAs
http://www.microsemi.com/soc/documents/Antifuse_Security_AN.pdf

User's Guides and Manuals

Antifuse Macro Library Guide
http://www.microsemi.com/soc/documents/libguide_UG.pdf
SmartGen, FlashROM, Analog System Builder, and Flash Memory System Builder
http://www.microsemi.com/soc/documents/genguide_ug.pdf
Silicon Sculptor II User's Guide
http://www.microsemi.com/soc/documents/silisculptII_sculpt3_ug.pdf

White Paper

Design Security in Nonvolatile Flash and Antifuse FPGAs
http://www.microsemi.com/soc/documents/DesignSecurity_WP.pdf
Understanding Actel Antifuse Device Security
http://www.microsemi.com/soc/documents/DesignSecurity_WP.pdf

Miscellaneous

Libero IDE flow diagram
http://www.microsemi.com/soc/products/tools/libero/flow.html

Thermal Characteristics

Introduction

The temperature variable in Microsemi's Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction temperature to be higher than the ambient temperature. EQ 1 can be used to calculate junction temperature.

T_J = Junction Temperature = $\Delta T + T_a$

EQ 1

Where:

T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient

$\Delta T = \theta_{ja} * P$

EQ 2

Where:

P = Power

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located under Table 2-6 on page 2-7.

Package Thermal Characteristics

The device junction-to-case thermal characteristic is θ_{jc}, and the junction-to-ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates. θ_{jc} values are provided for reference. The absolute maximum junction temperature is 125°C.

The maximum power dissipation allowed for commercial- and industrial-grade devices is a function of θ_{ja}. A sample calculation of the absolute maximum power dissipation allowed for an 896-pin FBGA package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. } (°C) - \text{Max. ambient temp. } (°C)}{\theta_{ja}(°C/W)} = \frac{125°C - 70°C}{13.6°C/W} = 4.04\ W$$

5 V Tolerance

There are two schemes to achieve 5 V tolerance:

1. 3.3 V PCI and 3.3 V PCI-X are the only I/O standards that directly allow 5 V tolerance. To implement this, an internal clamp diode between the input pad and the VCCI pad is enabled so that the voltage at the input pin is clamped, as shown in EQ 3:

Vinput = VCCI + Vdiode = 3.3 V + 0.7 V = 4.0 V

EQ 3

The internal VCCI clamp diode is only enabled while the device is powered on, so the voltage at the input will not be clamped if the VCCI or VCCA are powered off. An external series resistor (~100 Ω) is required between the input pin and the 5 V signal source to limit the current to less than 20 mA (Figure 2-3). The 100 Ω resistor was chosen to meet the input Tr/Tf requirement (Table 2-19 on page 2-21). The GND clamp diode is available for all I/O standards and always enabled.

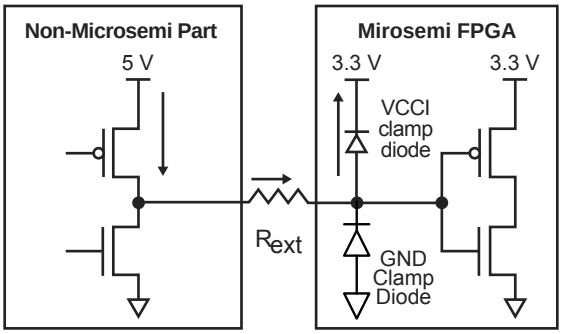

Figure 2-3 • **Use of an External Resistor for 5 V Tolerance**

2. 5 V tolerance can also be achieved with 3.3 V I/O standards (3.3 V PCI, 3.3 V PCI-X, and LVTTL) using a bus-switch product (e.g. IDTQS32X2384). This will convert the 5 V signal to a 3.3 V signal with minimum delay (Figure 2-4).

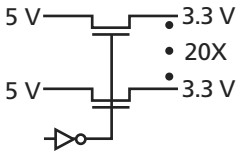

Figure 2-4 • **Bus Switch IDTQS32X2384**

Simultaneous Switching Outputs (SSO)

When multiple output drivers switch simultaneously, they induce a voltage drop in the chip/package power distribution. This simultaneous switching momentarily raises the ground voltage within the device relative to the system ground. This apparent shift in the ground potential to a non-zero value is known as simultaneous switching noise (SSN) or more commonly, ground bounce.

SSN becomes more of an issue in high pin count packages and when using high performance devices such as the Axcelerator family. Based upon testing, Microsemi recommends that users not exceed eight simultaneous switching outputs (SSO) per each VCCI/GND pair. To ease this potential burden on designers, Microsemi has designed all of the Axcelerator BGAs[3] to not exceed this limit with the exception of the CS180, which has an I/O to VCCI/GND pair ratio of nine to one.

Please refer to the *Simultaneous Switching Noise and Signal Integrity* application note for more information.

3. The user should note that in Bank 8 of both AX1000-FG484 and AX500-FG484, there are local violations of this 8:1 ratio.

1.8 V LVCMOS

Low-Voltage Complementary Metal-Oxide Semiconductor for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 3.3 V tolerant CMOS input buffer and a push-pull output buffer.

***Table 2-26* • DC Input and Output Levels**

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**
–0.3	0.2 VCCI	0.7 VCCI	3.6	0.2	VCCI – 0.2	8 mA	–8 mA

AC Loadings

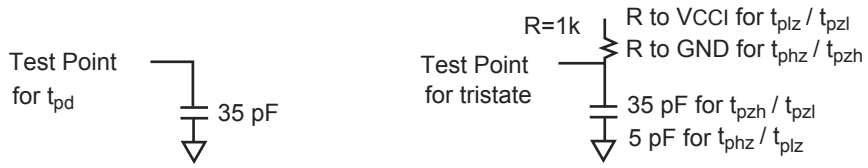

***Figure 2-17* • AC Test Loads**

***Table 2-27* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C_{load} (pF)
0	1.8	0.5 VCCI	N/A	35

*Note: * Measuring Point = VTRIP*

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses an LVTTL input buffer and a push-pull output buffer. The input and output buffers are 5 V tolerant with the aid of external components. Axcelerator 3.3 V PCI and 3.3 V PCI-X buffers are compliant with the PCI Local Bus Specification Rev. 2.1.

The PCI Compliance Specification requires the clamp diodes to be able to withstand for 11 ns, –3.5 V in undershoot, and 7.1 V in overshoot.

***Table 2-33* • DC Input and Output Levels**

	VIL		VIH		VOL	VOH	IOL	IOH
	Min., V	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**
PCI	–0.3	0.3 VCCI	0.5 VCCI	VCCI + 0.5	(per PCI specification)			
PCI-X	–0.5	0.35 VCCI	0.5 VCCI	VCCI + 0.5	(per PCI specification)			

AC Loadings

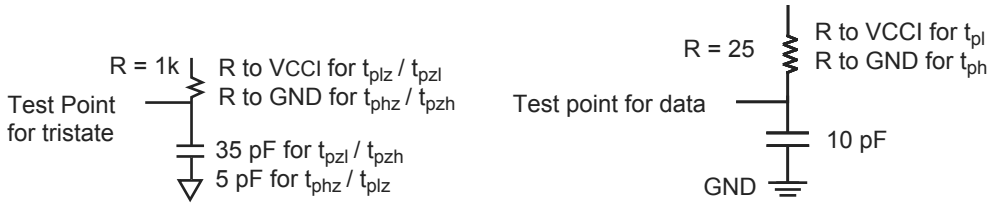

***Figure 2-18 •* AC Test Loads**

***Table 2-34* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C_{load} (pF)
(Per PCI Spec and PCI-X Spec)			N/A	10

*Note: * Measuring Point = VTRIP*

Timing Model and Waveforms

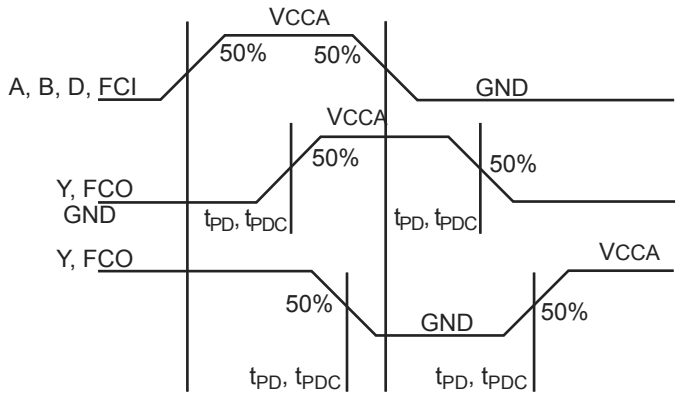

Figure 2-28 • **C-Cell Timing Model and Waveforms**

Timing Characteristics

Table 2-62 • **C-Cell**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays								
t_{PD}	Any input to output Y		0.74		0.84		0.99	ns
t_{PDC}	Any input to carry chain output (FCO)		0.57		0.64		0.76	ns
t_{PDB}	Any input through DB when one input is used		0.95		1.09		1.28	ns
t_{CCY}	Input to carry chain (FCI) to Y		0.61		0.69		0.82	ns
t_{CC}	Input to carry chain (FCI) to carry chain output (FCO)		0.08		0.09		0.11	ns

Timing Characteristics

Table 2-65 • AX125 Predicted Routing Delays
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		–2 Speed	–1 Speed	Std Speed	
Parameter	**Description**	**Typical**	**Typical**	**Typical**	**Units**
Predicted Routing Delays					
t_{DC}	DirectConnect Routing Delay, FO1	0.11	0.12	0.15	ns
t_{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t_{RD1}	Routing delay for FO1	0.35	0.40	0.47	ns
t_{RD2}	Routing delay for FO2	0.38	0.43	0.51	ns
t_{RD3}	Routing delay for FO3	0.43	0.48	0.57	ns
t_{RD4}	Routing delay for FO4	0.48	0.55	0.64	ns
t_{RD5}	Routing delay for FO5	0.55	0.62	0.73	ns
t_{RD6}	Routing delay for FO6	0.64	0.72	0.85	ns
t_{RD7}	Routing delay for FO7	0.79	0.89	1.05	ns
t_{RD8}	Routing delay for FO8	0.88	0.99	1.17	ns
t_{RD16}	Routing delay for FO16	1.49	1.69	1.99	ns
t_{RD32}	Routing delay for FO32	2.32	2.63	3.10	ns

Table 2-66 • AX250 Predicted Routing Delays
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		–2 Speed	–1 Speed	Std Speed	
Parameter	**Description**	**Typical**	**Typical**	**Typical**	**Units**
Predicted Routing Delays					
t_{DC}	DirectConnect Routing Delay, FO1	0.11	0.12	0.15	ns
t_{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t_{RD1}	Routing delay for FO1	0.39	0.45	0.53	ns
t_{RD2}	Routing delay for FO2	0.41	0.46	0.54	ns
t_{RD3}	Routing delay for FO3	0.48	0.55	0.64	ns
t_{RD4}	Routing delay for FO4	0.56	0.63	0.75	ns
t_{RD5}	Routing delay for FO5	0.60	0.68	0.80	ns
t_{RD6}	Routing delay for FO6	0.84	0.96	1.13	ns
t_{RD7}	Routing delay for FO7	0.90	1.02	1.20	ns
t_{RD8}	Routing delay for FO8	1.00	1.13	1.33	ns
t_{RD16}	Routing delay for FO16	2.17	2.46	2.89	ns
t_{RD32}	Routing delay for FO32	3.55	4.03	4.74	ns

Axcelerator Clock Management System

Introduction

Each member of the Axcelerator family[6] contains eight phase-locked loop (PLL) blocks which perform the following functions:

- Programmable Delay (32 steps of 250 ps)
- Clock Skew Minimization
- Clock Frequency Synthesis

Each PLL has the following key features:

- Input Frequency Range – 14 to 200 MHz
- Output Frequency Range – 20 MHz to 1 GHz
- Output Duty Cycle Range – 45% to 55%
- Maximum Long-Term Jitter – 1% or 100ps (whichever is greater)
- Maximum Short-Term Jitter – 50ps + 1% of Output Frequency
- Maximum Acquisition Time (lock) – 20µs

Physical Implementation

The eight PLL blocks are arranged in two groups of four. One group is located in the center of the northern edge of the chip, while the second group is centered on the southern edge. The northern group is associated with the four HCLK networks (e.g. PLLA can drive HCLKA), while the southern group is associated with the four CLK networks (e.g. PLLE can drive CLKE).

Each PLL cell is connected to two I/O pads and a PLL Cluster that interfaces with the FPGA core. Figure 2-48 illustrates a PLL block. The VCCPLL pin should be connected to a 1.5V power supply through a 250 Ω resistor. Furthermore, 0.1 µF and 10 µF decoupling capacitors should be connected across the VCCPLL and VCOMPPLL pins.

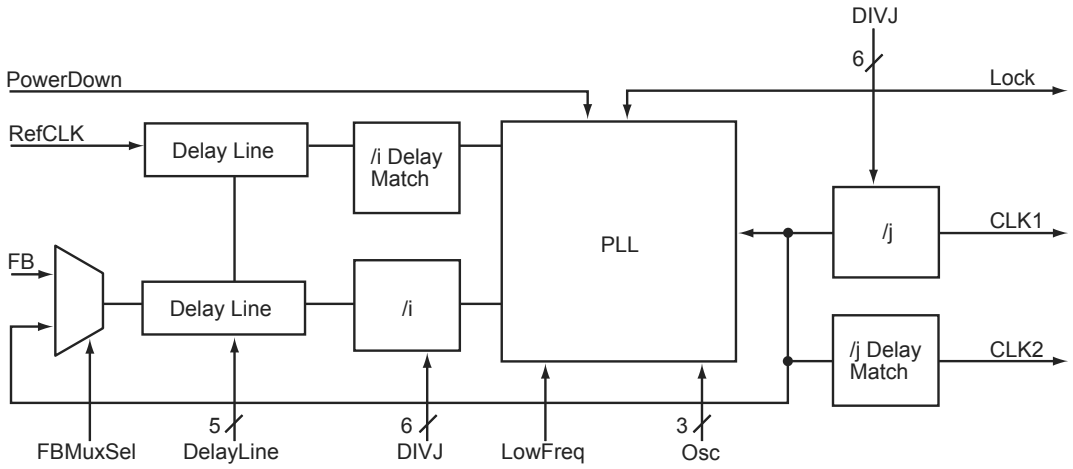

Figure 2-48 • **PLL Block Diagram**

Note: The VCOMPPLL pin should never be grounded (Figure 2-2 on page 2-9)!

The I/O pads associated with the PLL can also be configured for regular I/O functions except when it is used as a clock buffer. The I/O pads can be configured in all the modes available to the regular I/O pads in the same I/O bank. In particular, the [H]CLKxP pad can be configured as a differential pair,

6. *AX2000-CQ256 does not support operation of the phase-locked loops. This is in order to support full pin compatibility with RTAX2000S/SL-CQ256.*

Sample Implementations

Frequency Synthesis

Figure 2-53 illustrates an example where the PLL is used to multiply a 155.5 MHz external clock up to 622 MHz. Note that the same PLL schematic could use an external 350 MHz clock, which is divided down to 155 MHz by the FPGA internal logic.

Figure 2-54 illustrates the PLL using both dividers to synthesize a 133 MHz output clock from a 155 MHz input reference clock. The input frequency of 155 MHz is multiplied by 6 and divided by 7, giving a CLK1 output frequency of 132.86 MHz. When dividers are used, a given ratio can be generated in multiple ways, allowing the user to stay within the operating frequency ranges of the PLL.

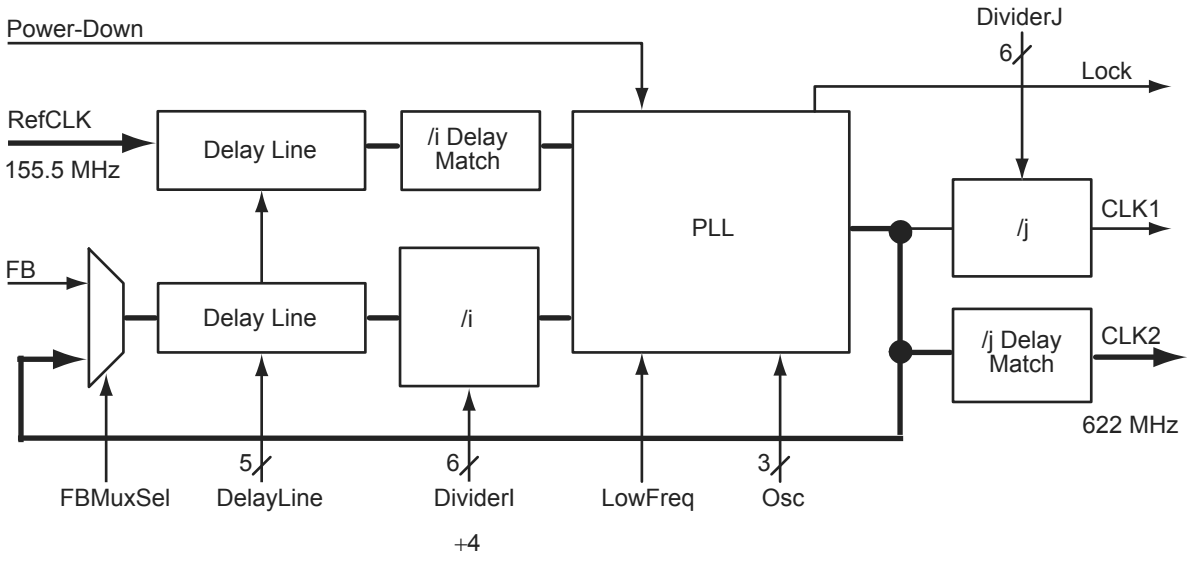

Figure 2-53 • **Using the PLL 155.5 MHz In, 622 MHz Out**

Adjustable Clock Delay

Figure 2-55 illustrates using the PLL to delay the reference clock by employing one of the adjustable delay lines. In this case, the output clock is delayed relative to the reference clock. Delaying the reference clock relative to the output clock is accomplished by using the delay line in the feedback path.

***Table 2-102* • Sixteen FIFO Blocks Cascaded**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
FIFO Module Timing								
t_{WSU}	Write Setup		16.32		18.60		21.86	ns
t_{WHD}	Write Hold		0.00		0.00		0.00	ns
t_{WCKH}	WCLK High		0.75		0.75		0.75	ns
t_{WCKL}	WCLK Low		13.40		13.40		13.40	ns
t_{WCKP}	Minimum WCLK Period	14.15		14.15		14.15		ns
t_{RSU}	Read Setup		17.16		19.54		22.97	ns
t_{RHD}	Read Hold		0.00		0.00		0.00	ns
t_{RCKH}	RCLK High		0.73		0.73		0.73	ns
t_{RCKL}	RCLK Low		14.41		14.41		14.41	ns
t_{RCKP}	Minimum RCLK period	15.14		15.14		15.14		ns
t_{CLRHF}	Clear High		0.00		0.00		0.00	ns
t_{CLR2FF}	Clear-to-flag (EMPTY/FULL)		1.92		2.18		2.57	ns
t_{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)		4.39		5.00		5.88	ns
t_{CK2FF}	Clock-to-flag (EMPTY/FULL)		2.13		2.42		2.85	ns
t_{CK2AF}	Clock-to-flag (AEMPTY/AFULL)		5.04		5.75		6.75	ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		12.08		13.76		16.17	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Nonpipelined)		12.83		14.62		17.18	ns

Note: Timing data for these sixteen cascaded FIFO blocks uses a depth of 65,536. For all other combinations, use Microsemi's timing software.

Building RAM and FIFO Modules

RAM and FIFO modules can be generated and included in a design in two different ways:

- Using the SmartGen Core Generator where the user defines the depth and width of the FIFO/RAM, and then instantiates this block into the design (refer to the *SmartGen, FlashROM, Analog System Builder, and Flash Memory System Builder* User's Guide for more information).
- The alternative is to instantiate the RAM/FIFO blocks manually, using inverters for polarity control and tying all unused data bits to ground.

Other Architectural Features

Low Power Mode

Although designed for high performance, the AX architecture also allows the user to place the device into a low power mode. Each I/O bank in an Axcelerator device can be configured individually, when in low power mode, to tristate all outputs, disable inputs, or both. The low power mode is activated by asserting the LP pin, which is grounded in normal operation.

While in the low power mode, the device is still fully functional and all internal logic states are preserved. This allows a user to disable all but a few signals and operate the part in a low-frequency, watchdog

BG729	
AX1000 Function	Pin Number
IO54PB1F5	E20
IO55NB1F5	E21
IO55PB1F5	D21
IO56NB1F5	H19
IO56PB1F5	G19
IO57NB1F5	D22
IO57PB1F5	C22
IO58NB1F5	B23
IO58PB1F5	A23
IO59NB1F5	D23
IO59PB1F5	C23
IO60NB1F5	G21
IO60PB1F5	G20
IO61NB1F5	E23
IO61PB1F5	E22
IO62NB1F5	F22
IO62PB1F5	F21
IO63NB1F5	H20
IO63PB1F5	J19
Bank 2	
IO64NB2F6	J21
IO64PB2F6	H21
IO65NB2F6	F24
IO65PB2F6	F23
IO66NB2F6	F26
IO66PB2F6	F25
IO67NB2F6	E26
IO67PB2F6	E25
IO68NB2F6	J22
IO68PB2F6	H22
IO69NB2F6	G24
IO69PB2F6	G23
IO70NB2F6	K20
IO70PB2F6	J20
IO71NB2F6	G26
IO71PB2F6	G25
IO72NB2F6	J24

BG729	
AX1000 Function	Pin Number
IO72PB2F6	J23
IO73NB2F6	H24
IO73PB2F6	H23
IO74NB2F7	L21
IO74PB2F7	K21
IO75NB2F7	G27
IO75PB2F7	F27
IO76NB2F7	K23
IO76PB2F7	K22
IO77NB2F7	H26
IO77PB2F7	H25
IO78NB2F7	K25
IO78PB2F7	K24
IO79NB2F7	J26
IO79PB2F7	J25
IO80NB2F7	M20
IO80PB2F7	L20
IO81NB2F7	J27
IO81PB2F7	H27
IO82NB2F7	L23
IO82PB2F7	L22
IO83NB2F7	L25
IO83PB2F7	L24
IO84NB2F7	N21
IO84PB2F7	M21
IO85NB2F8	K27
IO85PB2F8	K26
IO86NB2F8	M23
IO86PB2F8	M22
IO87NB2F8	M25
IO87PB2F8	M24
IO88NB2F8	L27
IO88PB2F8	L26
IO89NB2F8	M27
IO89PB2F8	M26
IO90NB2F8	N23
IO90PB2F8	N22

BG729	
AX1000 Function	Pin Number
IO91NB2F8	N25
IO91PB2F8	N24
IO92NB2F8	N27
IO92PB2F8	N26
IO93NB2F8	P26
IO93PB2F8	P27
IO94NB2F8	N19
IO94PB2F8	N20
IO95NB2F8	P23
IO95PB2F8	P22
Bank 3	
IO96NB3F9	P25
IO96PB3F9	P24
IO97NB3F9	R26
IO97PB3F9	R27
IO98NB3F9	P21
IO98PB3F9	P20
IO99NB3F9	R24
IO99PB3F9	R25
IO100NB3F9	T26
IO100PB3F9	T27
IO101NB3F9	T24
IO101PB3F9	T25
IO102NB3F9	R20
IO102PB3F9	R21
IO103NB3F9	R23
IO103PB3F9	R22
IO104NB3F9	U26
IO104PB3F9	U27
IO105NB3F9	U24
IO105PB3F9	U25
IO106NB3F9	R19
IO106PB3F9	P19
IO107NB3F10	V26
IO107PB3F10	V27
IO108NB3F10	T23
IO108PB3F10	T22

FG484	
AX500 Function	Pin Number
IO54PB2F5	H22
IO55NB2F5	L17
IO55PB2F5	K17
IO56NB2F5	K21
IO56PB2F5	K22
IO58NB2F5	L20
IO58PB2F5	K20
IO59NB2F5	L18
IO59PB2F5	K18
IO60NB2F5	M21
IO60PB2F5	L21
IO61NB2F5	L16
IO61PB2F5	K16
IO62NB2F5	M19
IO62PB2F5	L19
Bank 3	
IO63NB3F6	N16
IO63PB3F6	M16
IO64NB3F6	P22
IO64PB3F6	N22
IO65NB3F6	N20
IO65PB3F6	M20
IO66NB3F6	P21
IO66PB3F6	N21
IO67NB3F6	N18
IO67PB3F6	N19
IO68NB3F6	T22
IO68PB3F6	R22
IO69NB3F6	N17
IO69PB3F6	M17
IO70NB3F6	T21
IO70PB3F6	R21
IO71NB3F6	P18
IO71PB3F6	P19
IO72NB3F6	R20

FG484	
AX500 Function	Pin Number
IO72PB3F6	P20
IO73PB3F6	R19
IO74NB3F7	V21
IO74PB3F7	U21
IO75NB3F7	V22
IO75PB3F7	U22
IO76NB3F7	U20
IO76PB3F7	T20
IO77NB3F7	R17
IO77PB3F7	P17
IO78NB3F7	W21
IO78PB3F7	W22
IO79NB3F7	T18
IO79PB3F7	R18
IO80NB3F7	W20
IO80PB3F7	V20
IO81NB3F7	U19
IO81PB3F7	T19
IO82NB3F7	U18
IO82PB3F7	V19
IO83NB3F7	R16
IO83PB3F7	P16
Bank 4	
IO84NB4F8	AB18
IO84PB4F8	AB19
IO85NB4F8	T15
IO85PB4F8	T16
IO86NB4F8	AA18
IO86PB4F8	AA19
IO87NB4F8	W17
IO87PB4F8	V17
IO88NB4F8	Y19
IO88PB4F8	W18
IO89NB4F8	U14
IO89PB4F8	U15

FG484	
AX500 Function	Pin Number
IO90NB4F8	Y17
IO90PB4F8	Y18
IO91NB4F8	V15
IO91PB4F8	V16
IO92PB4F8	AB17
IO93NB4F8	Y15
IO93PB4F8	Y16
IO94NB4F9	AA16
IO94PB4F9	AA17
IO95NB4F9	AB14
IO95PB4F9	AB15
IO96NB4F9	W15
IO96PB4F9	W16
IO97NB4F9	AA13
IO97PB4F9	AB13
IO98NB4F9	AA14
IO98PB4F9	AA15
IO100NB4F9	Y14
IO100PB4F9	W14
IO101NB4F9	Y12
IO101PB4F9	Y13
IO102NB4F9	AA11
IO102PB4F9	AA12
IO103NB4F9/CLKEN	V12
IO103PB4F9/CLKEP	V13
IO104NB4F9/CLKFN	W11
IO104PB4F9/CLKFP	W12
Bank 5	
IO105NB5F10/CLKGN	U10
IO105PB5F10/CLKGP	U11
IO106NB5F10/CLKHN	V9
IO106PB5F10/CLKHP	V10
IO107NB5F10	Y10
IO107PB5F10	Y11
IO108NB5F10	AA9

FG676	
AX1000 Function	**Pin Number**
GND	A8
GND	AC23
GND	AC4
GND	AD24
GND	AD3
GND	AE2
GND	AE25
GND	AF1
GND	AF13
GND	AF14
GND	AF19
GND	AF26
GND	AF8
GND	B2
GND	B25
GND	B26
GND	C24
GND	C3
GND	G20
GND	G7
GND	H1
GND	H19
GND	H26
GND	H8
GND	J18
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	K14
GND	K15
GND	K16
GND	K17
GND	L10
GND	L11

FG676	
AX1000 Function	**Pin Number**
GND	L12
GND	L13
GND	L14
GND	L15
GND	L16
GND	L17
GND	M10
GND	M11
GND	M12
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	N1
GND	N10
GND	N11
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N26
GND	P1
GND	P10
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P26
GND	R10
GND	R11

FG676	
AX1000 Function	**Pin Number**
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	T10
GND	T11
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	U10
GND	U11
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	V18
GND	V9
GND	W1
GND	W19
GND	W26
GND	W8
GND	Y20
GND	Y7
GND/LP	C2
NC	A25
NC	AC13
NC	AC14
NC	AF2
NC	AF25

FG896	
AX1000 Function	Pin Number
NC	K1
NC	K2
NC	L30
NC	M30
NC	N29
NC	T1
NC	U1
NC	W30
NC	Y1
NC	Y2
NC	Y30
PRA	G15
PRB	D16
PRC	AB16
PRD	AF16
TCK	G7
TDI	D5
TDO	J8
TMS	F6
TRST	C4
VCCA	AD6
VCCA	AH26
VCCA	E28
VCCA	E3
VCCA	L12
VCCA	L13
VCCA	L14
VCCA	L15
VCCA	L16
VCCA	L17
VCCA	L18
VCCA	L19
VCCA	M11
VCCA	M20
VCCA	N11

FG896	
AX1000 Function	Pin Number
VCCA	N20
VCCA	P11
VCCA	P20
VCCA	R11
VCCA	R20
VCCA	T11
VCCA	T20
VCCA	U11
VCCA	U20
VCCA	V11
VCCA	V20
VCCA	W11
VCCA	W20
VCCA	Y12
VCCA	Y13
VCCA	Y14
VCCA	Y15
VCCA	Y16
VCCA	Y17
VCCA	Y18
VCCA	Y19
VCCPLA	G14
VCCPLB	H15
VCCPLC	G17
VCCPLD	J16
VCCPLE	AH17
VCCPLF	AC16
VCCPLG	AH14
VCCPLH	AD15
VCCDA	AD24
VCCDA	AD7
VCCDA	AF12
VCCDA	AF13
VCCDA	AF15
VCCDA	AF18

FG896	
AX1000 Function	Pin Number
VCCDA	AF19
VCCDA	C13
VCCDA	C5
VCCDA	D13
VCCDA	D19
VCCDA	D3
VCCDA	E18
VCCDA	F26
VCCDA	G16
VCCDA	T25
VCCDA	T4
VCCIB0	A3
VCCIB0	B3
VCCIB0	J10
VCCIB0	J11
VCCIB0	J12
VCCIB0	K11
VCCIB0	K12
VCCIB0	K13
VCCIB0	K14
VCCIB0	K15
VCCIB1	A28
VCCIB1	B28
VCCIB1	J19
VCCIB1	J20
VCCIB1	J21
VCCIB1	K16
VCCIB1	K17
VCCIB1	K18
VCCIB1	K19
VCCIB1	K20
VCCIB2	C29
VCCIB2	C30
VCCIB2	K22
VCCIB2	L21

FG896	
AX2000 Function	Pin Number
Bank 0	
IO00NB0F0	B4
IO00PB0F0	A4
IO01NB0F0	F8
IO01PB0F0	F7
IO02NB0F0	D6
IO02PB0F0	E6
IO04NB0F0	A5
IO04PB0F0	B5
IO05NB0F0	H8
IO05PB0F0	G8
IO06NB0F0	D7
IO06PB0F0	E7
IO07NB0F0	D8
IO07PB0F0	E8
IO08NB0F0	C7
IO08PB0F0	C6
IO09NB0F0	G9
IO09PB0F0	H9
IO10NB0F0	A6
IO10PB0F0	B6
IO11NB0F0	H10
IO11PB0F0	G10
IO12NB0F1	E9
IO12PB0F1	F9
IO13NB0F1	E10
IO13PB0F1	F10
IO15NB0F1	F11
IO15PB0F1	G11
IO16NB0F1	A7
IO16PB0F1	B7
IO17NB0F1	D10
IO17PB0F1	D9
IO18NB0F1	C9
IO18PB0F1	C8

FG896	
AX2000 Function	Pin Number
IO19NB0F1	D11
IO19PB0F1	E11
IO20PB0F1	B8
IO21NB0F1	H12
IO21PB0F1	H11
IO23NB0F2	A10
IO23PB0F2	A9
IO25NB0F2	F12
IO25PB0F2	G12
IO26NB0F2	B11
IO26PB0F2	B10
IO27NB0F2	D12
IO27PB0F2	E12
IO28NB0F2	C12
IO28PB0F2	C11
IO30NB0F2	A12
IO30PB0F2	A11
IO31NB0F2	F13
IO31PB0F2	G13
IO33NB0F2	H13
IO33PB0F2	J13
IO34NB0F3	B13
IO34PB0F3	B12
IO37NB0F3	E14
IO37PB0F3	E13
IO38NB0F3	B14
IO38PB0F3	A14
IO39NB0F3	H14
IO39PB0F3	J14
IO40NB0F3	B15
IO40PB0F3	A15
IO41NB0F3/HCLKAN	C14
IO41PB0F3/HCLKAP	D14
IO42NB0F3/HCLKBN	E15
IO42PB0F3/HCLKBP	D15

FG896	
AX2000 Function	Pin Number
Bank 1	
IO43NB1F4/HCLKCN	E17
IO43PB1F4/HCLKCP	E16
IO44NB1F4/HCLKDN	C17
IO44PB1F4/HCLKDP	D17
IO45NB1F4	A16
IO45PB1F4	B16
IO47NB1F4	H17
IO47PB1F4	J17
IO48NB1F4	A17
IO48PB1F4	B17
IO49NB1F4	H18
IO49PB1F4	J18
IO51NB1F4	F18
IO51PB1F4	G18
IO52NB1F4	B18
IO53NB1F4	D18
IO53PB1F4	C18
IO55NB1F5	H19
IO55PB1F5	G19
IO56NB1F5	B19
IO56PB1F5	A19
IO57NB1F5	E20
IO57PB1F5	E19
IO58NB1F5	C20
IO58PB1F5	C19
IO59NB1F5	B20
IO59PB1F5	A20
IO61NB1F5	F20
IO61PB1F5	F19
IO62NB1F5	A22
IO62PB1F5	A21
IO63NB1F5	D21
IO63PB1F5	D20
IO65NB1F6	G20

FG1152	
AX2000 Function	Pin Number
IO155PB3F14	AC29
IO156NB3F14	AE30
IO156PB3F14	AD30
IO157NB3F14	AC26
IO157PB3F14	AB26
IO158NB3F14	AH33
IO158PB3F14	AG33
IO159NB3F14	AD27
IO159PB3F14	AC27
IO160NB3F14	AG32
IO160PB3F14	AF32
IO161NB3F15	AG31
IO161PB3F15	AF31
IO162NB3F15	AF29
IO162PB3F15	AE29
IO163NB3F15	AE28
IO163PB3F15	AD28
IO164NB3F15	AG30
IO164PB3F15	AF30
IO165NB3F15	AE26
IO165PB3F15	AD26
IO166NB3F15	AJ30
IO166PB3F15	AH30
IO167NB3F15	AG28
IO167PB3F15	AF28
IO168NB3F15	AF27
IO168PB3F15	AE27
IO169NB3F15	AH29
IO169PB3F15	AG29
IO170NB3F15	AD25
IO170PB3F15	AC25
Bank 4	
IO171NB4F16	AP29
IO171PB4F16	AN29
IO172NB4F16	AH26

FG1152	
AX2000 Function	Pin Number
IO172PB4F16	AH27
IO173NB4F16	AJ27
IO173PB4F16	AJ28
IO174NB4F16	AL27
IO174PB4F16	AL28
IO175NB4F16	AM28
IO175PB4F16	AM29
IO176NB4F16	AG25
IO176PB4F16	AG26
IO177NB4F16	AK26
IO177PB4F16	AK27
IO178NB4F16	AF25
IO178PB4F16	AE25
IO179NB4F16	AP28
IO179PB4F16	AN28
IO180NB4F16	AJ25
IO180PB4F16	AJ26
IO181NB4F17	AM26
IO181PB4F17	AM27
IO182NB4F17	AF24
IO182PB4F17	AE24
IO183NB4F17	AH24
IO183PB4F17	AH25
IO184NB4F17	AG23
IO184PB4F17	AG24
IO185NB4F17	AL25
IO185PB4F17	AL26
IO186NB4F17	AP25
IO186PB4F17	AP26
IO187NB4F17	AK24
IO187PB4F17	AK25
IO188NB4F17	AF23
IO188PB4F17	AE23
IO189NB4F17	AN24
IO189PB4F17	AM24

FG1152	
AX2000 Function	Pin Number
IO190NB4F17	AH22
IO190PB4F17	AH23
IO191NB4F17	AJ23
IO191PB4F17	AJ24
IO192NB4F17	AG21
IO192PB4F17	AG22
IO193NB4F18	AP23
IO193PB4F18	AP24
IO194NB4F18	AN22
IO194PB4F18	AN23
IO195NB4F18	AM23
IO195PB4F18	AL23
IO196NB4F18	AF21
IO196PB4F18	AF22
IO197NB4F18	AL22
IO197PB4F18	AM22
IO198NB4F18	AE21
IO198PB4F18	AE22
IO199NB4F18	AJ21
IO199PB4F18	AJ22
IO200NB4F18	AK21
IO200PB4F18	AK22
IO201NB4F18	AM21
IO201PB4F18	AL21
IO202NB4F18	AE20
IO202PB4F18	AD20
IO203NB4F19	AN21
IO203PB4F19	AP21
IO204NB4F19	AP20
IO204PB4F19	AN20
IO205NB4F19	AN19
IO205PB4F19	AP19
IO206NB4F19	AG20
IO206PB4F19	AF20
IO207NB4F19	AL19

PQ208	
AX250 Function	Pin Number
Bank 0	
IO02NB0F0	197
IO03NB0F0	198
IO03PB0F0	199
IO12NB0F0/HCLKAN	191
IO12PB0F0/HCLKAP	192
IO13NB0F0/HCLKBN	185
IO13PB0F0/HCLKBP	186
Bank 1	
IO14NB1F1/HCLKCN	180
IO14PB1F1/HCLKCP	181
IO15NB1F1/HCLKDN	174
IO15PB1F1/HCLKDP	175
IO16NB1F1	170
IO16PB1F1	171
IO24NB1F1	165
IO24PB1F1	166
IO26NB1F1	161
IO26PB1F1	162
IO27NB1F1	159
IO27PB1F1	160
Bank 2	
IO29NB2F2	151
IO29PB2F2	153
IO30NB2F2	152
IO30PB2F2	154
IO31PB2F2	148
IO32NB2F2	146
IO32PB2F2	147
IO34NB2F2	144
IO34PB2F2	145
IO39NB2F2	139
IO39PB2F2	140
IO40PB2F2	141
IO41NB2F2	137
IO41PB2F2	138
IO43NB2F2	132

PQ208	
AX250 Function	Pin Number
IO43PB2F2	134
IO44NB2F2	131
IO44PB2F2	133
Bank 3	
IO45NB3F3	127
IO45PB3F3	129
IO46NB3F3	126
IO46PB3F3	128
IO48NB3F3	122
IO48PB3F3	123
IO50NB3F3	120
IO50PB3F3	121
IO55NB3F3	116
IO55PB3F3	117
IO57NB3F3	114
IO57PB3F3	115
IO59NB3F3	110
IO59PB3F3	111
IO60NB3F3	108
IO60PB3F3	109
IO61NB3F3	106
IO61PB3F3	107
Bank 4	
IO62NB4F4	100
IO62PB4F4	103
IO63NB4F4	101
IO63PB4F4	102
IO64NB4F4	96
IO64PB4F4	97
IO72NB4F4	91
IO72PB4F4	92
IO74NB4F4/CLKEN	87
IO74PB4F4/CLKEP	88
IO75NB4F4/CLKFN	81
IO75PB4F4/CLKFP	82
Bank 5	
IO76NB5F5/CLKGN	76

PQ208	
AX250 Function	Pin Number
IO76PB5F5/CLKGP	77
IO77NB5F5/CLKHN	70
IO77PB5F5/CLKHP	71
IO78NB5F5	66
IO78PB5F5	67
IO86NB5F5	62
IO87NB5F5	60
IO87PB5F5	61
IO88NB5F5	56
IO88PB5F5	57
IO89NB5F5	54
IO89PB5F5	55
Bank 6	
IO91NB6F6	47
IO91PB6F6	49
IO92NB6F6	48
IO92PB6F6	50
IO93NB6F6	42
IO93PB6F6	43
IO94PB6F6	44
IO96NB6F6	40
IO96PB6F6	41
IO101NB6F6	35
IO101PB6F6	36
IO102PB6F6	37
IO103NB6F6	33
IO103PB6F6	34
IO105NB6F6	28
IO105PB6F6	30
IO106NB6F6	27
IO106PB6F6	29
Bank 7	
IO107NB7F7	23
IO107PB7F7	25
IO108NB7F7	22
IO108PB7F7	24
IO110NB7F7	18

CQ352	
AX500 Function	Pin Number
GND	21
GND	27
GND	33
GND	39
GND	45
GND	51
GND	57
GND	63
GND	69
GND	75
GND	81
GND	88
GND	89
GND	97
GND	103
GND	109
GND	115
GND	121
GND	133
GND	145
GND	151
GND	157
GND	163
GND	169
GND	176
GND	177
GND	186
GND	192
GND	198
GND	204
GND	210
GND	216
GND	222
GND	228
GND	234

CQ352	
AX500 Function	Pin Number
GND	240
GND	246
GND	252
GND	258
GND	264
GND	265
GND	274
GND	280
GND	286
GND	292
GND	298
GND	310
GND	322
GND	330
GND	334
GND	340
GND	345
GND/LP	352
NC	91
NC	117
NC	130
NC	131
NC	148
NC	174
NC	268
NC	294
NC	307
NC	308
NC	327
NC	328
PRA	312
PRB	311
PRC	135
PRD	134
TCK	349

CQ352	
AX500 Function	Pin Number
TDI	348
TDO	347
TMS	350
TRST	351
VCCA	3
VCCA	14
VCCA	32
VCCA	56
VCCA	74
VCCA	87
VCCA	102
VCCA	114
VCCA	150
VCCA	162
VCCA	175
VCCA	191
VCCA	209
VCCA	233
VCCA	251
VCCA	263
VCCA	279
VCCA	291
VCCA	329
VCCA	339
VCCDA	2
VCCDA	44
VCCDA	90
VCCDA	116
VCCDA	132
VCCDA	149
VCCDA	178
VCCDA	221
VCCDA	266
VCCDA	293
VCCDA	309