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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	8064
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	115
Number of Gates	500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax500-pqg208

Ordering Information

AX1000 – 1 FG G 896 I

- **Application**
  - Blank = Commercial (0 to +70° C)
  - PP = Pre-Production
  - I = Industrial (-40 to +85° C)
  - M = Military (-55 to +125° C)
- **Package Lead Count**
- **Lead-Free Packaging**
  - Blank = Standard Packaging
  - G = RoHS-Compliant Packaging
- **Package Type**
  - BG = Ball Grid Array (1.27mm pitch)
  - FG = Fine Ball Grid Array (1.0mm pitch)
  - PQ = Plastic Quad Flat Pack (0.5mm pitch)
  - CQ = Ceramic Quad Flat Pack (0.5mm pitch)
  - CG = Ceramic Column Grid Array
- **Speed Grade**
  - Blank = Standard Speed
  - 1 = Approximately 15% Faster than Standard
  - 2 = Approximately 25% Faster than Standard
- **Part Number**
  - AX125 = 125,000 Equivalent System Gates
  - AX250 = 250,000 Equivalent System Gates
  - AX500 = 500,000 Equivalent System Gates
  - AX1000 = 1,000,000 Equivalent System Gates
  - AX2000 = 2,000,000 Equivalent System Gates

Device Resources

User I/Os (Including Clock Buffers)					
Package	**AX125**	**AX250**	**AX500**	**AX1000**	**AX2000**
PQ208	–	115	115	–	–
CQ208	–	115	115	–	–
CQ256	–	–	–	–	136
FG256	138	138	–	–	–
FG324	168	–	–	–	–
CQ352	–	198	198	198	198
FG484	–	248	317	317	–
CG624	–	–	–	418	418
FG676	–	–	336	418	–
BG729	–	–	–	516	–
FG896	–	–	–	516	586
FG1152	–	–	–	–	684

Note: The FG256, FG324, and FG484 are footprint compatible with one another. The FG676, FG896, and FG1152 are also footprint compatible with one another.

Figure 1-2 • **Axcelerator Family Interconnect Elements**

Logic Modules

Microsemi's Axcelerator family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell). The Axcelerator device can implement more than 4,000 combinatorial functions of up to five inputs (Figure 1-3).

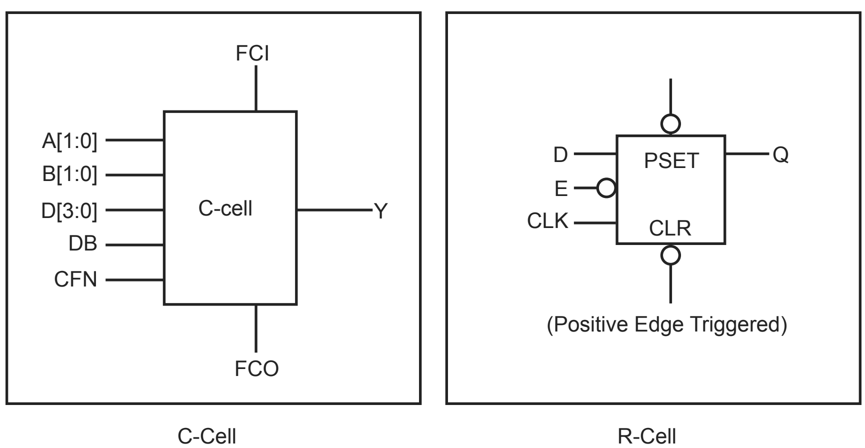


Figure 1-3 • **AX C-Cell and R-Cell**

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and active-low enable control signals (Figure 1-3). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility (e.g., easy mapping of dual-data-rate functions into the FPGA) while conserving valuable clock resources. The clock source for the R-cell can be chosen from the hardwired clocks, routed clocks, or internal logic.

Poutputs = PI/O * po * Fpo

C_{load} = the output load (technology dependent)
VCCI = the output voltage (technology dependent)
po = the number of outputs
F_{po} = the average output frequency

Pmemory = P11 * Nblock * FRCLK + P12 * Nblock * FWCLK

N_{block} = the number of RAM/FIFO blocks (1 block = 4k)
F_{RCLK} = the read-clock frequency of the memory
F_{WCLK} = the write-clock frequency of the memory

PPLL = P13 * FCLK

F_{RefCLK} = the clock frequency of the clock input of the PLL
F_{CLK} = the clock frequency of the first clock output of the PLL

Power Estimation Example

This example employs an AX1000 shift-register design with 1,080 R-cells, one C-cell, one reset input, and one LVTTL 12 mA output, with high slew.

This design uses one HCLK at 100 MHz.

ms = 1,080 (in a shift register - 100% of R-cells are toggling at each clock cycle)
Fs = 100 MHz
s = 1080
=> P_{HCLK} = (P1 + P2 * s + P3 * sqrt[s]) * Fs = 79 mW
and Fs = 100 MHz
=> $P_{R\text{-}cells}$ = P7 * ms * Fs = 173 mW
mc = 1 (1 C-cell in this shift-register)
and Fs = 100 MHz
=> $P_{C\text{-}cells}$ = P8 * mc * Fs = 0.14 mW
F_{pi} ~ 0 MHz
and pi= 1 (1 reset input => this is why F_{pi}=0)
=> P_{inputs} = P9 * pi * F_{pi} = 0 mW
F_{po} = 50 MHz
and po = 1
=> $P_{outputs}$ = $P_{I/O}$ * po * F_{po}= 27.10 mW
No RAM/FIFO in this shift-register
=> P_{memory} = 0 mW
No PLL in this shift-register
=> P_{PLL} = 0 mW
$P_{ac} = P_{HCLK} + P_{CLK} + P_{R\text{-}cells} + P_{C\text{-}cells} + P_{inputs} + P_{outputs} + P_{memory} + P_{PLL}$ = 276 mW
P_{dc} = 7.5mA * 1.5V = 11.25 mW
$P_{total} = P_{dc} + P_{ac}$ = 11.25 mW + 276mW = 290.30 mW

Thermal Characteristics

Introduction

The temperature variable in Microsemi's Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction temperature to be higher than the ambient temperature. EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_a$$

EQ 1

Where:

T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient

$$\Delta T = \theta_{ja} * P$$

EQ 2

Where:

P = Power

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located under Table 2-6 on page 2-7.

Package Thermal Characteristics

The device junction-to-case thermal characteristic is θ_{jc}, and the junction-to-ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates. θ_{jc} values are provided for reference. The absolute maximum junction temperature is 125°C.

The maximum power dissipation allowed for commercial- and industrial-grade devices is a function of θ_{ja}. A sample calculation of the absolute maximum power dissipation allowed for an 896-pin FBGA package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. }(^\circ\text{C}) - \text{Max. ambient temp. }(^\circ\text{C})}{\theta_{ja}(^\circ\text{C/W})} = \frac{125^\circ\text{C} - 70^\circ\text{C}}{13.6^\circ\text{C/W}} = 4.04\text{ W}$$

Table 2-22 • 3.3 V LVTTL I/O Module
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVTTL Output Drive Strength = 1 (8 mA) / High Slew Rate								
t_{DP}	Input Buffer		1.68		1.92		2.26	ns
t_{PY}	Output Buffer		4.23		4.81		5.66	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		4.64		5.28		6.21	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		4.23		4.81		5.66	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.89		1.91		1.91	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.01		2.02		2.03	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Implementation Example:

Figure 2-47 shows a complex clock distribution example. The reference clock (RefCLK) of PLLE is being sourced from non-clock signal pins (INBUF to PLLINT). The CLK1 output of PLLE is being fed to the RefCLK input of PLLF. The CLK2 output of PLLE is driving logic (via PLLOUT). In turn, this logic is driving the global resource CLKE. PLLF is driving both CLKF and CLKG global resources.

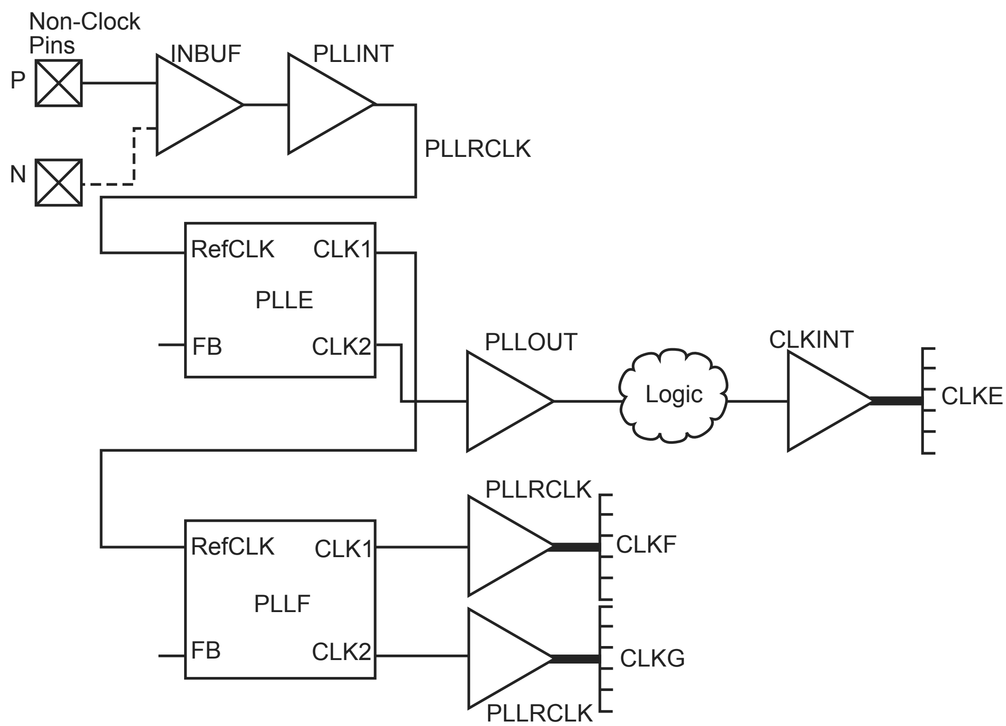


Figure 2-47 • **Complex Clock Distribution Example**

FIFO

Every memory block has its own embedded FIFO controller. Each FIFO block has one read port and one write port. This embedded FIFO controller uses no internal FPGA logic and features:

- Glitch-free FIFO Flags
- Gray-code address counters/pointers to prevent metastability problems
- Overflow and underflow control

Both ports are configurable in various sizes from 4k x 1 to 128 x 36, similar to the RAM block size. Each port is fully synchronous.

Read and write operations can be completely independent. Data on the appropriate WD pins are written to the FIFO on every active WCLK edge as long as WEN is high. Data is read from the FIFO and output on the appropriate RD pins on every active RCLK edge as long as REN is asserted.

The FIFO block offers programmable almost-empty (AEMPTY) and almost-full (AFULL) flags as well as EMPTY and FULL flags (Figure 2-61):

- The FULL flag is synchronous to WCLK. It allows the FIFO to inhibit writing when full.
- The EMPTY flag is synchronous to RCLK. It allows the FIFO to inhibit reading at the empty condition.

Gray code counters are used to prevent metastability problems associated with flag logic. The depth of the FIFO is dependent on the data width and the number of memory blocks used to create the FIFO. The write operations to the FIFO are synchronous with respect to the WCLK, and the read operations are synchronous with respect to the RCLK.

The FIFO block may be reset to the empty state.

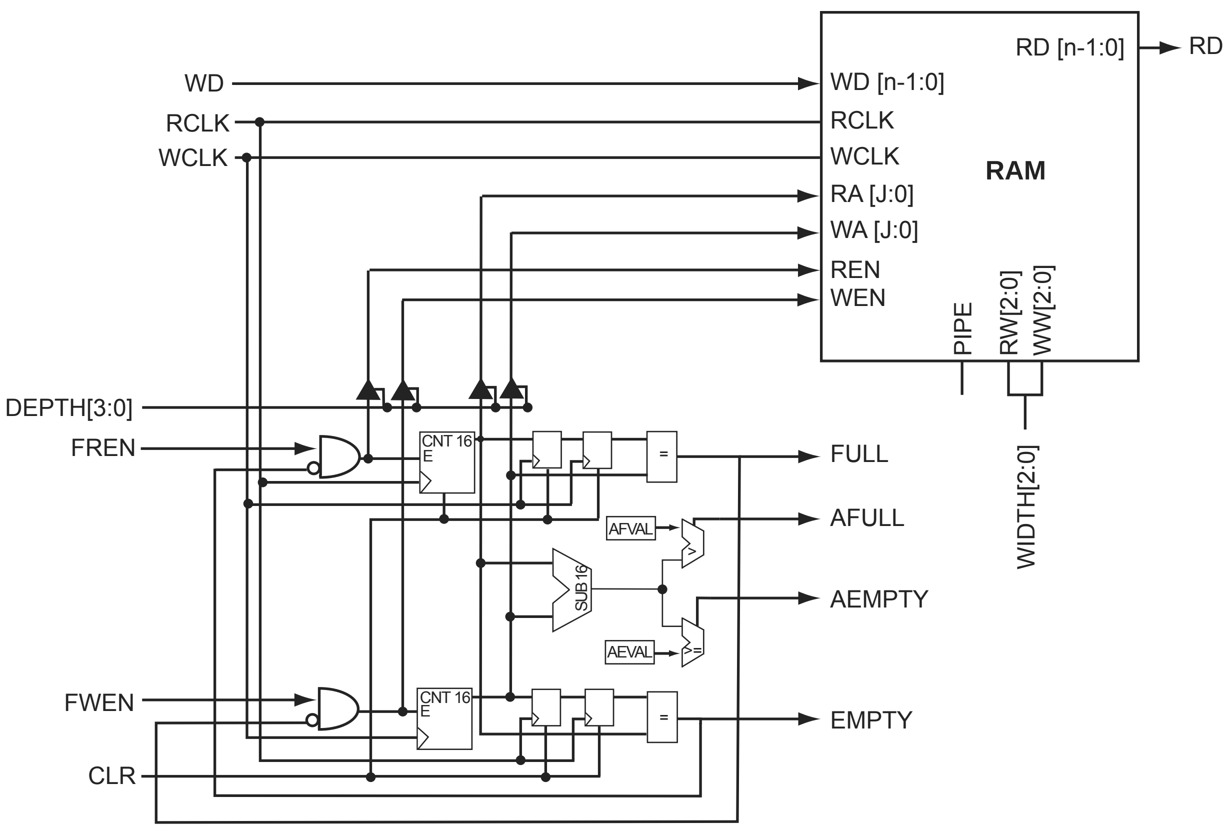


Figure 2-61 • **Axcelerator RAM with Embedded FIFO Controller**

BG729	
AX1000 Function	**Pin Number**
VCCIB0	B4
VCCIB0	C4
VCCIB0	J10
VCCIB0	J11
VCCIB0	J12
VCCIB0	K12
VCCIB0	K13
VCCIB1	A24
VCCIB1	B24
VCCIB1	C24
VCCIB1	J16
VCCIB1	J17
VCCIB1	J18
VCCIB1	K15
VCCIB1	K16
VCCIB2	D25
VCCIB2	D26
VCCIB2	D27
VCCIB2	K19
VCCIB2	L19
VCCIB2	M18
VCCIB2	M19
VCCIB2	N18
VCCIB3	AD25
VCCIB3	AD26
VCCIB3	AD27
VCCIB3	R18
VCCIB3	T18
VCCIB3	T19
VCCIB3	U19
VCCIB3	V19
VCCIB4	AE24
VCCIB4	AF24
VCCIB4	AG24
VCCIB4	V15
VCCIB4	V16
VCCIB4	W16

BG729	
AX1000 Function	**Pin Number**
VCCIB4	W17
VCCIB4	W18
VCCIB5	AE4
VCCIB5	AF4
VCCIB5	AG4
VCCIB5	V12
VCCIB5	V13
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB6	AD1
VCCIB6	AD2
VCCIB6	AD3
VCCIB6	R10
VCCIB6	T10
VCCIB6	T9
VCCIB6	U9
VCCIB6	V9
VCCIB7	D1
VCCIB7	D2
VCCIB7	D3
VCCIB7	K9
VCCIB7	L9
VCCIB7	M10
VCCIB7	M9
VCCIB7	N10
VCOMPLA	B13
VCOMPLB	A14
VCOMPLC	A15
VCOMPLD	J15
VCOMPLE	AG15
VCOMPLF	W15
VCOMPLG	AC14
VCOMPLH	W13
VPUMP	D24

FG324	
AX125 Function	Pin Number
Bank 0	
IO00NB0F0	C5
IO00PB0F0	C4
IO01NB0F0	A3
IO01PB0F0	A2
IO02NB0F0	C7
IO02PB0F0	C6
IO03NB0F0	B5
IO03PB0F0	B4
IO04NB0F0	A5
IO04PB0F0	A4
IO05NB0F0	A7
IO05PB0F0	A6
IO06NB0F0	B7
IO06PB0F0	B6
IO07NB0F0/HCLKAN	C9
IO07PB0F0/HCLKAP	C8
IO08NB0F0/HCLKBN	B10
IO08PB0F0/HCLKBP	B9
Bank 1	
IO09NB1F1/HCLKCN	D11
IO09PB1F1/HCLKCP	D10
IO10NB1F1/HCLKDN	C12
IO10PB1F1/HCLKDP	C11
IO11NB1F1	A15
IO11PB1F1	A14
IO12NB1F1	B14
IO12PB1F1	B13
IO13NB1F1	A17
IO13PB1F1	A16
IO14NB1F1	D13
IO14PB1F1	D12
IO15NB1F1	C14
IO15PB1F1	C13
IO16NB1F1	B16

FG324	
AX125 Function	Pin Number
IO16PB1F1	C15
IO17NB1F1	E14
IO17PB1F1	E13
Bank 2	
IO18NB2F2	G14
IO18PB2F2	F14
IO19NB2F2	D16
IO19PB2F2	D15
IO20NB2F2	C18
IO20PB2F2	B18
IO21NB2F2	D17
IO21PB2F2	C17
IO22NB2F2	F17
IO22PB2F2	E17
IO23NB2F2	G16
IO23PB2F2	F16
IO24NB2F2	E18
IO24PB2F2	D18
IO25NB2F2	G18
IO25PB2F2	F18
IO26NB2F2	H17
IO26PB2F2	G17
IO27NB2F2	J16
IO27PB2F2	H16
IO28NB2F2	J18
IO28PB2F2	H18
IO29NB2F2	K17
IO29PB2F2	J17
Bank 3	
IO30NB3F3	N18
IO30PB3F3	M18
IO31NB3F3	L18
IO31PB3F3	K18
IO32NB3F3	L16
IO32PB3F3	L17

FG324	
AX125 Function	Pin Number
IO33NB3F3	R18
IO33PB3F3	P18
IO34NB3F3	N15
IO34PB3F3	M15
IO35NB3F3	M16
IO35PB3F3	M17
IO36NB3F3	P16
IO36PB3F3	N16
IO37NB3F3	R17
IO37PB3F3	P17
IO38NB3F3	N14
IO38PB3F3	M14
IO39NB3F3	U18
IO39PB3F3	T18
IO40NB3F3	R16
IO40PB3F3	T17
IO41NB3F3	P13
IO41PB3F3	P14
Bank 4	
IO42NB4F4	T13
IO42PB4F4	T14
IO43NB4F4	U15
IO43PB4F4	T15
IO44NB4F4	U13
IO44PB4F4	U14
IO45NB4F4	V15
IO45PB4F4	V16
IO46NB4F4	V13
IO46PB4F4	V14
IO47NB4F4	V12
IO47PB4F4	U12
IO48NB4F4	V10
IO48PB4F4	V11
IO49NB4F4/CLKEN	T10
IO49PB4F4/CLKEP	T11

FG484	
AX500 Function	**Pin Number**
IO108PB5F10	AA10
IO110NB5F10	AB9
IO110PB5F10	AB10
IO111NB5F10	Y8
IO111PB5F10	Y9
IO112NB5F10	AB7
IO113NB5F10	W8
IO113PB5F10	W9
IO114NB5F11	AA7
IO114PB5F11	AA8
IO115NB5F11	AB5
IO115PB5F11	AB6
IO116NB5F11	Y6
IO116PB5F11	Y7
IO117NB5F11	U8
IO117PB5F11	U9
IO118NB5F11	AA5
IO118PB5F11	AA6
IO119NB5F11	AA4
IO119PB5F11	AB4
IO120NB5F11	Y4
IO120PB5F11	Y5
IO121NB5F11	W6
IO121PB5F11	W7
IO122NB5F11	V3
IO122PB5F11	W3
IO123NB5F11	T7
IO123PB5F11	T8
IO124NB5F11	V4
IO124PB5F11	W5
IO125NB5F11	V6
IO125PB5F11	V7
Bank 6	
IO126NB6F12	V2
IO126PB6F12	W2

FG484	
AX500 Function	**Pin Number**
IO127NB6F12	P7
IO127PB6F12	R7
IO128NB6F12	V1
IO128PB6F12	W1
IO129NB6F12	U5
IO129PB6F12	T5
IO130NB6F12	T1
IO130PB6F12	U1
IO131NB6F12	P6
IO131PB6F12	R6
IO132NB6F12	T4
IO132PB6F12	U4
IO133NB6F12	U2
IO134NB6F12	T3
IO134PB6F12	U3
IO135NB6F12	P5
IO135PB6F12	R5
IO136NB6F13	R2
IO136PB6F13	T2
IO138NB6F13	P4
IO138PB6F13	R4
IO139NB6F13	N2
IO139PB6F13	P2
IO140NB6F13	P3
IO140PB6F13	R3
IO141NB6F13	M6
IO141PB6F13	N6
IO142NB6F13	P1
IO142PB6F13	R1
IO143NB6F13	M5
IO143PB6F13	N5
IO144NB6F13	M4
IO144PB6F13	N4
IO145NB6F13	M7
IO145PB6F13	N7

FG484	
AX500 Function	**Pin Number**
IO146NB6F13	M3
IO146PB6F13	N3
Bank 7	
IO147NB7F14	K7
IO147PB7F14	L7
IO148NB7F14	M2
IO148PB7F14	N1
IO149NB7F14	K5
IO149PB7F14	L5
IO150NB7F14	L3
IO150PB7F14	L2
IO151NB7F14	K6
IO151PB7F14	L6
IO152NB7F14	K2
IO152PB7F14	K1
IO153NB7F14	K4
IO153PB7F14	K3
IO154NB7F14	H3
IO154PB7F14	J3
IO155NB7F14	H5
IO155PB7F14	J5
IO156NB7F14	H4
IO156PB7F14	J4
IO157NB7F14	H2
IO157PB7F14	J2
IO158NB7F15	H1
IO158PB7F15	J1
IO159NB7F15	F1
IO159PB7F15	G1
IO160NB7F15	F2
IO160PB7F15	G2
IO161NB7F15	H6
IO161PB7F15	J6
IO162NB7F15	F3
IO162PB7F15	G3

FG676	
AX500 Function	**Pin Number**
GND	R10
GND	R11
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	T10
GND	T11
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	U10
GND	U11
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	V18
GND	V9
GND	W1
GND	W19
GND	W26
GND	W8
GND	Y20
GND	Y7
GND/LP	C2
NC	A11
NC	A21

FG676	
AX500 Function	**Pin Number**
NC	A22
NC	A24
NC	A25
NC	AA11
NC	AA19
NC	AA20
NC	AA4
NC	AA5
NC	AA6
NC	AA7
NC	AA8
NC	AA9
NC	AB1
NC	AB11
NC	AB17
NC	AB18
NC	AB19
NC	AB20
NC	AB8
NC	AB9
NC	AC1
NC	AC13
NC	AC14
NC	AC25
NC	AD1
NC	AD11
NC	AD16
NC	AD25
NC	AE1
NC	AF2
NC	AF25
NC	B11
NC	B24
NC	B4
NC	C16

FG676	
AX500 Function	**Pin Number**
NC	C4
NC	D1
NC	D13
NC	D14
NC	D17
NC	D18
NC	D2
NC	D26
NC	D3
NC	D9
NC	E1
NC	E18
NC	E23
NC	E24
NC	E26
NC	E3
NC	E4
NC	E9
NC	F1
NC	F18
NC	F20
NC	F21
NC	F22
NC	F23
NC	F24
NC	F4
NC	F6
NC	F7
NC	G21
NC	G22
NC	H21
NC	H22
NC	H23
NC	H5
NC	H6

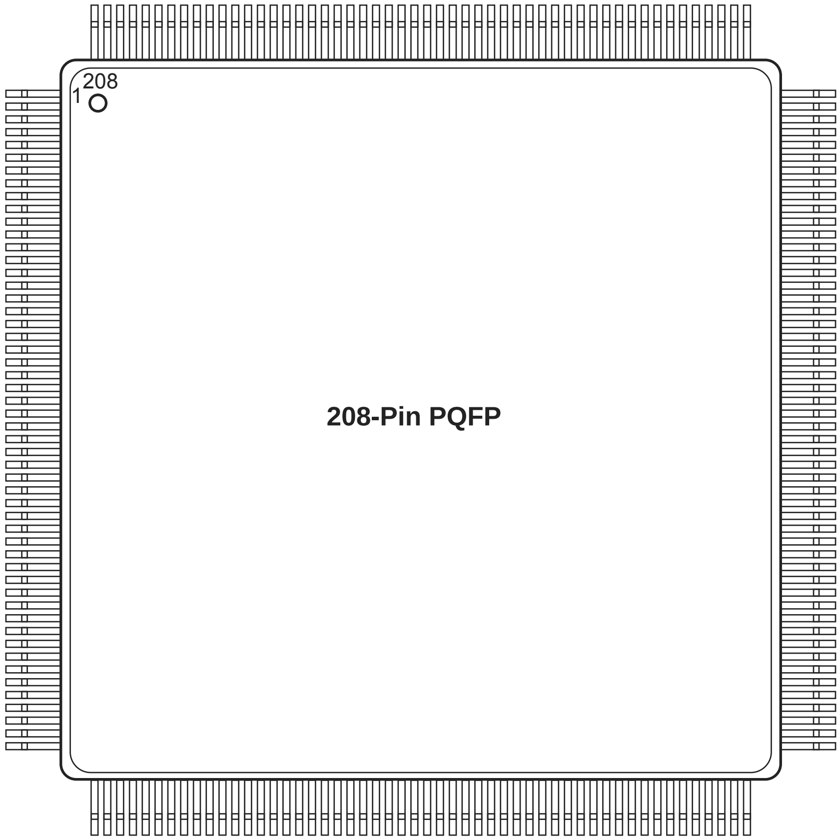
FG1152	
AX2000 Function	Pin Number
IO259NB6F24	AF7
IO259PB6F24	AG7
IO260NB6F24	AH3
IO260PB6F24	AH4
IO261NB6F24	AH5
IO261PB6F24	AJ5
IO262NB6F24	AE6
IO262PB6F24	AF6
IO263NB6F24	AF5
IO263PB6F24	AG5
IO264NB6F24	AD8
IO264PB6F24	AE8
IO265NB6F24	AF3
IO265PB6F24	AG3
IO266NB6F24	AC10
IO266PB6F24	AD10
IO267NB6F25	AD7
IO267PB6F25	AE7
IO268NB6F25	AD5
IO268PB6F25	AE5
IO269NB6F25	AE4
IO269PB6F25	AF4
IO270NB6F25	AB9
IO270PB6F25	AC9
IO271NB6F25	AC6
IO271PB6F25	AD6
IO272NB6F25	AB8
IO272PB6F25	AC8
IO273NB6F25	AE1
IO273PB6F25	AE2
IO274NB6F25	AA10
IO274PB6F25	AB10
IO275NB6F25	AB7
IO275PB6F25	AC7
IO276NB6F25	AD1

FG1152	
AX2000 Function	Pin Number
IO276PB6F25	AD2
IO277NB6F25	AC4
IO277PB6F25	AC3
IO278NB6F26	AA8
IO278PB6F26	AA9
IO279NB6F26	AB5
IO279PB6F26	AB6
IO280NB6F26	Y10
IO280PB6F26	Y11
IO281NB6F26	AB3
IO281PB6F26	AB4
IO282NB6F26	Y7
IO282PB6F26	AA7
IO283NB6F26	AC2
IO283PB6F26	AC1
IO284NB6F26	Y9
IO284PB6F26	Y8
IO285NB6F26	AA5
IO285PB6F26	AA6
IO286NB6F26	W10
IO286PB6F26	W11
IO287NB6F26	AA3
IO287PB6F26	AA4
IO288NB6F26	W9
IO288PB6F26	W8
IO289NB6F27	AA1
IO289PB6F27	AA2
IO290NB6F27	W6
IO290PB6F27	Y6
IO291NB6F27	W5
IO291PB6F27	Y5
IO292NB6F27	V7
IO292PB6F27	W7
IO293NB6F27	W4
IO293PB6F27	Y4

FG1152	
AX2000 Function	Pin Number
IO294NB6F27	V10
IO294PB6F27	V11
IO295NB6F27	Y1
IO295PB6F27	Y2
IO296NB6F27	W1
IO296PB6F27	W2
IO297NB6F27	V1
IO297PB6F27	V2
IO298NB6F27	V9
IO298PB6F27	V8
IO299NB6F27	U4
IO299PB6F27	V4
Bank 7	
IO300NB7F28	U10
IO300PB7F28	U11
IO301NB7F28	U2
IO301PB7F28	U1
IO302NB7F28	U6
IO302PB7F28	U7
IO303NB7F28	T3
IO303PB7F28	U3
IO304NB7F28	U9
IO304PB7F28	U8
IO305NB7F28	R2
IO305PB7F28	R1
IO306NB7F28	R4
IO306PB7F28	T4
IO307NB7F28	R5
IO307PB7F28	T5
IO308NB7F28	T11
IO308PB7F28	T10
IO309NB7F28	T6
IO309PB7F28	T7
IO310NB7F29	T9
IO310PB7F29	T8

FG1152	
AX2000 Function	**Pin Number**
VCOMPLD	K18
VCOMPLE	AH19
VCOMPLF	AF18
VCOMPLG	AH16
VCOMPLH	AD17
VPUMP	J26

PQ208



Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.microsemi.com/soc/products/rescenter/package/index.html.

CQ352	
AX250 Function	Pin Number
GND	21
GND	27
GND	33
GND	39
GND	45
GND	51
GND	57
GND	63
GND	69
GND	75
GND	81
GND	88
GND	89
GND	97
GND	103
GND	109
GND	115
GND	121
GND	133
GND	145
GND	151
GND	157
GND	163
GND	169
GND	176
GND	177
GND	186
GND	192
GND	198
GND	204
GND	210
GND	216
GND	222
GND	228
GND	234
GND	240
GND	246
GND	252
GND	258
GND	264
GND	265
GND	274
GND	280
GND	286
GND	292
GND	298
GND	310
GND	322
GND	330
GND	334
GND	340
GND	345
GND	352
NC	91
NC	117
NC	130
NC	131
NC	148
NC	174
NC	268
NC	294
NC	307
NC	308
NC	327
NC	328
PRA	312
PRB	311
PRC	135
PRD	134
TCK	349
TDI	348
TDO	347
TMS	350
TRST	351
VCCA	3
VCCA	14
VCCA	32
VCCA	56
VCCA	74
VCCA	87
VCCA	102
VCCA	114
VCCA	150
VCCA	162
VCCA	175
VCCA	191
VCCA	209
VCCA	233
VCCA	251
VCCA	263
VCCA	279
VCCA	291
VCCA	329
VCCA	339
VCCDA	2
VCCDA	44
VCCDA	90
VCCDA	116
VCCDA	132
VCCDA	149
VCCDA	178
VCCDA	221
VCCDA	266
VCCDA	293
VCCDA	309

CQ352	
AX500 Function	**Pin Number**
IO87PB4F8	171
IO89NB4F8	166
IO89PB4F8	167
IO94NB4F9	164
IO94PB4F9	165
IO95NB4F9	160
IO95PB4F9	161
IO97NB4F9	158
IO97PB4F9	159
IO99NB4F9	154
IO99PB4F9	155
IO100NB4F9	146
IO100PB4F9	147
IO101NB4F9	152
IO101PB4F9	153
IO103NB4F9/CLKEN	142
IO103PB4F9/CLKEP	143
IO104NB4F9/CLKFN	136
IO104PB4F9/CLKFP	137
Bank 5	
IO105NB5F10/CLKGN	128
IO105PB5F10/CLKGP	129
IO106NB5F10/CLKHN	122
IO106PB5F10/CLKHP	123
IO107NB5F10	118
IO107PB5F10	119
IO114NB5F11	112
IO114PB5F11	113
IO115NB5F11	110
IO115PB5F11	111
IO116NB5F11	106
IO116PB5F11	107
IO117NB5F11	104
IO117PB5F11	105
IO119NB5F11	100

CQ352	
AX500 Function	**Pin Number**
IO119PB5F11	101
IO121NB5F11	98
IO121PB5F11	99
IO123NB5F11	94
IO123PB5F11	95
IO125NB5F11	92
IO125PB5F11	93
Bank 6	
IO126PB6F12	86
IO127NB6F12	84
IO127PB6F12	85
IO129NB6F12	82
IO129PB6F12	83
IO131NB6F12	78
IO131PB6F12	79
IO133NB6F12	76
IO133PB6F12	77
IO134NB6F12	72
IO134PB6F12	73
IO135NB6F12	70
IO135PB6F12	71
IO137NB6F13	66
IO137PB6F13	67
IO138NB6F13	64
IO138PB6F13	65
IO139NB6F13	60
IO139PB6F13	61
IO141NB6F13	54
IO141PB6F13	55
IO142NB6F13	58
IO142PB6F13	59
IO143NB6F13	52
IO143PB6F13	53
IO145NB6F13	48
IO145PB6F13	49

CQ352	
AX500 Function	**Pin Number**
IO146NB6F13	46
IO146PB6F13	47
Bank 7	
IO147NB7F14	40
IO147PB7F14	41
IO148NB7F14	42
IO148PB7F14	43
IO149NB7F14	36
IO149PB7F14	37
IO151NB7F14	30
IO151PB7F14	31
IO152NB7F14	34
IO152PB7F14	35
IO153NB7F14	28
IO153PB7F14	29
IO155NB7F14	24
IO155PB7F14	25
IO157NB7F14	22
IO157PB7F14	23
IO159NB7F15	16
IO159PB7F15	17
IO160NB7F15	18
IO160PB7F15	19
IO161NB7F15	12
IO161PB7F15	13
IO163NB7F15	10
IO163PB7F15	11
IO165NB7F15	6
IO165PB7F15	7
IO167NB7F15	4
IO167PB7F15	5
Dedicated I/O	
GND	1
GND	9
GND	15

CQ352	
AX1000 Function	Pin Number
Bank 0	
IO02NB0F0	341
IO02PB0F0	342
IO03PB0F0	343
IO04NB0F0	337
IO04PB0F0	338
IO08NB0F0	331
IO08PB0F0	332
IO09NB0F0	335
IO09PB0F0	336
IO24NB0F2	325
IO24PB0F2	326
IO25NB0F2	323
IO25PB0F2	324
IO30NB0F2/HCLKAN	319
IO30PB0F2/HCLKAP	320
IO31NB0F2/HCLKBN	313
IO31PB0F2/HCLKBP	314
Bank 1	
IO32NB1F3/HCLKCN	305
IO32PB1F3/HCLKCP	306
IO33NB1F3/HCLKDN	299
IO33PB1F3/HCLKDP	300
IO38NB1F3	295
IO38PB1F3	296
IO54NB1F5	287
IO54PB1F5	288
IO55NB1F5	289
IO55PB1F5	290
IO56NB1F5	281
IO56PB1F5	282
IO57NB1F5	283
IO57PB1F5	284
IO59NB1F5	277
IO59PB1F5	278

CQ352	
AX1000 Function	Pin Number
IO60NB1F5	275
IO60PB1F5	276
IO61NB1F5	271
IO61PB1F5	272
IO63NB1F5	269
IO63PB1F5	270
Bank 2	
IO64NB2F6	259
IO64PB2F6	260
IO67NB2F6	261
IO67PB2F6	262
IO68NB2F6	255
IO68PB2F6	256
IO69NB2F6	253
IO69PB2F6	254
IO74NB2F7	249
IO74PB2F7	250
IO75NB2F7	247
IO75PB2F7	248
IO76NB2F7	243
IO76PB2F7	244
IO77NB2F7	241
IO77PB2F7	242
IO78NB2F7	237
IO78PB2F7	238
IO79NB2F7	235
IO79PB2F7	236
IO82NB2F7	231
IO82PB2F7	232
IO83NB2F7	229
IO83PB2F7	230
IO94NB2F8	225
IO94PB2F8	226
IO95NB2F8	223
IO95PB2F8	224

CQ352	
AX1000 Function	Pin Number
Bank 3	
IO96NB3F9	217
IO96PB3F9	218
IO97NB3F9	219
IO97PB3F9	220
IO99NB3F9	213
IO99PB3F9	214
IO108NB3F10	211
IO108PB3F10	212
IO109NB3F10	207
IO109PB3F10	208
IO111NB3F10	205
IO111PB3F10	206
IO112NB3F10	199
IO112PB3F10	200
IO113NB3F10	201
IO113PB3F10	202
IO115NB3F10	195
IO115PB3F10	196
IO116NB3F10	193
IO116PB3F10	194
IO117NB3F10	189
IO117PB3F10	190
IO124NB3F11	183
IO124PB3F11	184
IO125NB3F11	187
IO125PB3F11	188
IO127NB3F11	181
IO127PB3F11	182
IO128NB3F11	179
IO128PB3F11	180
Bank 4	
IO130NB4F12	172
IO130PB4F12	173
IO131NB4F12	170

CQ352	
AX1000 Function	**Pin Number**
IO131PB4F12	171
IO132NB4F12	166
IO132PB4F12	167
IO133NB4F12	164
IO133PB4F12	165
IO134NB4F12	160
IO134PB4F12	161
IO136NB4F12	158
IO136PB4F12	159
IO137NB4F12	154
IO137PB4F12	155
IO138NB4F12	152
IO138PB4F12	153
IO153NB4F14	146
IO153PB4F14	147
IO159NB4F14/CLKEN	142
IO159PB4F14/CLKEP	143
IO160NB4F14/CLKFN	136
IO160PB4F14/CLKFP	137
Bank 5	
IO161NB5F15/CLKGN	128
IO161PB5F15/CLKGP	129
IO162NB5F15/CLKHN	122
IO162PB5F15/CLKHP	123
IO167NB5F15	118
IO167PB5F15	119
IO183NB5F17	110
IO183PB5F17	111
IO184NB5F17	112
IO184PB5F17	113
IO185NB5F17	104
IO185PB5F17	105
IO186NB5F17	106
IO186PB5F17	107
IO187NB5F17	98

CQ352	
AX1000 Function	**Pin Number**
IO187PB5F17	99
IO188NB5F17	100
IO188PB5F17	101
IO190NB5F17	94
IO190PB5F17	95
IO192NB5F17	92
IO192PB5F17	93
Bank 6	
IO193PB6F18	86
IO194NB6F18	84
IO194PB6F18	85
IO196NB6F18	78
IO196PB6F18	79
IO197NB6F18	82
IO197PB6F18	83
IO198NB6F18	76
IO198PB6F18	77
IO203NB6F19	72
IO203PB6F19	73
IO204NB6F19	70
IO204PB6F19	71
IO205NB6F19	66
IO205PB6F19	67
IO206NB6F19	64
IO206PB6F19	65
IO207NB6F19	60
IO207PB6F19	61
IO208NB6F19	58
IO208PB6F19	59
IO211NB6F19	54
IO211PB6F19	55
IO212NB6F19	52
IO212PB6F19	53
IO223NB6F20	48
IO223PB6F20	49

CQ352	
AX1000 Function	**Pin Number**
IO224NB6F20	46
IO224PB6F20	47
Bank 7	
IO225NB7F21	40
IO225PB7F21	41
IO226NB7F21	42
IO226PB7F21	43
IO237NB7F22	34
IO237PB7F22	35
IO238NB7F22	36
IO238PB7F22	37
IO240NB7F22	30
IO240PB7F22	31
IO241NB7F22	28
IO241PB7F22	29
IO242NB7F22	24
IO242PB7F22	25
IO244NB7F22	22
IO244PB7F22	23
IO245NB7F22	18
IO245PB7F22	19
IO246NB7F22	16
IO246PB7F22	17
IO249NB7F23	12
IO249PB7F23	13
IO250NB7F23	10
IO250PB7F23	11
IO256NB7F23	4
IO256PB7F23	5
IO257NB7F23	6
IO257PB7F23	7
Dedicated I/O	
GND	1
GND	9
GND	15

CQ352	
AX1000 Function	Pin Number
GND	21
GND	27
GND	33
GND	39
GND	45
GND	51
GND	57
GND	63
GND	69
GND	75
GND	81
GND	88
GND	89
GND	97
GND	103
GND	109
GND	115
GND	121
GND	133
GND	145
GND	151
GND	157
GND	163
GND	169
GND	176
GND	177
GND	186
GND	192
GND	198
GND	204
GND	210
GND	216
GND	222
GND	228
GND	234

CQ352	
AX1000 Function	Pin Number
GND	240
GND	246
GND	252
GND	258
GND	264
GND	265
GND	274
GND	280
GND	286
GND	292
GND	298
GND	310
GND	322
GND	330
GND	334
GND	340
GND	345
GND	352
NC	91
NC	130
NC	131
NC	174
NC	268
NC	307
NC	308
PRA	312
PRB	311
PRC	135
PRD	134
TCK	349
TDI	348
TDO	347
TMS	350
TRST	351
VCCA	3

CQ352	
AX1000 Function	Pin Number
VCCA	14
VCCA	32
VCCA	56
VCCA	74
VCCA	87
VCCA	102
VCCA	114
VCCA	150
VCCA	162
VCCA	175
VCCA	191
VCCA	209
VCCA	233
VCCA	251
VCCA	263
VCCA	279
VCCA	291
VCCA	329
VCCA	339
VCCDA	2
VCCDA	44
VCCDA	90
VCCDA	116
VCCDA	117
VCCDA	132
VCCDA	148
VCCDA	149
VCCDA	178
VCCDA	221
VCCDA	266
VCCDA	293
VCCDA	294
VCCDA	309
VCCDA	327
VCCDA	328

4 – Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Revision	Changes	Page
Revision 18 (March 2012)	Table 2-1 • Absolute Maximum Ratings was updated to correct the maximum DC core supply voltage (VCCA) from 1.6 V to 1.7 V (SAR 36786). The maximum input voltage (VI) was corrected from 3.75 V to 4.1 V (SAR 35419).	2-1
	Values for tristate leakage current IOZ, and IIH and IIL were added to Table 2-3 • Standby Current (SARs 35774, 32021).	2-2
	Figure 2-2 • VCCPLX and VCOMPLX Power Supply Connect was updated to correct the units for the resistance from "W" to Ω (SAR 36415).	2-9
	In the Introduction to the "User I/Os" section, the following sentence was added to clarify the slew rate setting (SAR 34943): The slew rate setting is effective for both rising and falling edges.	2-11
	Figure 2-3 • Use of an External Resistor for 5 V Tolerance was revised to show the VCCI and GND clamp diodes. The explanatory text above the figure was revised as well (SAR 34942).	2-13
	EQ 3 for 5 V tolerance was corrected to change Vdiode from 0.6 V to 0.7 V (SAR 36786).	2-13
	Additional information was added to the "Using the Weak Pull-Up and Pull-Down Circuits" section to clarify how the weak pull-up and pull-down resistors are physically implemented (SAR 34945).	2-17
	The description for the C_{INCLK} parameter in Table 2-18 • Input Capacitance was changed from "Input capacitance on clock pin" to "Input capacitance on HCLK and RCLK pin" (SAR 34944).	2-21
	Table 2-19 • I/O Input Rise Time and Fall Time* is new (SAR 34942).	2-21
	The minimum VIL for 1.5 V LVCMOS and PCI was corrected from –0.5 to –0.3 in Table 2-29 • DC Input and Output Levels and Table 2-33 • DC Input and Output Levels (SAR 34358).	2-38, 2-40
	Support for simulating the GCLR/ GPSET feature in the Axcelerator Family was added in Libero software v9.0 SPI1. Reference to the section explaining this in the *Antifuse Macro Library Guide* was added to the "R-Cell" section (SAR 26413).	2-58
	The enable signal in Figure 2-32 • R-Cell Delays was corrected to show it is active low rather than active high (SAR 34946).	2-59
Revision 17 (September 2011)	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "Axcelerator Family Device Status" table indicates the status for each device in the device family.	iii
	The "Features" section, "Programmable Interconnect Element" section, and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 32865).	i, 1-1, 2-108