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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	8064
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	115
Number of Gates	500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax500-pqg208i

Packaging Data

Refer to the following documents located on the Microsemi SoC Products Group website for additional packaging information.

- Package Mechanical Drawings

- Package Thermal Characteristics and Weights

- Hermetic Package Mechanical Information

Contact your local Microsemi representative for device availability.

User I/Os²

Introduction

The Axcelerator family features a flexible I/O structure, supporting a range of mixed voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V) with its bank-selectable I/Os. Table 2-8 on page 2-12 contains the I/O standards supported by the Axcelerator family, and Table 2-10 on page 2-12 compares the features of the different I/O standards.

Each I/O provides programmable slew rates, drive strengths, and weak pull-up and weak pull-down circuits. The slew rate setting is effective for both rising and falling edges.

I/O standards, except 3.3 V PCI and 3.3 V PCI-X, are capable of hot insertion. 3.3 V PCI and 3.3 V PCI-X are 5 V tolerant with the aid of an external resistor.

The input buffer has an optional user-configurable delay element. The element can reduce or eliminate the hold time requirement for input signals registered within the I/O cell. The value for the delay is set on a bank-wide basis. Note that the delay WILL be a function of process variations as well as temperature and voltage changes.

Each I/O includes three registers: an input (InReg), an output (OutReg), and an enable register (EnReg). I/Os are organized into banks, and there are eight banks per device—two per side (Figure 2-6 on page 2-18). Each I/O bank has a common VCCI, the supply voltage for its I/Os.

For voltage-referenced I/Os, each bank also has a common reference-voltage bus, VREF. While VREF must have a common voltage for an entire I/O bank, its location is user-selectable. In other words, any user I/O in the bank can be selected to be a VREF.

The location of the VREF pin should be selected according to the following rules:

- Any pin that is assigned as a VREF can control a maximum of eight user I/O pad locations in each direction (16 total maximum) within the same I/O bank.
- I/O pad locations listed as no connects are counted as part of the 16 maximum. In many cases, this leads to fewer than eight user I/O package pins in each direction being controlled by a VREF pin.
- Dedicated I/O pins such as GND and VCCI are counted as part of the 16.
- The two user I/O pads immediately adjacent on each side of the VREF pin (four in total) may only be used as inputs. The exception is when there is a VCCI/GND pair separating the VREF pin and the user I/O pad location.
- The user does not need to assign VREF pins for OUTBUF and TRIBUF. VREF pins are needed only for input and bidirectional I/Os.

The differential amplifier supply voltage VCCDA should be connected to 3.3 V.

A user can gain access to the various I/O standards in three ways:

- Instantiate specific library macros that represent the desired specific standard.
- Use generic I/O macros and then use Designer's PinEditor to specify the desired I/O standards (please note that this is not applicable to differential standards).
- A combination of the first two methods.

Refer to the *I/O Features in Axcelerator Family Devices* application note and the *Antifuse Macro Library Guide* for more details.

2. Do not use an external resistor to pull the I/O above V_{CCI} for a higher logic "1" voltage level. The desired higher logic "1" voltage level will be degraded due to a small I/O current, which exists when the I/O is pulled up above V_{CCI} .

Using the Weak Pull-Up and Pull-Down Circuits

Each Axcelerator I/O comes with a weak pull-up/down circuit (on the order of 10 k Ω). These are weak transistors with the gates tied on, so the on resistance of the transistor emulates a resistor. The weak pull-up and pull-down is active only when the device is powered up, and they must be biased to be on. When the rails are coming up, they are not biased fully, so they do not behave as resistors until the voltage is at sufficient levels to bias the transistors. The key is they really are transistors; they are not traces of poly silicon, which is another way to do an on-chip resistor (those take much more room). I/O macros are provided for combinations of pull up/down for LVTTL, LVCMOS (2.5 V, 1.8 V, and 1.5 V) standards. These macros can be instantiated if a keeper circuit for any input buffer is required.

Customizing the I/O

- A five-bit programmable input delay element is associated with each I/O. The value of this delay is set on a bank-wide basis (Table 2-14). It is optional for each input buffer within the bank (i.e. the user can enable or disable the delay element for the I/O). When the input buffer drives a register within the I/O, the delay element is activated by default to ensure a zero hold-time. The default setting for this property can be set in Designer. When the input buffer does not drive a register, the delay element is deactivated to provide higher performance. Again, this can be overridden by changing the default setting for this property in Designer.
- The slew-rate value for the LVTTL output buffer can be programmed and can be set to either slow or fast.
- The drive strength value for LVTTL output buffers can be programmed as well. There are four different drive strength values – 8 mA, 12 mA, 16 mA, or 24 mA – that can be specified in Designer.⁵

Table 2-14 • Bank-Wide Delay Values

Bits Setting	Delay (ns)	Bits Setting	Delay (ns)
0	0.54	16	2.01
1	0.65	17	2.13
2	0.71	18	2.19
3	0.83	19	2.3
4	0.9	20	2.38
5	1.01	21	2.49
6	1.08	22	2.55
7	1.19	23	2.67
8	1.27	24	2.75
9	1.39	25	2.87
10	1.45	26	2.93
11	1.56	27	3.04
12	1.64	28	3.12
13	1.75	29	3.23
14	1.81	30	3.29
15	1.93	31	3.41

Note: Delay values are approximate and will vary with process, temperature, and voltage.

5. These values are minimum drive strengths.

3.3 V LVTTTL

Low-Voltage Transistor-Transistor Logic is a general purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTTL input buffer and push-pull output buffer.

Table 2-20 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
−0.3	0.8	2.0	3.6	0.4	2.4	24	−24

AC Loadings

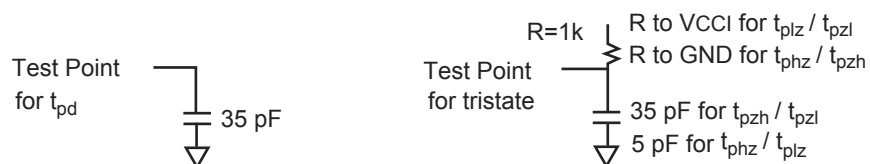


Figure 2-15 • AC Test Loads

Table 2-21 • AC Waveforms, Measuring Points, and Capacitive Load

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
0	3.0	1.40	N/A	35

Note: * Measuring Point = VTRIP

Table 2-22 • 3.3 V LVTTTL I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVTTTL Output Drive Strength = 2 (12 mA) / Low Slew Rate								
t _{DP}	Input Buffer		1.68		1.92		2.26	ns
t _{PY}	Output Buffer		12.14		13.83		16.26	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		12.43		14.16		16.65	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		12.17		13.86		16.30	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.73		1.74		1.75	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.22		2.23		2.24	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.38		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

1.5 V LVCMOS (JESD8-11)

Low-Voltage Complementary Metal-Oxide Semiconductor for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 3.3 V tolerant CMOS input buffer and a push-pull output buffer.

Table 2-29 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
-0.3	0.35 VCCI	0.65 VCCI	3.6	0.4	VCCI - 0.4	8 mA	-8 mA

AC Loadings

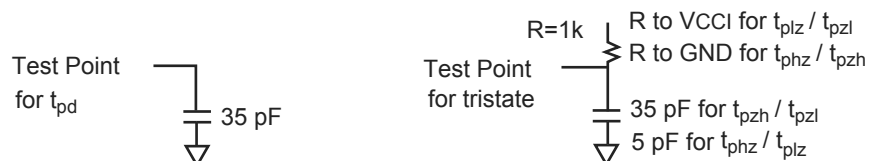


Table 2-30 • AC Test Loads

Table 2-31 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
0	1.5	0.5V _{CCI}	N/A	35

Note: * Measuring Point = VTRIP

Table 2-40 • 3.3 V GTL+ I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V GTL+I/O Module Timing								
t _{DP}	Input Buffer		1.71		1.95		2.29	ns
t _{PY}	Output Buffer		1.13		1.29		1.52	ns
t _{CLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t _{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

SSTL3

Stub Series Terminated Logic for 3.3 V is a general-purpose 3.3 V memory bus standard (JESD8-8). The Axcelerator devices support both classes of this standard. This requires a differential amplifier input buffer and a push-pull output buffer.

Class I

Table 2-50 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
-0.3	VREF – 0.2	VREF + 0.2	3.6	VREF – 0.6	VREF + 0.6	8	–8

AC Loadings

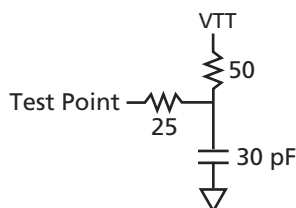


Figure 2-23 • AC Test Loads

Table 2-51 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
VREF – 1.0	VREF + 1.0	VREF	1.50	30

Note: *Measuring Point = VTRIP

Timing Characteristics

Table 2-52 • 3.3 V SSTL3 Class I I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
3.3 V SSTL3 Class I I/O Module Timing								
t _{DP}	Input Buffer		1.78		2.03		2.39	ns
t _{PY}	Output Buffer		2.17		2.47		2.91	ns
t _{ICKLQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t _{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Table 2-69 • AX2000 Predicted Routing Delays
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

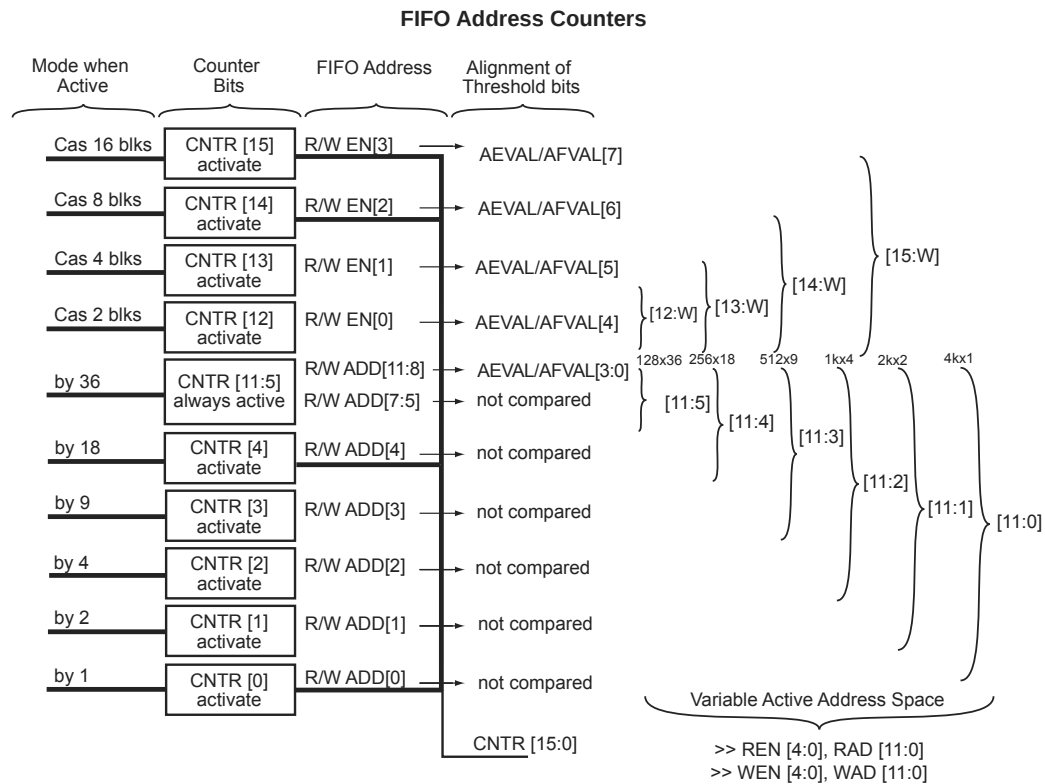
		-2 Speed	-1 Speed	Std Speed	
Parameter	Description	Typical	Typical	Typical	Units
Predicted Routing Delays					
t _{DC}	DirectConnect Routing Delay, FO1	0.12	0.13	0.15	ns
t _{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t _{RD1}	Routing delay for FO1	0.50	0.56	0.66	ns
t _{RD2}	Routing delay for FO2	0.59	0.67	0.79	ns
t _{RD3}	Routing delay for FO3	0.70	0.80	0.94	ns
t _{RD4}	Routing delay for FO4	0.76	0.87	1.02	ns
t _{RD5}	Routing delay for FO5	0.98	1.11	1.31	ns
t _{RD6}	Routing delay for FO6	1.48	1.68	1.97	ns
t _{RD7}	Routing delay for FO7	1.65	1.87	2.20	ns
t _{RD8}	Routing delay for FO8	1.73	1.96	2.31	ns
t _{RD16}	Routing delay for FO16	2.58	2.92	3.44	ns
t _{RD32}	Routing delay for FO32	4.24	4.81	5.65	ns

FIFO Flag Logic

The FIFO is user configurable into various DEPTHS and WIDTHS. Figure 2-62 shows the FIFO address counter details.

- Bits 11 to 5 are active for all modes.
- As the data word size is reduced, more least-significant bits are added to the address.
- As the number of cascaded blocks increases, the number of significant bits in the address increases.

For example, if four blocks are cascaded as a 1kx16 FIFO with each block having a 1kx4 aspect ratio, bits 11 to 2 of the address will be used to specify locations within each RAM block, whereas bits 13 and 12 will be used to specify the RAM block.



Note: Inactive counter bits are set to zero.

Figure 2-62 • FIFO Address Counters

The AFULL and AEMPTY flag threshold values are programmable. The threshold values are AFVAL and AEVAL, respectively. Although the trigger threshold for each flag is defined with eight bits, the effective number of threshold bits in the comparison depends on the configuration. The effective number of threshold bits corresponds to the range of active bits in the FIFO address space (Table 2-94).

Table 2-94 • FIFO Flag Logic

Mode	Inactive AEVAL/AFVAL Bits	Inactive DIFF Bits (set to 0)	DIFF Comparison to AFVAL/AEVAL
Non-cascade	[7:4]	[15:12]	DIFF[11:8] with AE/FVAL[3:0]
Cascade 2 blocks	[7:5]	[15:13]	DIFF[12:8] with AE/FVAL[4:0]
Cascade 4 blocks	[7:6]	[15:14]	DIFF[13:8] with AE/FVAL[5:0]
Cascade 8 blocks	[7]	[15]	DIFF[14:8] with AE/FVAL[6:0]
Cascade 16 blocks	None	None	DIFF[15:8] with AE/FVAL[7:0]

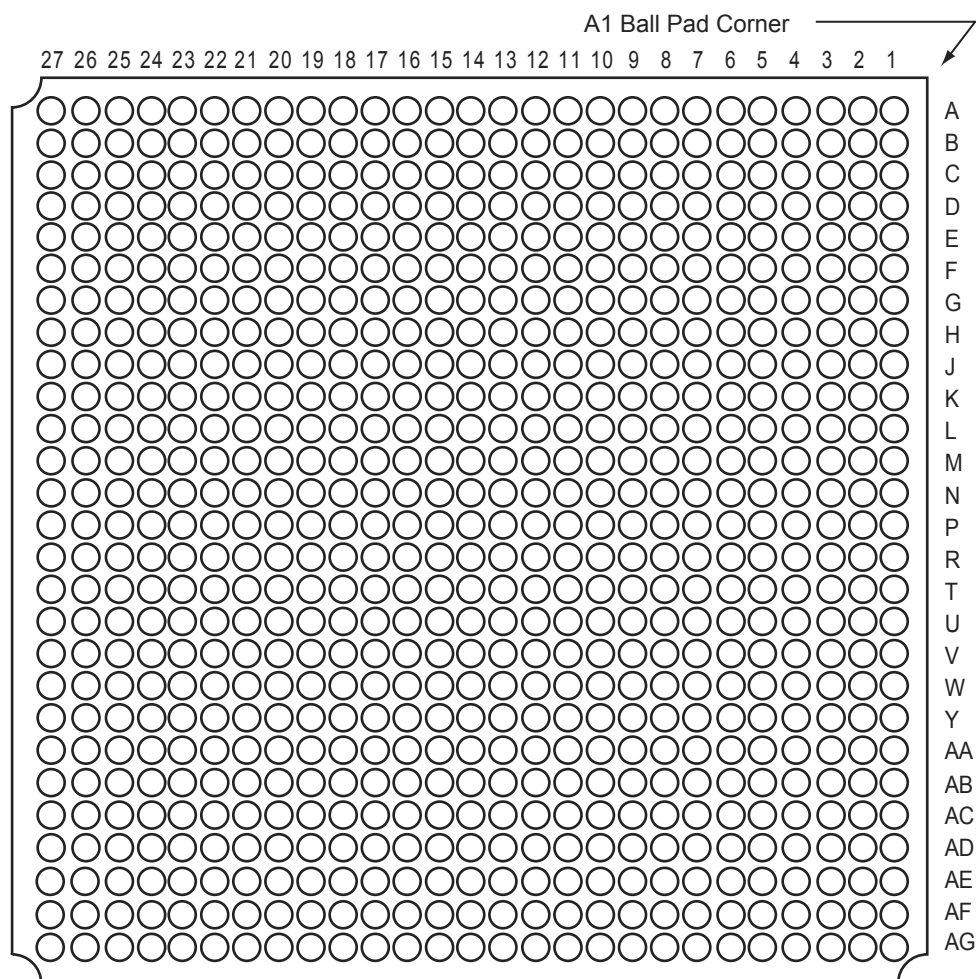
Table 2-100 • Four FIFO Blocks Cascaded
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
FIFO Module Timing								
t _{WSU}	Write Setup		14.60		16.63		19.55	ns
t _{WHD}	Write Hold		0.00		0.00		0.00	ns
t _{WCKH}	WCLK High		0.75		0.75		0.75	ns
t _{WCKL}	WCLK Low		2.51		2.51		2.51	ns
t _{WCKP}	Minimum WCLK Period	3.26		3.26		3.26		ns
t _{RSU}	Read Setup		15.27		17.39		20.44	ns
t _{RHD}	Read Hold		0.00		0.00		0.00	ns
t _{RCKH}	RCLK High		0.73		0.73		0.73	ns
t _{RCKL}	RCLK Low		2.96		2.96		2.96	ns
t _{RCKP}	Minimum RCLK period	3.69		3.69		3.69		ns
t _{CLRHF}	Clear High		0.00		0.00		0.00	ns
t _{CLR2FF}	Clear-to-flag (EMPTY/FULL)		1.92		2.18		2.57	ns
t _{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)		4.39		5.00		5.88	ns
t _{CK2FF}	Clock-to-flag (EMPTY/FULL)		2.13		2.42		2.85	ns
t _{CK2AF}	Clock-to-flag (AEMPTY/AFULL)		5.04		5.75		6.75	ns
t _{RCK2RD1}	RCLK-To-OUT (Pipelined)		2.36		2.69		3.16	ns
t _{RCK2RD2}	RCLK-To-OUT (Nonpipelined)		2.83		3.23		3.79	ns

Note: Timing data for these four cascaded FIFO blocks uses a depth of 16,384. For all other combinations, use Microsemi's timing software.

3 – Package Pin Assignments

BG729



Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

FG484		FG484		FG484	
AX250 Function	Pin Number	AX250 Function	Pin Number	AX250 Function	Pin Number
IO52NB3F3	P18	IO69PB4F4	AA17	IO87NB5F5	Y4
IO52PB3F3	P19	IO70NB4F4	AB14	IO87PB5F5	Y5
IO53NB3F3	R20	IO70PB4F4	AB15	IO88NB5F5	V6
IO53PB3F3	P20	IO71NB4F4	Y14	IO88PB5F5	V7
IO54NB3F3	T21	IO71PB4F4	W14	IO89NB5F5	T7
IO54PB3F3	R21	IO72NB4F4	AA14	IO89PB5F5	T8
IO55NB3F3	R17	IO72PB4F4	AA15	Bank 6	
IO55PB3F3	P17	IO73NB4F4	AA13	IO90NB6F6	V4
IO56NB3F3	U20	IO73PB4F4	AB13	IO90PB6F6	W5
IO56PB3F3	T20	IO74NB4F4/CLKEN	V12	IO91NB6F6	P7
IO57NB3F3	T18	IO74PB4F4/CLKEP	V13	IO91PB6F6	R7
IO57PB3F3	R18	IO75NB4F4/CLKFN	W11	IO92NB6F6	U5
IO58NB3F3	U19	IO75PB4F4/CLKFP	W12	IO92PB6F6	T5
IO58PB3F3	T19	Bank 5		IO93NB6F6	P6
IO59NB3F3	R16	IO76NB5F5/CLKGN	U10	IO93PB6F6	R6
IO59PB3F3	P16	IO76PB5F5/CLKGP	U11	IO94NB6F6	T4
IO60NB3F3	W20	IO77NB5F5/CLKHN	V9	IO94PB6F6	U4
IO60PB3F3	V20	IO77PB5F5/CLKHP	V10	IO95NB6F6	P5
IO61NB3F3	U18	IO78NB5F5	AA9	IO95PB6F6	R5
IO61PB3F3	V19	IO78PB5F5	AA10	IO96NB6F6	T3
Bank 4		IO79NB5F5	AB9	IO96PB6F6	U3
IO62NB4F4	T15	IO79PB5F5	AB10	IO97NB6F6	P3
IO62PB4F4	T16	IO80NB5F5	AA7	IO97PB6F6	R3
IO63NB4F4	W17	IO80PB5F5	AA8	IO98NB6F6	R2
IO63PB4F4	V17	IO81NB5F5	W8	IO98PB6F6	T2
IO64NB4F4	V15	IO81PB5F5	W9	IO99NB6F6	P4
IO64PB4F4	V16	IO82NB5F5	AB5	IO99PB6F6	R4
IO65NB4F4	Y19	IO82PB5F5	AB6	IO100NB6F6	P1
IO65PB4F4	W18	IO83NB5F5	AA5	IO100PB6F6	R1
IO66NB4F4	AB18	IO83PB5F5	AA6	IO101NB6F6	M7
IO66PB4F4	AB19	IO84NB5F5	U8	IO101PB6F6	N7
IO67NB4F4	W15	IO84PB5F5	U9	IO102NB6F6	N2
IO67PB4F4	W16	IO85NB5F5	Y6	IO102PB6F6	P2
IO68NB4F4	U14	IO85PB5F5	Y7	IO103NB6F6	M6
IO68PB4F4	U15	IO86NB5F5	W6	IO103PB6F6	N6
IO69NB4F4	AA16	IO86PB5F5	W7	IO104NB6F6	M4

FG484	
AX500 Function	Pin Number
IO163NB7F15	G5
IO163PB7F15	G6
IO164NB7F15	D1
IO164PB7F15	E1
IO165NB7F15	F4
IO165PB7F15	G4
IO166NB7F15	D2
IO166PB7F15	E2
IO167NB7F15	F5
IO167PB7F15	E4
Dedicated I/O	
VCCDA	H7
GND	A1
GND	A11
GND	A12
GND	A2
GND	A21
GND	A22
GND	AA1
GND	AA2
GND	AA21
GND	AA22
GND	AB1
GND	AB11
GND	AB12
GND	AB2
GND	AB21
GND	AB22
GND	B1
GND	B2
GND	B21
GND	B22
GND	C20
GND	C3
GND	D19

FG484	
AX500 Function	Pin Number
GND	D4
GND	E18
GND	E5
GND	G18
GND	H15
GND	H8
GND	J14
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	L1
GND	L10
GND	L11
GND	L12
GND	L13
GND	L22
GND	M1
GND	M10
GND	M11
GND	M12
GND	M13
GND	M22
GND	N10
GND	N11
GND	N12
GND	N13
GND	P14
GND	P9
GND	R15
GND	R8
GND	U16
GND	U6
GND	V18

FG484	
AX500 Function	Pin Number
GND	V5
GND	W19
GND	W4
GND	Y20
GND	Y3
GND/LP	G7
NC	AB8
NC	AB16
NC	C10
NC	C11
NC	C14
PRA	G11
PRB	F11
PRC	T12
PRD	U12
TCK	G8
TDI	F9
TDO	F7
TMS	F6
TRST	F8
VCCA	G17
VCCA	J10
VCCA	J11
VCCA	J12
VCCA	J13
VCCA	J7
VCCA	K14
VCCA	K9
VCCA	L14
VCCA	L9
VCCA	M14
VCCA	M9
VCCA	N14
VCCA	N9
VCCA	P10

FG896		FG896		FG896	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO103NB3F9	V27	IO120PB3F11	Y24	IO137PB4F12	AC21
IO103PB3F9	U27	IO121NB3F11	AB25	IO138NB4F12	AK24
IO104NB3F9	W29	IO121PB3F11	AA25	IO138PB4F12	AK25
IO104PB3F9	V29	IO122NB3F11	AC26	IO139NB4F13	AE21
IO105NB3F9	Y28	IO122PB3F11	AB26	IO139PB4F13	AE22
IO105PB3F9	W28	IO123NB3F11	AG28	IO140NB4F13	AG23
IO106NB3F9	V25	IO123PB3F11	AF28	IO140PB4F13	AG24
IO106PB3F9	U25	IO124NB3F11	AB23	IO141NB4F13	AF22
IO107NB3F10	W26	IO124PB3F11	AA23	IO141PB4F13	AF23
IO107PB3F10	V26	IO125NB3F11	AF27	IO142NB4F13	AJ23
IO108NB3F10	W24	IO125PB3F11	AE27	IO142PB4F13	AJ24
IO108PB3F10	V24	IO126NB3F11	AD25	IO143NB4F13	AD19
IO109NB3F10	Y27	IO126PB3F11	AC25	IO143PB4F13	AD20
IO109PB3F10	W27	IO127NB3F11	AE26	IO144NB4F13	AG21
IO110NB3F10	V23	IO127PB3F11	AD26	IO144PB4F13	AG22
IO110PB3F10	V22	IO128NB3F11	AC24	IO145NB4F13	AE19
IO111NB3F10	AA29	IO128PB3F11	AB24	IO145PB4F13	AE20
IO111PB3F10	Y29	Bank 4		IO146NB4F13	AF20
IO112NB3F10	Y25	IO129NB4F12	AD23	IO146PB4F13	AF21
IO112PB3F10	W25	IO129PB4F12	AC23	IO147NB4F13	AC19
IO113NB3F10	AB27	IO130NB4F12	AK26	IO147PB4F13	AC20
IO113PB3F10	AA27	IO130PB4F12	AK27	IO148NB4F13	AH22
IO114NB3F10	Y23	IO131NB4F12	AF24	IO148PB4F13	AH23
IO114PB3F10	W23	IO131PB4F12	AF25	IO149NB4F13	AC18
IO115NB3F10	AA26	IO132NB4F12	AG25	IO149PB4F13	AB18
IO115PB3F10	Y26	IO132PB4F12	AG26	IO150NB4F13	AK21
IO116NB3F10	AC28	IO133NB4F12	AD22	IO150PB4F13	AJ21
IO116PB3F10	AB28	IO133PB4F12	AC22	IO151NB4F13	AE18
IO117NB3F10	AE29	IO134NB4F12	AE23	IO151PB4F13	AD18
IO117PB3F10	AD29	IO134PB4F12	AE24	IO152NB4F14	AJ20
IO118NB3F11	AE28	IO135NB4F12	AH24	IO152PB4F14	AK20
IO118PB3F11	AD28	IO135PB4F12	AH25	IO153NB4F14	AG19
IO119NB3F11	AD27	IO136NB4F12	AJ25	IO153PB4F14	AG20
IO119PB3F11	AC27	IO136PB4F12	AJ26	IO154NB4F14	AH19
IO120NB3F11	AA24	IO137NB4F12	AD21	IO154PB4F14	AH20

FG896	
AX1000 Function	Pin Number
VCCIB2	L22
VCCIB2	M21
VCCIB2	M22
VCCIB2	N21
VCCIB2	P21
VCCIB2	R21
VCCIB3	AA22
VCCIB3	AH29
VCCIB3	AH30
VCCIB3	T21
VCCIB3	U21
VCCIB3	V21
VCCIB3	W21
VCCIB3	W22
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA16
VCCIB4	AA17
VCCIB4	AA18
VCCIB4	AA19
VCCIB4	AA20
VCCIB4	AB19
VCCIB4	AB20
VCCIB4	AB21
VCCIB4	AJ28
VCCIB4	AK28
VCCIB5	AA11
VCCIB5	AA12
VCCIB5	AA13
VCCIB5	AA14
VCCIB5	AA15
VCCIB5	AB10
VCCIB5	AB11
VCCIB5	AB12
VCCIB5	AJ3

FG896	
AX1000 Function	Pin Number
VCCIB5	AK3
VCCIB6	AA9
VCCIB6	AH1
VCCIB6	AH2
VCCIB6	T10
VCCIB6	U10
VCCIB6	V10
VCCIB6	W10
VCCIB6	W9
VCCIB6	Y10
VCCIB6	Y9
VCCIB7	C1
VCCIB7	C2
VCCIB7	K9
VCCIB7	L10
VCCIB7	L9
VCCIB7	M10
VCCIB7	M9
VCCIB7	N10
VCCIB7	P10
VCCIB7	R10
VCOMPLA	F14
VCOMPLB	J15
VCOMPLC	F17
VCOMPLD	H16
VCOMPLE	AF17
VCOMPLF	AD16
VCOMPLG	AF14
VCOMPLH	AB15
VPUMP	G24

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
GND	AK12	GND	AN34	GND	D1
GND	AK17	GND	AN4	GND	D11
GND	AK18	GND	AN9	GND	D2
GND	AK23	GND	AP13	GND	D24
GND	AK30	GND	AP2	GND	D3
GND	AK5	GND	AP22	GND	D31
GND	AL1	GND	AP27	GND	D32
GND	AL11	GND	AP3	GND	D33
GND	AL2	GND	AP31	GND	D34
GND	AL24	GND	AP32	GND	D4
GND	AL3	GND	AP33	GND	E12
GND	AL31	GND	AP4	GND	E17
GND	AL32	GND	AP8	GND	E18
GND	AL33	GND	B1	GND	E23
GND	AL34	GND	B2	GND	E30
GND	AL4	GND	B26	GND	E5
GND	AM1	GND	B3	GND	F29
GND	AM10	GND	B31	GND	F30
GND	AM15	GND	B32	GND	F6
GND	AM2	GND	B33	GND	G28
GND	AM20	GND	B34	GND	G7
GND	AM25	GND	B4	GND	H1
GND	AM3	GND	B9	GND	H34
GND	AM31	GND	C1	GND	J2
GND	AM32	GND	C10	GND	J33
GND	AM33	GND	C15	GND	K3
GND	AM34	GND	C2	GND	K32
GND	AM4	GND	C20	GND	L11
GND	AN1	GND	C25	GND	L24
GND	AN2	GND	C3	GND	L31
GND	AN26	GND	C31	GND	L4
GND	AN3	GND	C32	GND	M12
GND	AN31	GND	C33	GND	M23
GND	AN32	GND	C34	GND	M30
GND	AN33	GND	C4	GND	M5

CQ208	
AX250 Function	Pin Number
IO110PB7F7	19
IO112NB7F7	16
IO112PB7F7	17
IO117NB7F7	12
IO117PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121PB7F7	7
IO122NB7F7	5
IO122PB7F7	6
IO123NB7F7	3
IO123PB7F7	4
Dedicated I/O	
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90
GND	94
GND	99
GND	104
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169
GND	173

CQ208	
AX250 Function	Pin Number
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	14
VCCA	38
VCCA	52
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	156
VCCA	168
VCCA	195
VCCDA	1
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
VCCIB0	193

CQ208	
AX250 Function	Pin Number
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124
VCCIB4	89
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCCPLA	189
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

CG624	
AX2000 Function	Pin Number
VCCIB2	D23
VCCIB2	E22
VCCIB2	K17
VCCIB2	L17
VCCIB2	M16
VCCIB3	AA22
VCCIB3	AB23
VCCIB3	AC24
VCCIB3	AC25
VCCIB3	P16
VCCIB3	R17
VCCIB3	T17
VCCIB4	AB21
VCCIB4	AC22
VCCIB4	AD23
VCCIB4	AE23
VCCIB4	T14
VCCIB4	U15
VCCIB4	U16
VCCIB5	AB5
VCCIB5	AC4
VCCIB5	AD3
VCCIB5	AE3
VCCIB5	T12
VCCIB5	U10
VCCIB5	U11
VCCIB6	AA4
VCCIB6	AB3
VCCIB6	AC1
VCCIB6	AC2
VCCIB6	P10
VCCIB6	R9

Note: **Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*

CG624	
AX2000 Function	Pin Number
VCCIB6	T9
VCCIB7	C1
VCCIB7	C2
VCCIB7	D3
VCCIB7	E4
VCCIB7	K9
VCCIB7	L9
VCCIB7	M10
VCCPLA	E12
VCCPLB	J12
VCCPLC	E14
VCCPLD	H14
VCCPLE	Y14
VCCPLF	U14
VCCPLG	Y12
VCCPLH	U12
VCOMPLA	F12
VCOMPLB	H12
VCOMPLC	F14
VCOMPLD	J14
VCOMPLE	AA14
VCOMPLF	V14
VCOMPLG	AA12
VCOMPLH	V12
VPUMP	E20

Note: **Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*