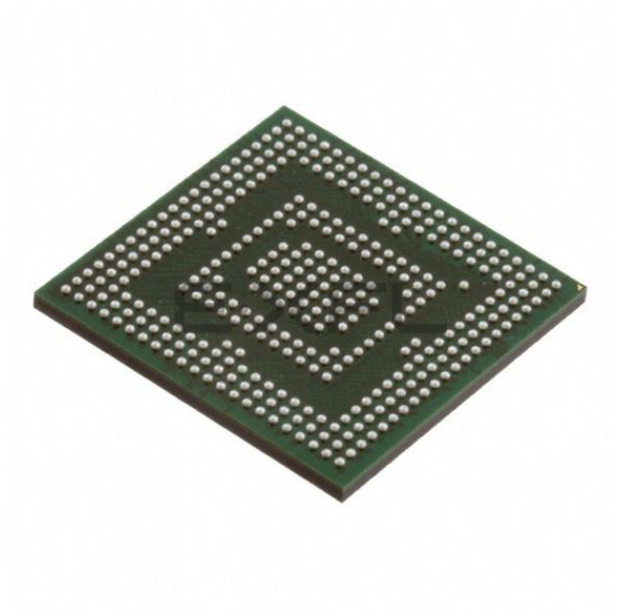

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Dual Core
Interface	CAN, EBI/EMI, Ethernet, I²C, SPI, SPORT, UART/USART, USB OTG
Clock Rate	500MHz
Non-Volatile Memory	ROM (64kB)
On-Chip RAM	808K x 8
Voltage - I/O	1.8V, 3.3V
Voltage - Core	1.25V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	349-LFBGA, CSPBGA
Supplier Device Package	349-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adbf609wcbcz502

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REVISION HISTORY

2/14—Rev. 0 to Rev. A

Added the system clock output specification and additional peripheral external clocks in Clock Related Operating Conditions on Page 53. These changes affect the following peripheral timing sections.

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Serial Ports—External Clock 80
Serial Peripheral Interface (SPI) Port—Master Timing 86
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Additional revisions include the following.

Corrected S0SEL and S1SEL in Figure 8 Clock Relationships and Divider Values 54

Revised the dynamic and static current tables CCLK Dynamic Current per core (mA, with ASF = 1) 57
Static Current—IDD_DEEPSLEEP (mA) 58

Corrected the t_{WARE} parameter in Asynchronous Page Mode Read 64

Corrected the timing diagram in Bus Request/Bus Grant . 69

Corrected the signal names in the following figures:
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Mobile DDR SDRAM Clock and Control Cycle Timing ... 72

Added Figure 29 and updated Table 42 in Enhanced Parallel Peripheral Interface Timing 74

Corrected the t_{HSPIDM}, t_{SDSCIM}, t_{SPICLK}, t_{HDSM}, and t_{SPITDM} specifications in Serial Peripheral Interface (SPI) Port—Master Timing 86

Corrected the t_{HDSPID} specification in Serial Peripheral Interface (SPI) Port—Slave Timing 88

Corrected $t_{SRDYSCKM1}$ in Serial Peripheral Interface (SPI) Port—SPI_RDY Timing 92

Revised all parameters in Timer Cycle Timing 94

Corrected the timing diagram in ADC Controller Module (ACM) Timing 96

Removed TWI signals in footnote 3 in JTAG Test And Emulation Port Timing 101

Added models to Automotive Products 112

Event Handling

The processor provides event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing of a higher-priority event takes precedence over servicing of a lower-priority event. The processor provides support for five different types of events:

- Emulation – An emulation event causes the processor to enter emulation mode, allowing command and control of the processor via the JTAG interface.
- Reset – This event resets the processor.
- Nonmaskable Interrupt (NMI) – The NMI event can be generated either by the software watchdog timer, by the NMI input signal to the processor, or by software. The NMI event is frequently used as a power-down indicator to initiate an orderly shutdown of the system.
- Exceptions – Events that occur synchronously to program flow (in other words, the exception is taken before the instruction is allowed to complete). Conditions such as data alignment violations and undefined instructions cause exceptions.
- Interrupts – Events that occur asynchronously to program flow. They are caused by input signals, timers, and other peripherals, as well as by an explicit software instruction.

Core Event Controller (CEC)

The CEC supports nine general-purpose interrupts (IVG15–7), in addition to the dedicated interrupt and exception events. Of these general-purpose interrupts, the two lowest-priority interrupts (IVG15–14) are recommended to be reserved for software interrupt handlers. For more information, see the *ADSP-BF60x Processor Programmer's Reference*.

System Event Controller (SEC)

The SEC manages the enabling, prioritization, and routing of events from each system interrupt or fault source. Additionally, it provides notification and identification of the highest priority active system interrupt request to each core and routes system fault sources to its integrated fault management unit.

Trigger Routing Unit (TRU)

The TRU provides system-level sequence control without core intervention. The TRU maps trigger masters (generators of triggers) to trigger slaves (receivers of triggers). Slave endpoints can be configured to respond to triggers in various ways. Common applications enabled by the TRU include:

- Automatically triggering the start of a DMA sequence after a sequence from another DMA channel completes
- Software triggering
- Synchronization of concurrent activities

Pin Interrupts

Every port pin on the processor can request interrupts in either an edge-sensitive or a level-sensitive manner with programmable polarity. Interrupt functionality is decoupled from GPIO operation. Six system-level interrupt channels (PINT0–5) are reserved for this purpose. Each of these interrupt channels can manage up to 32 interrupt pins. The assignment from pin to interrupt is not performed on a pin-by-pin basis. Rather, groups of eight pins (half ports) can be flexibly assigned to interrupt channels.

Every pin interrupt channel features a special set of 32-bit memory-mapped registers that enable half-port assignment and interrupt management. This includes masking, identification, and clearing of requests. These registers also enable access to the respective pin states and use of the interrupt latches, regardless of whether the interrupt is masked or not. Most control registers feature multiple MMR address entries to write-one-to-set or write-one-to-clear them individually.

General-Purpose I/O (GPIO)

Each general-purpose port pin can be individually controlled by manipulation of the port control, status, and interrupt registers:

- GPIO direction control register – Specifies the direction of each individual GPIO pin as input or output.
- GPIO control and status registers – A "write one to modify" mechanism allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins.
- GPIO interrupt mask registers – Allow each individual GPIO pin to function as an interrupt to the processor. GPIO pins defined as inputs can be configured to generate hardware interrupts, while output pins can be triggered by software interrupts.
- GPIO interrupt sensitivity registers – Specify whether individual pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant.

Pin Multiplexing

The processor supports a flexible multiplexing scheme that multiplexes the GPIO pins with various peripherals. A maximum of 4 peripherals plus GPIO functionality is shared by each GPIO pin. All GPIO pins have a bypass path feature – that is, when the output enable and the input enable of a GPIO pin are both active, the data signal before the pad driver is looped back to the receive path for the same GPIO pin. For more information, see GP I/O Multiplexing for 349-Ball CSP_BGA on Page 33.

MEMORY ARCHITECTURE

The processor views memory as a single unified 4G byte address space, using 32-bit addresses. All resources, including internal memory, external memory, and I/O control registers, occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low-latency core-accessible memory as cache or SRAM, and larger, lower-cost and performance interface-accessible memory systems. See Figure 3 and Figure 4.

Memory Protection

The Blackfin cores feature a memory protection concept, which grants data and/or instruction accesses from enabled memory regions only. A supervisor mode vs. user mode programming model supports dynamically varying access rights. Increased flexibility in memory page size options supports a simple method of static memory partitioning.

System Protection

All system resources and L2 memory banks can be controlled by either the processor cores, memory-to-memory DMA, or the system debug unit (SDU). A system protection unit (SPU) enables write accesses to specific resources that are locked to any of four masters: Core 0, Core 1, Memory DMA, and the System Debug Unit. System protection is enabled in greater granularity for some modules (L2, SEC and GPIO controllers) through a *global lock* concept.

Watchpoint Protection

The primary purpose of watchpoints and hardware breakpoints is to serve emulator needs. When enabled, they signal an emulator event whenever user-defined system resources are accessed or a core executes from user-defined addresses. Watchpoint events can be configured such that they signal the events to the other Blackfin core or to the fault management unit.

Dual Watchdog

The two on-chip watchdog timers each may supervise one Blackfin core.

Bandwidth Monitor

All DMA channels that operate in memory-to-memory mode (Memory DMA, PVP Memory Pipe DMA, PIXC DMA) are equipped with a bandwidth monitor mechanism. They can signal a system event or fault when transactions tend to starve because system buses are fully loaded with higher-priority traffic.

Signal Watchdogs

The eight general-purpose timers feature two new modes to monitor off-chip signals. The Watchdog Period mode monitors whether external signals toggle with a period within an expected range. The Watchdog Width mode monitors whether the pulse widths of external signals are in an expected range. Both modes help to detect incorrect undesired toggling (or lack thereof) of system-level signals.

Up/Down Count Mismatch Detection

The up/down counter can monitor external signal pairs, such as request/grant strobes. If the edge count mismatch exceeds the expected range, the up/down counter can flag this to the processor or to the fault management unit.

Fault Management

The fault management unit is part of the system event controller (SEC). Any system event, whether a dual-bit uncorrectable ECC error, or any peripheral status interrupt, can be defined as being a "fault". Additionally, the system events can be defined as an interrupt to the cores. If defined as such, the SEC forwards the event to the fault management unit which may automatically reset the entire device for reboot, or simply toggle the SYS_FAULT output pins to signal off-chip hardware. Optionally, the fault management unit can delay the action taken via a keyed sequence, to provide a final chance for the Blackfin cores to resolve the crisis and to prevent the fault action from being taken.

ADDITIONAL PROCESSOR PERIPHERALS

The processor contains a rich set of peripherals connected to the core via several high-bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the block diagram on Page 1). The processors contain high-speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

The following sections describe additional peripherals that were not described in the previous sections.

Timers

The processor includes several timers which are described in the following sections.

General-Purpose Timers

There is one GP timer unit and it provides eight general-purpose programmable timers. Each timer has an external pin that can be configured either as a pulse width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input on the TMRx pins, an external clock TMRCLK input pin, or to the internal SCLK0.

The timer units can be used in conjunction with the UARTs and the CAN controller to measure the width of the pulses in the data stream to provide a software auto-baud detect function for the respective serial channels.

The timers can generate interrupts to the processor core, providing periodic events for synchronization to either the system clock or to external signals. Timer events can also trigger other peripherals via the TRU (for instance, to signal a fault).

Core Timers

Each processor core also has its own dedicated timer. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generating periodic operating system interrupts.

Watchdog Timers

Each core includes a 32-bit timer, which may be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state, via generation of a hardware reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before

A third counter input can provide flexible zero marker support and can alternatively be used to input the push-button signal of thumb wheels. All three pins have a programmable debouncing circuit.

Internal signals forwarded to each general-purpose timer enable these timers to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmable count values are exceeded.

Serial Peripheral Interface (SPI) Ports

The processors have two SPI-compatible ports that allow the processor to communicate with multiple SPI-compatible devices.

In its simplest mode, the SPI interface uses three pins for transferring data: two data pins (Master Output-Slave Input, MOSI, and Master Input-Slave Output, MISO) and a clock pin (serial clock, SPI_CLK). A SPI chip select input pin ($\overline{\text{SPI\_SS}}$) lets other SPI devices select the processor, and seven SPI chip select output pins ($\overline{\text{SPI\_SEL7–1}}$) let the processor select other SPI devices. The SPI select pins are reconfigured general-purpose I/O pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

In a multi-master or multi-slave SPI system, the MOSI and MISO data output pins can be configured to behave as open drain outputs (using the ODM bit) to prevent contention and possible damage to pin drivers. An external pull-up resistor is required on both the MOSI and MISO pins when this option is selected.

When ODM is set and the SPI is configured as a master, the MOSI pin is three-stated when the data driven out on MOSI is a logic-high. The MOSI pin is not three-stated when the driven data is a logic-low. Similarly, when ODM is set and the SPI is configured as a slave, the MISO pin is three-stated if the data driven out on MISO is a logic-high.

The SPI port's baud rate and clock phase/polarities are programmable, and it has integrated DMA channels for both transmit and receive data streams.

UART Ports

The processors provide two full-duplex universal asynchronous receiver/transmitter (UART) ports, which are fully compatible with PC-standard UARTs. Each UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits, and none, even, or odd parity. Optionally, an additional address bit can be transferred to interrupt only addressed nodes in multi-drop bus (MDB) systems. A frame is terminates by one, one and a half, two or two and a half stop bits.

The UART ports support automatic hardware flow control through the Clear To Send (CTS) input and Request To Send (RTS) output with programmable assertion FIFO levels.

To help support the Local Interconnect Network (LIN) protocols, a special command causes the transmitter to queue a break command of programmable bit length into the transmit buffer. Similarly, the number of stop bits can be extended by a programmable inter-frame space.

The capabilities of the UARTs are further extended with support for the Infrared Data Association (IrDA®) serial infrared physical layer link specification (SIR) protocol.

TWI Controller Interface

The processors include a 2-wire interface (TWI) module for providing a simple exchange method of control data between multiple devices. The TWI module is compatible with the widely used I^2C bus standard. The TWI module offers the capabilities of simultaneous master and slave operation and support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two pins for transferring clock (TWI_SCL) and data (TWI_SDA) and supports the protocol at speeds up to 400k bits/sec. The TWI interface pins are compatible with 5 V logic levels.

Additionally, the TWI module is fully compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

Removable Storage Interface (RSI)

The removable storage interface (RSI) controller acts as the host interface for multimedia cards (MMC), secure digital memory cards (SD), secure digital input/output cards (SDIO). The following list describes the main features of the RSI controller.

- Support for a single MMC, SD memory, SDIO card
- Support for 1-bit and 4-bit SD modes
- Support for 1-bit, 4-bit, and 8-bit MMC modes
- Support for eMMC 4.3 embedded NAND flash devices
- A ten-signal external interface with clock, command, and up to eight data lines
- Card interface clock generation from SCLK0
- SDIO interrupt and read wait features

Controller Area Network (CAN)

A CAN controller implements the CAN 2.0B (active) protocol. This protocol is an asynchronous communications protocol used in both industrial and automotive control systems. The CAN protocol is well suited for control applications due to its capability to communicate reliably over a network. This is because the protocol incorporates CRC checking, message error tracking, and fault node confinement.

The CAN controller offers the following features:

- 32 mailboxes (8 receive only, 8 transmit only, 16 configurable for receive or transmit).
- Dedicated acceptance masks for each mailbox.
- Additional data filtering on first two bytes.
- Support for both the standard (11-bit) and extended (29-bit) identifier (ID) message formats.

Table 3. Clock Dividers

Clock Source	Divider
CCLK (core clock)	By 4
SYSCLK (System clock)	By 2
SCLK0 (system clock for PVP, all peripherals not covered by SCLK1)	None
SCLK1 (system clock for SPORTS, SPI, ACM)	None
DCLK (LPDDR/DDR2 clock)	By 2
OCLK (output clock)	Programmable
CLKBUF	None, direct from SYS_CLKIN

Power Management

As shown in Table 4, the processor supports five different power domains, which maximizes flexibility while maintaining compliance with industry standards and conventions. There are no sequencing requirements for the various power domains, but all domains must be powered according to the appropriate Specifications table for processor operating conditions; even if the feature/peripheral is not used.

Table 4. Power Domains

Power Domain	V_{DD} Range
All internal logic	V_{DD_INT}
DDR2/LPDDR	V_{DD_DMC}
USB	V_{DD_USB}
Thermal diode	V_{DD_TD}
All other I/O (includes SYS, JTAG, and Ports pins)	V_{DD_EXT}

The dynamic power management feature of the processor allows the processor's core clock frequency (f_{CCLK}) to be dynamically controlled.

The power dissipated by a processor is largely a function of its clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation.

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor cores and all enabled peripherals run at full speed.

Active Operating Mode—Moderate Dynamic Power Savings

In the active mode, the PLL is enabled but bypassed. Because the PLL is bypassed, the processor's core clocks and system clocks run at the input clock (SYS_CLKIN) frequency. DMA access is available to appropriately configured L1 memories.

For more information about PLL controls, see the "Dynamic Power Management" chapter in the *ADSP-BF60x Blackfin Processor Hardware Reference.*

See Table 5 for a summary of the power settings for each mode.

Table 5. Power Settings

Mode/State	PLL	PLL Bypassed	f_{CCLK}	f_{SYSCLK}, f_{DCLK}, f_{SCLK0}, f_{SCLK1}	Core Power
Full On	Enabled	No	Enabled	Enabled	On
Active	Enabled/ Disabled	Yes	Enabled	Enabled	On
Deep Sleep	Disabled	—	Disabled	Disabled	On
Hibernate	Disabled	—	Disabled	Disabled	Off

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core and to all synchronous peripherals. Asynchronous peripherals may still be running but cannot access internal resources or external memory.

Hibernate State—Maximum Static Power Savings

The hibernate state maximizes static power savings by disabling the voltage and clocks to the processor cores and to all of the peripherals. This setting signals the external voltage regulator supplying the V_{DD_INT} pins to shut off using the SYS_EXTWAKE signal, which provides the lowest static power dissipation. Any critical information stored internally (for example, memory contents, register contents, and other information) must be written to a non-volatile storage device prior to removing power if the processor state is to be preserved.

Since the V_{DD_EXT} pins can still be supplied in this mode, all of the external pins three-state, unless otherwise specified. This allows other devices that may be connected to the processor to still have power applied without drawing unwanted current.

Reset Control Unit

Reset is the initial state of the whole processor or one of the cores and is the result of a hardware or software triggered event. In this state, all control registers are set to their default values and functional units are idle. Exiting a full system reset starts with Core-0 only being ready to boot. Exiting a Core-n only reset starts with this Core-n being ready to boot.

The Reset Control Unit (RCU) controls how all the functional units enter and exit reset. Differences in functional requirements and clocking constraints define how reset signals are generated. Programs must guarantee that none of the reset functions puts the system into an undefined state or causes resources to stall. This is particularly important when only one of the cores is reset (programs must ensure that there is no pending system activity involving the core that is being reset).

Table 7. ADSP-BF60x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
LP3_D6	LP3 Data 6	F	PF_14
LP3_D7	LP3 Data 7	F	PF_15
PA_00 – PA_15	PORTA Position 00 through PORTA Position 15	A	PA_00 – PA_15
PB_00 – PB_15	PORTB Position 00 through PORTB Position 15	B	PB_00 – PB_15
PC_00 – PC_15	PORTC Position 00 through PORTC Position 15	C	PC_00 – PC_15
PD_00 – PD_15	PORTD Position 00 through PORTD Position 15	D	PD_00 – PD_15
PE_00 – PE_15	PORTE Position 00 through PORTE Position 15	E	PE_00 – PE_15
PF_00 – PF_15	PORTF Position 00 through PORTF Position 15	F	PF_00 – PF_15
PG_00 – PG_15	PORTG Position 00 through PORTG Position 15	G	PG_00 – PG_15
PPI0_CLK	EPPI0 Clock	E	PE_09
PPI0_D00	EPPI0 Data 0	F	PF_00
PPI0_D01	EPPI0 Data 1	F	PF_01
PPI0_D02	EPPI0 Data 2	F	PF_02
PPI0_D03	EPPI0 Data 3	F	PF_03
PPI0_D04	EPPI0 Data 4	F	PF_04
PPI0_D05	EPPI0 Data 5	F	PF_05
PPI0_D06	EPPI0 Data 6	F	PF_06
PPI0_D07	EPPI0 Data 7	F	PF_07
PPI0_D08	EPPI0 Data 8	F	PF_08
PPI0_D09	EPPI0 Data 9	F	PF_09
PPI0_D10	EPPI0 Data 10	F	PF_10
PPI0_D11	EPPI0 Data 11	F	PF_11
PPI0_D12	EPPI0 Data 12	F	PF_12
PPI0_D13	EPPI0 Data 13	F	PF_13
PPI0_D14	EPPI0 Data 14	F	PF_14
PPI0_D15	EPPI0 Data 15	F	PF_15
PPI0_D16	EPPI0 Data 16	E	PE_03
PPI0_D17	EPPI0 Data 17	E	PE_04
PPI0_D18	EPPI0 Data 18	E	PE_00
PPI0_D19	EPPI0 Data 19	E	PE_01
PPI0_D20	EPPI0 Data 20	D	PD_12
PPI0_D21	EPPI0 Data 21	D	PD_15
PPI0_D22	EPPI0 Data 22	E	PE_02
PPI0_D23	EPPI0 Data 23	E	PE_05
PPI0_FS1	EPPI0 Frame Sync 1 (HSYNC)	E	PE_08
PPI0_FS2	EPPI0 Frame Sync 2 (VSYNC)	E	PE_07
PPI0_FS3	EPPI0 Frame Sync 3 (FIELD)	E	PE_06
PPI1_CLK	EPPI1 Clock	B	PB_14
PPI1_D00	EPPI1 Data 0	C	PC_00
PPI1_D01	EPPI1 Data 1	C	PC_01
PPI1_D02	EPPI1 Data 2	C	PC_02
PPI1_D03	EPPI1 Data 3	C	PC_03
PPI1_D04	EPPI1 Data 4	C	PC_04
PPI1_D05	EPPI1 Data 5	C	PC_05
PPI1_D06	EPPI1 Data 6	C	PC_06
PPI1_D07	EPPI1 Data 7	C	PC_07

Table 12. Signal Multiplexing for Port E

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function Input Tap
PE_00	SPI1_D3	PPI0_D18	SPT1_BD1	
PE_01	SPI1_D2	PPI0_D19	SPT1_BD0	
PE_02	SPI1_RDY	PPI0_D22	SPT1_ACLK	
PE_03		PPI0_D16	ACM0_FS/SPT1_BFS	
PE_04		PPI0_D17	ACM0_CLK/SPT1_BCLK	
PE_05		PPI0_D23	SPT1_AFS	
PE_06	SPT1_ATDV	PPI0_FS3	LP3_CLK	
PE_07	SPT1_BTDV	PPI0_FS2	LP3_ACK	
PE_08	PWM0_SYNC	PPI0_FS1	LP2_ACK	ACM0_T0
PE_09		PPI0_CLK	LP2_CLK	$\overline{\text{PWM0\_TRIP0}}$
PE_10	ETH1_MDC	PWM1_DL	RSI0_D6	
PE_11	ETH1_MDIO	PWM1_DH	RSI0_D7	
PE_12		PWM1_CL	RSI0_D5	
PE_13	ETH1_CRS	PWM1_CH	RSI0_D4	
PE_14		SPT2_ATDV	TM0_TMR0	
PE_15	ETH1_RXD1	PWM1_BL	RSI0_D3	

Table 13. Signal Multiplexing for Port F

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function Input Tap
PF_00	PWM0_AL	PPI0_D00	LP2_D0	
PF_01	PWM0_AH	PPI0_D01	LP2_D1	
PF_02	PWM0_BL	PPI0_D02	LP2_D2	
PF_03	PWM0_BH	PPI0_D03	LP2_D3	
PF_04	PWM0_CL	PPI0_D04	LP2_D4	
PF_05	PWM0_CH	PPI0_D05	LP2_D5	
PF_06	PWM0_DL	PPI0_D06	LP2_D6	
PF_07	PWM0_DH	PPI0_D07	LP2_D7	
PF_08	$\overline{\text{SPI1\_SEL5}}$	PPI0_D08	LP3_D0	
PF_09	$\overline{\text{SPI1\_SEL6}}$	PPI0_D09	LP3_D1	
PF_10	ACM0_A4	PPI0_D10	LP3_D2	
PF_11		PPI0_D11	LP3_D3	$\overline{\text{PWM0\_TRIP1}}$
PF_12	ACM0_A2	PPI0_D12	LP3_D4	
PF_13	ACM0_A3	PPI0_D13	LP3_D5	
PF_14	ACM0_A0	PPI0_D14	LP3_D6	
PF_15	ACM0_A1	PPI0_D15	LP3_D7	

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
DMC0_DQ13	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 13. Notes: No notes.
DMC0_DQ14	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 14. Notes: No notes.
DMC0_DQ15	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 15. Notes: No notes.
DMC0_LDM	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Mask for Lower Byte. Notes: No notes.
DMC0_LDQS	I/O	C	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Lower Byte. Notes: For LPDDR, a 100k ohm pull-down resistor is required.
$\overline{\text{DMC0\_LDQS}}$	I/O	C	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Lower Byte (complement). Notes: For single ended DDR2, connect to VREF_DMC. For LPDDR, leave unconnected.
DMC0_ODT	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 On-die termination. Notes: For LPDDR, leave unconnected.
$\overline{\text{DMC0\_RAS}}$	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Row Address Strobe. Notes: No notes.
DMC0_UDM	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Mask for Upper Byte. Notes: No notes.
DMC0_UDQS	I/O	C	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Upper Byte. Notes: For LPDDR, a 100k ohm pull-down resistor is required.
$\overline{\text{DMC0\_UDQS}}$	I/O	C	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Upper Byte (complement). Notes: For single ended DDR2, connect to VREF_DMC. For LPDDR, leave unconnected.
$\overline{\text{DMC0\_WE}}$	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Write Enable. Notes: No notes.
GND	g	na	none	none	none	none	none	na	Desc: Ground. Notes: No notes.
$\overline{\text{JTG\_EMU}}$	I/O	A	none	none	none	none	none	VDD_EXT	Desc: Emulation Output. Notes: No notes.
JTG_TCK	I/O	na	pd	none	none	none	none	VDD_EXT	Desc: JTG Clock. Notes: Functional during reset.
JTG_TDI	I/O	na	pu	none	none	none	none	VDD_EXT	Desc: JTG Serial Data Input. Notes: Functional during reset.
JTG_TDO	I/O	A	none	none	none	none	none	VDD_EXT	Desc: JTG Serial Data Output. Notes: Functional during reset, three-state when $\overline{\text{JTG\_TRST}}$ is asserted.
JTG_TMS	I/O	na	pu	none	none	none	none	VDD_EXT	Desc: JTG Mode Select. Notes: Functional during reset.
$\overline{\text{JTG\_TRST}}$	I/O	na	pd	none	none	none	none	VDD_EXT	Desc: JTG Reset. Notes: Functional during reset.

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

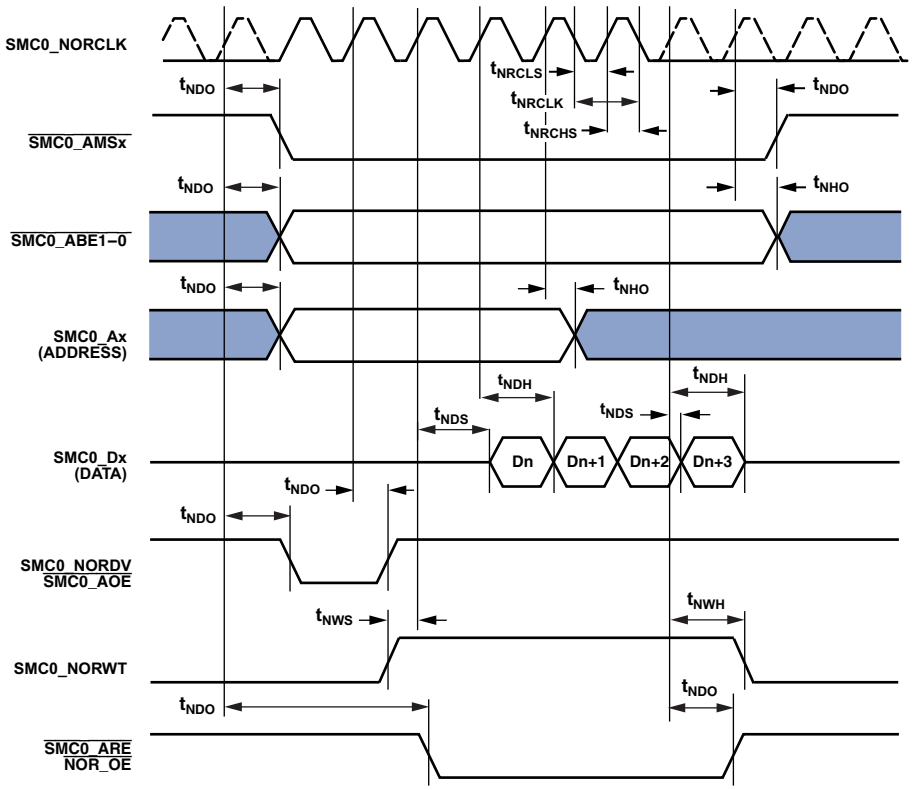
Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PF_03	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 3 | PWM0 Channel B High Side | EPPI0 Data 3 | LP2 Data 3. Notes: No notes.
PF_04	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 4 | PWM0 Channel C Low Side | EPPI0 Data 4 | LP2 Data 4. Notes: No notes.
PF_05	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 5 | PWM0 Channel C High Side | EPPI0 Data 5 | LP2 Data 5. Notes: No notes.
PF_06	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 6 | PWM0 Channel D Low Side | EPPI0 Data 6 | LP2 Data 6. Notes: No notes.
PF_07	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 7 | PWM0 Channel D High Side | EPPI0 Data 7 | LP2 Data 7. Notes: No notes.
PF_08	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 8 | SPI1 Slave Select Output b | EPPI0 Data 8 | LP3 Data 0. Notes: No notes.
PF_09	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 9 | SPI1 Slave Select Output b | EPPI0 Data 9 | LP3 Data 1. Notes: No notes.
PF_10	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 10 | ACM0 Address 4 | EPPI0 Data 10 | LP3 Data 2. Notes: No notes.
PF_11	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 11 | EPPI0 Data 11 | LP3 Data 3 | PWM0 Shutdown Input. Notes: No notes.
PF_12	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 12 | ACM0 Address 2 | EPPI0 Data 12 | LP3 Data 4. Notes: No notes.
PF_13	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 13 | ACM0 Address 3 | EPPI0 Data 13 | LP3 Data 5. Notes: No notes.
PF_14	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 14 | EPPI0 Data 14 | ACM0 Address 0 | LP3 Data 6. Notes: No notes.
PF_15	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 15 | ACM0 Address 1 | EPPI0 Data 15 | LP3 Data 7. Notes: No notes.
PG_00	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PG Position 0 | PWM1 Channel B High Side | RSI0 Data 2 | ETH1 Receive Data 0. Notes: Has an optional internal pull-up resistor for use with RSI. See the RSI chapter in the processor hardware reference for more details.
PG_01	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PG Position 1 | SPORT2 Channel A Frame Sync | TIMER0 Timer 2 | CAN0 Transmit. Notes: No notes.

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
USB0_DP	I/O	F	none	none	none	none	none	VDD_USB	Desc: USB0 Data +. Notes: Pull low if not using USB. For complete documentation of hibernate behavior when USB is used, see the USB chapter in the processor hardware reference.
USB0_ID	I/O	na	none	none	none	pu	none	VDD_USB	Desc: USB0 OTG ID. Notes: If USB is not used, connect to ground. When USB is being used, the internal pull-up resistor that is present during hibernate is programmable. See the USB chapter in the processor hardware reference. Active during reset.
USB0_VBC	I/O	E	none	none	none	wk	none	VDD_USB	Desc: USB0 VBUS Control. Notes: If USB is not used, pull low.
USB0_VBUS	I/O	G	none	none	none	none	none	VDD_USB	Desc: USB0 Bus Voltage. Notes: If USB is not used, connect to ground.
VDD_DMC	s	na	none	none	none	none	none	na	Desc: VDD for DMC. Notes: If the DMC is not used, connect to VDD_INT.
VDD_EXT	s	na	none	none	none	none	none	na	Desc: External VDD. Notes: Must be powered.
VDD_INT	s	na	none	none	none	none	none	na	Desc: Internal VDD. Notes: Must be powered.
VDD_TD	s	na	none	none	none	none	none	na	Desc: VDD for Thermal Diode. Notes: If the thermal diode is not used, connect to ground.
VDD_USB	s	na	none	none	none	none	none	na	Desc: VDD for USB. Notes: If USB is not used, connect to VDD_EXT.
VREF_DMC	s	na	none	none	none	none	none	na	Desc: VREF for DMC. Notes: If the DMC is not used, connect to VDD_INT.

Parameter		Test Conditions	Min	Typical	Max	Unit
I_{DD_IDLE}[23]	V_{DD_INT} Current in Idle	f_{CCLK} = 500 MHz ASFC0 = 0.14 (Idle) ASFC1 = 0 (Disabled) f_{SYSCLK} = 250 MHz, $f_{SCLK0/1}$ = 125 MHz f_{DCLK} = 0 MHz (DDR Disabled) f_{USBCLK} = 0 MHz (USB Disabled) No PVP or DMA activity T_J = 25°C		137		mA
I_{DD_TYP}[23]	V_{DD_INT} Current	f_{CCLK} = 500 MHz ASFC0 = 1.0 (Full-on Typical) ASFC1 = 0.86 (App) f_{SYSCLK} = 250 MHz, $f_{SCLK0/1}$ = 125 MHz f_{DCLK} = 250 MHz f_{USBCLK} = 0 MHz (USB Disabled) DMA Data Rate = 124 MB/s Medium PVP Activity T_J = 25°C		357		mA
$I_{DD\_HIBERNATE}$[22, 24]	Hibernate State Current	V_{DD_INT} = 0 V, V_{DD_EXT} = V_{DD_TD} = V_{DD_USB} = 3.3 V, V_{DD_DMC} = 1.8 V, V_{REF_DMC} = 0.9 V, T_J = 25°C, f_{CLKIN} = 0 MHz		40		µA
$I_{DD\_HIBERNATE}$[22, 24]	Hibernate State Current Without USB	V_{DD_INT} = 0 V, V_{DD_EXT} = V_{DD_TD} = V_{DD_USB} = 3.3 V, V_{DD_DMC} = 1.8 V, V_{REF_DMC} = 0.9 V, T_J = 25°C, f_{CLKIN} = 0 MHz, USB protection disabled (USB0_PHY_CTL.DIS=1)		10		µA
I_{DD_INT}[23]	V_{DD_INT} Current	f_{CCLK} > 0 MHz $f_{SCLK0/1}$ ≥ 0 MHz			See I_{DDINT_TOT} equation on Page 57	mA

[1] Applies to all output and bidirectional signals except DMC0 signals, TWI signals and USB0 signals.
[2] Applies to all DMC0 output and bidirectional signals in DDR2 full drive strength mode.
[3] Applies to all DMC0 output and bidirectional signals in DDR2 half drive strength mode.
[4] Applies to all DMC0 output and bidirectional signals in LPDDR full drive strength mode.
[5] Applies to all DMC0 output and bidirectional signals in LPDDR three-quarter drive strength mode.
[6] Applies to all DMC0 output and bidirectional signals in LPDDR half drive strength mode.
[7] Applies to all DMC0 output and bidirectional signals in LPDDR one-quarter drive strength mode.
[8] Applies to all output and bidirectional signals except DMC0 signals and USB0 signals.
[9] Applies to signals SMC0_ARDY, $\overline{\text{SMC0\_BR}}$, SYS_BMODE0–2, SYS_CLKIN, SYS_HWRST, SYS_PWRGD, JTG_TDI, and $\overline{\text{JTG\_TMS}}$.
[10] Applies to signals JTG_TCK and $\overline{\text{JTG\_TRST}}$.
[11] Applies to signals SMC0_ARDY, $\overline{\text{SMC0\_BR}}$, SYS_BMODE0–2, SYS_CLKIN, SYS_HWRST, SYS_PWRGD, JTG_TCK, and $\overline{\text{JTG\_TRST}}$.
[12] Applies to signals JTG_TDI, JTG_TMS.
[13] Applies to signal USB0_CLKIN.
[14] Applies to signals PA0–15, PB0–15, PC0–15, PD0–15, PE0–15, PF0–15, PG0–15, $\overline{\text{SMC0\_AMS0}}$, $\overline{\text{SMC0\_ARE}}$, $\overline{\text{SMC0\_AWE}}$, $\overline{\text{SMC0\_A0E}}$, SMC0_A01–02, SMC0_D00–15, SYS_FAULT, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{JTG\_EMU}}$, JTG_TDO, USB0_DM, USB0_DP, USB0_ID, USB0_VBC, USB0_VBUS.
[15] Applies to DMC0_A[00:13], $\overline{\text{DMC0\_BA}}$[0:2], $\overline{\text{DMC0\_CAS}}$, $\overline{\text{DMC0\_CS0}}$, DMC0_DQ[00:15], DMC0_LQDS, $\overline{\text{DMC0\_LDQS}}$, DMC0_UDQS, $\overline{\text{DMC0\_UDQS}}$, DMC0_LDM, DMC0_UDM, DMC0_ODT, $\overline{\text{DMC0\_RAS}}$, and $\overline{\text{DMC0\_WE}}$.
[16] Applies to signals PA0–15, PB0–15, PC0–15, PD0–15, PE0–15, PF0–15, PG0–15, $\overline{\text{SMC0\_A0E}}$, SMC0_A01–02, SMC0_D00–15, SYS_FAULT, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{JTG\_EMU}}$, JTG_TDO, USB0_DM, USB0_DP, USB0_ID, USB0_VBC, USB0_VBUS, DMC0_A00–13, DMC0_BA0–2, $\overline{\text{DMC0\_CAS}}$, $\overline{\text{DMC0\_CS0}}$, DMC0_DQ00–15, DMC0_LQDS, $\overline{\text{DMC0\_LDQS}}$, DMC0_UDQS, $\overline{\text{DMC0\_UDQS}}$, DMC0_LDM, DMC0_UDM, DMC0_ODT, $\overline{\text{DMC0\_RAS}}$, $\overline{\text{DMC0\_WE}}$, and TWI signals.
[17] Applies to signals $\overline{\text{SMC0\_AMS0}}$, $\overline{\text{SMC0\_ARE}}$, $\overline{\text{SMC0\_AWE}}$, and when RSI pull-up resistors are enabled, PE10–13, 15 and PG00, 02, 03, 05.
[18] Applies to all TWI signals.
[19] Applies to all signals, except DMC0 and TWI signals.
[20] Guaranteed, but not tested.
[21] Applies to all DMC0 signals.
[22] See the *ADSP-BF60x Blackfin Processor Hardware Reference Manual* for definition of deep sleep and hibernate operating modes.
[23] Additional information can be found at Total Internal Power Dissipation on Page 57.
[24] Applies to V_{DD_EXT}, V_{DD_DMC}, V_{DD_USB} and V_{DD_TD} supply signals only. Clock inputs are tied high or low.



NOTE: SMC0_NORCLK dotted line represents a free running version of SMC0_NORCLK that is not visible on the SMC0_NORCLK pin.

Figure 15. Synchronous Burst AC Interface Timing

Asynchronous Write

Table 32. Asynchronous Memory Write (BxMODE = b#00)

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Timing Requirement				
$t_{DARDYAWE}$[1]	SMC0_ARDY Valid After $\overline{SMC0\_AWE}$ Low[2]		(WAT – 2.5) × t_{SCLK0} – 17.5	ns
Switching Characteristics				
t_{ENDAT}	DATA Enable After $\overline{SMC0\_AMSx}$ Assertion	–3		ns
t_{DDAT}	DATA Disable After $\overline{SMC0\_AMSx}$ Deassertion		3	ns
t_{AMSAWE}	SMC0_Ax/$\overline{SMC0\_AMSx}$ Assertion Before $\overline{SMC0\_AWE}$ Low[3]	(PREST + WST + PREAT) × t_{SCLK0} – 2		ns
t_{HAWE}	Output[4] Hold After $\overline{SMC0\_AWE}$ High[5]	WHT × t_{SCLK0} – 2		ns
t_{WAWE}[6]	$\overline{SMC0\_AWE}$ Active Low Width[2]	WAT × t_{SCLK0} – 2		ns
$t_{DAWEARDY}$[1]	$\overline{SMC0\_AWE}$ High Delay After SMC0_ARDY Assertion	2.5 × t_{SCLK0}	3.5 × t_{SCLK0} + 17.5	ns

[1] SMC_BxCTL.ARDYEN bit = 1.
[2] WAT value set using the SMC_BxTIM.WAT bits.
[3] PREST, WST, PREAT values set using the SMC_BxETIM.PREST bits, SMC_BxTIM.WST bits, SMC_BxETIM.PREAT bits, and the SMC_BxTIM.RAT bits.
[4] Output signals are DATA, SMC0_Ax, $\overline{SMC0\_AMSx}$, $\overline{SMC0\_ABEx}$.
[5] WHT value set using the SMC_BxTIM.WHT bits.
[6] SMC_BxCTL.ARDYEN bit = 0.

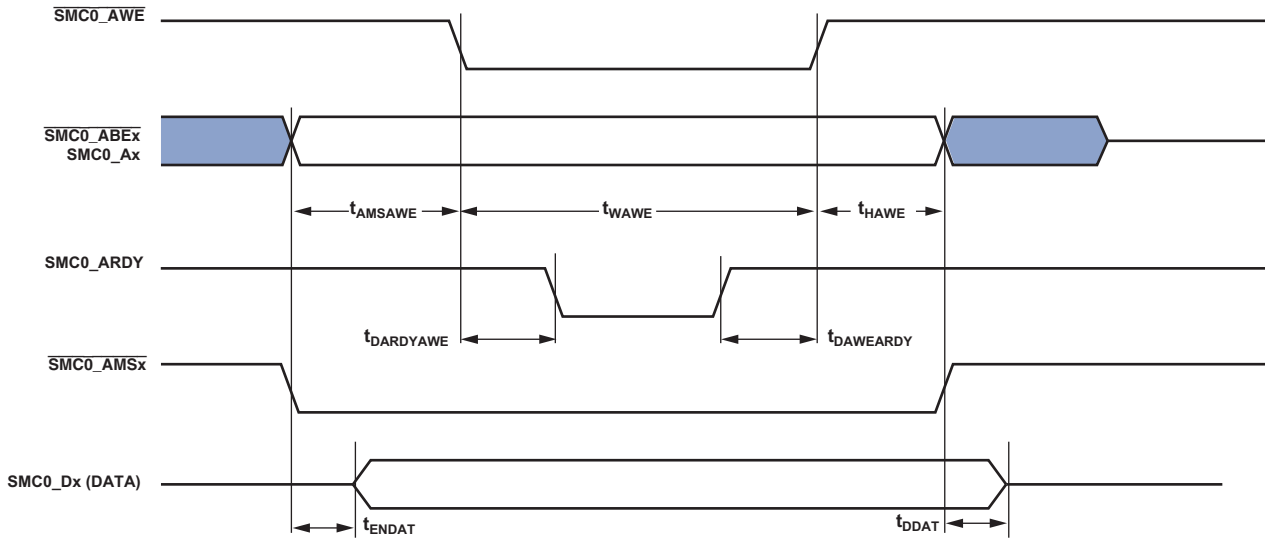


Figure 16. Asynchronous Write

DDR2 SDRAM Read Cycle Timing

Table 37. DDR2 SDRAM Read Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		250 MHz[1] Min	Max	Unit
Timing Requirements				
t_{DQSQ}	DMC0_DQS-DMC0_DQ Skew for DMC0_DQS and Associated DMC0_DQ Signals		0.35	ns
t_{QH}	DMC0_DQ, DMC0_DQS Output Hold Time From DMC0_DQS	1.6		ns
t_{RPRE}	Read Preamble	0.9		t_{CK}
t_{RPST}	Read Postamble	0.4		t_{CK}

[1] In order to ensure proper operation of the DDR2, all the DDR2 guidelines have to be strictly followed.

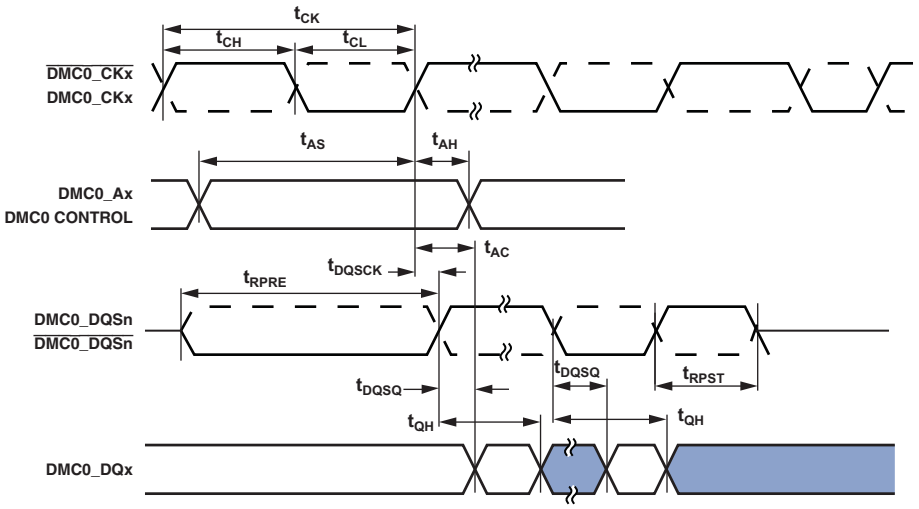
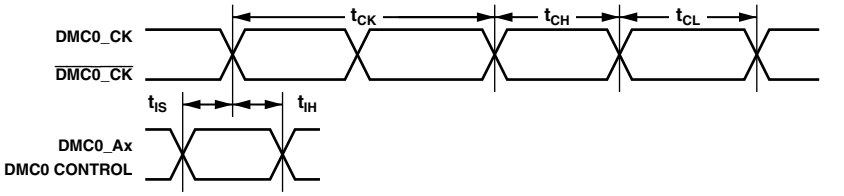


Figure 20. DDR2 SDRAM Controller Input AC Timing

Mobile DDR SDRAM Clock and Control Cycle Timing

Table 39. Mobile DDR SDRAM Read Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		200 MHz Min	200 MHz Max	Unit
Switching Characteristics				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	5		ns
t_{CH}	Minimum Clock Pulse Width	0.45	0.55	t_{CK}
t_{CL}	Maximum Clock Pulse Width	0.45	0.55	t_{CK}
t_{IS}	Control/Address Setup Relative to DMC0_CK Rise	1		ns
t_{IH}	Control/Address Hold Relative to DMC0_CK Rise	1		ns



NOTE: CONTROL = DMC0_CS0, DMC0_CKE, DMC0_RAS, DMC0_CAS, AND DMC0_WE.
ADDRESS = DMC0_A00–13, AND DMC0_BA0–1.

Figure 22. Mobile DDR SDRAM Clock and Control Cycle Timing

Mobile DDR SDRAM Read Cycle Timing

Table 40. Mobile DDR SDRAM Read Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		200 MHz Min	200 MHz Max	Unit
Timing Requirements				
t_{QH}	DMC0_DQ, DMC0_DQS Output Hold Time From DMC0_DQS	1.75		ns
t_{DQSQ}	DMC0_DQS-DMC0_DQ Skew for DMC0_DQS and Associated DMC0_DQ Signals		0.4	ns
t_{RPRE}	Read Preamble	0.9	1.1	t_{CK}
t_{RPST}	Read Postamble	0.4	0.6	t_{CK}

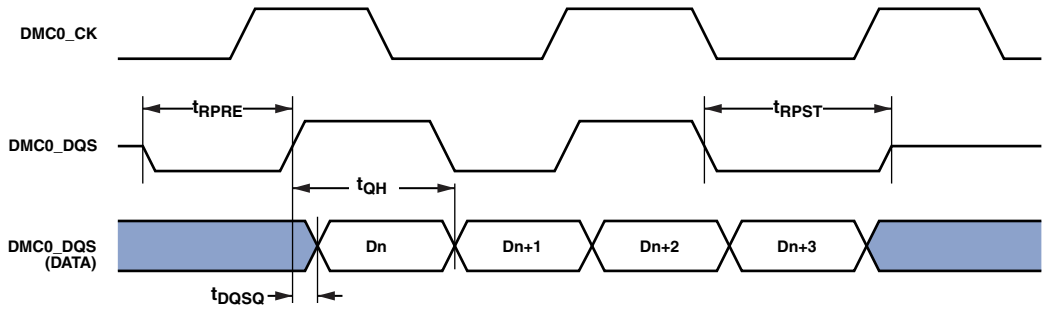


Figure 23. Mobile DDR SDRAM Controller Input AC Timing

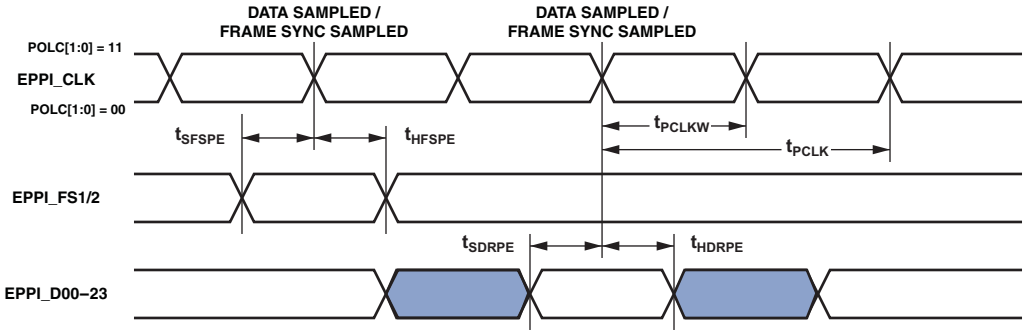


Figure 32. PPI External Clock GP Receive Mode with External Frame Sync Timing

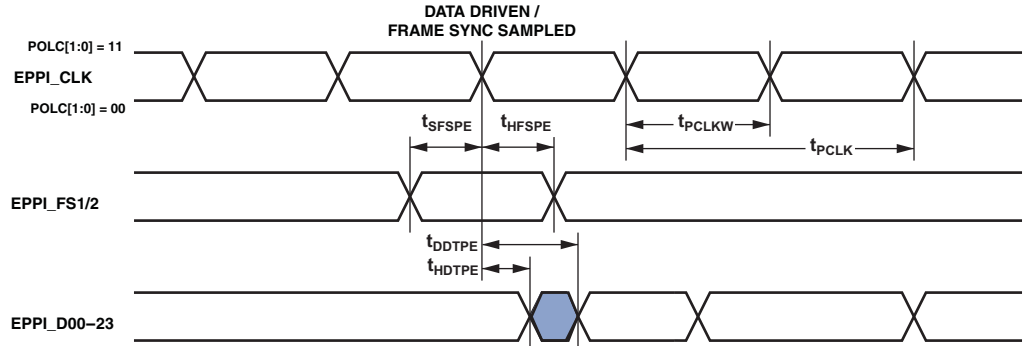


Figure 33. PPI External Clock GP Transmit Mode with External Frame Sync Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

The UART ports receive and transmit operations are described in the *ADSP-BF60x Blackfin Processor Hardware Reference Manual*.

CAN Interface

The CAN interface timing is described in the *ADSP-BF60x Blackfin Processor Hardware Reference Manual*.

Universal Serial Bus (USB) On-The-Go—Receive and Transmit Timing

Table 62 describes the USB On-The-Go receive and transmit operations.

Table 62. USB On-The-Go—Receive and Transmit Timing

Parameter		V_{DD_USB} 3.3 V Nominal Min	Max	Unit
Timing Requirements				
f_{USBS}	USB_XI Frequency	48	48	MHz
fs_{USB}	USB_XI Clock Frequency Stability	–50	+50	ppm

Table 66. 10/100 Ethernet MAC Controller Timing: RMII Station Management

Parameter[1]		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Timing Requirements				
t_{MDIOS}	ETHx_MDIO Input Valid to ETHx_MDC Rising Edge (Setup)	14		ns
t_{MDCIH}	ETHx_MDC Rising Edge to ETHx_MDIO Input Invalid (Hold)	0		ns
Switching Characteristics				
t_{MDCOV}	ETHx_MDC Falling Edge to ETHx_MDIO Output Valid		t_{SCLK0} + 5	ns
t_{MDCOH}	ETHx_MDC Falling Edge to ETHx_MDIO Output Invalid (Hold)	t_{SCLK0} −1		ns

[1] ETHx_MDC/ETHx_MDIO is a 2-wire serial bidirectional port for controlling one or more external PHYs. ETHx_MDC is an output clock whose minimum period is programmable as a multiple of the system clock SCLK0. ETHx_MDIO is a bidirectional data line.

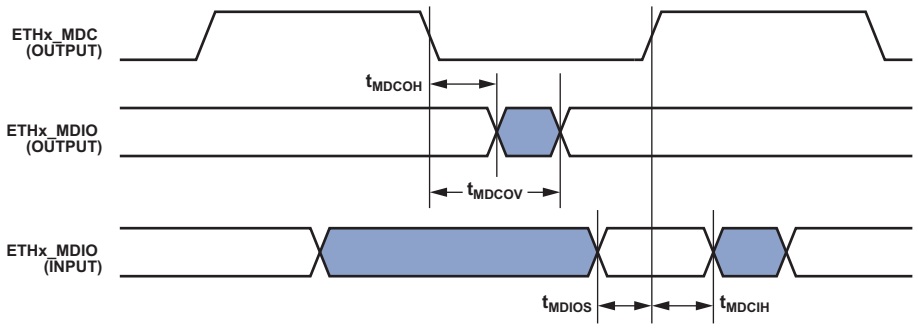


Figure 57. 10/100 Ethernet MAC Controller Timing: RMII Station Management

349-BALL CSP_BGA BALL ASSIGNMENT (ALPHABETICAL BY PIN NAME)

Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.
DMC0_A00	Y21	GND	A01	GND	N11	PB_09	C05
DMC0_A01	U22	GND	A22	GND	N12	PB_10	A04
DMC0_A02	Y22	GND	AA02	GND	N13	PB_11	B04
DMC0_A03	T20	GND	AA21	GND	N14	PB_12	C04
DMC0_A04	W20	GND	AA22	GND	N15	PB_13	K03
DMC0_A05	U21	GND	AB01	GND	P09	PB_14	L03
DMC0_A06	W21	GND	AB22	GND	P10	PB_15	M03
DMC0_A07	T21	GND	B21	GND	P11	PC_00	K01
DMC0_A08	W22	GND	C20	GND	P12	PC_01	L02
DMC0_A09	U20	GND	D12	GND	P13	PC_02	L01
DMC0_A10	R22	GND	G01	GND	P14	PC_03	M02
DMC0_A11	V22	GND	J01	GND	W11	PC_04	M01
DMC0_A12	T22	GND	J09	GND	Y03	PC_05	N02
DMC0_A13	V21	GND	J10	GND	Y20	PC_06	N01
DMC0_BA0	R21	GND	J11	GND	C03	PC_07	P02
DMC0_BA1	V20	GND	J12	GND	B02	PC_08	P01
DMC0_BA2	R20	GND	J13	$\overline{\text{JTG\_EMU}}$	E02	PC_09	R02
$\overline{\text{DMC0\_CAS}}$	E20	GND	J14	JTG_TCK	D03	PC_10	R01
DMC0_CK	M20	GND	K08	JTG_TDI	D01	PC_11	T02
DMC0_CKE	P20	GND	K09	JTG_TDO	D02	PC_12	T01
$\overline{\text{DMC0\_CK}}$	L20	GND	K10	JTG_TMS	E03	PC_13	U02
$\overline{\text{DMC0\_CS0}}$	F20	GND	K11	$\overline{\text{JTG\_TRST}}$	E01	PC_14	U01
DMC0_DQ00	M21	GND	K12	PA_00	A13	PC_15	V02
DMC0_DQ01	M22	GND	K13	PA_01	B13	PD_00	V01
DMC0_DQ02	P21	GND	K14	PA_02	A12	PD_01	W02
DMC0_DQ03	N22	GND	K15	PA_03	B12	PD_02	Y02
DMC0_DQ04	N21	GND	L08	PA_04	A11	PD_03	Y01
DMC0_DQ05	P22	GND	L09	PA_05	B11	PD_04	W01
DMC0_DQ06	L21	GND	L10	PA_06	A10	PD_05	AB02
DMC0_DQ07	L22	GND	L11	PA_07	B10	PD_06	P03
DMC0_DQ08	F22	GND	L12	PA_08	A09	PD_07	R03
DMC0_DQ09	H21	GND	L13	PA_09	B09	PD_08	T03
DMC0_DQ10	E21	GND	L14	PA_10	A08	PD_09	U03
DMC0_DQ11	J22	GND	L15	PA_11	B08	PD_10	V03
DMC0_DQ12	J21	GND	M04	PA_12	A07	PD_11	AA01
DMC0_DQ13	E22	GND	M08	PA_13	B07	PD_12	W03
DMC0_DQ14	H22	GND	M09	PA_14	A06	PD_13	AA03
DMC0_DQ15	F21	GND	M10	PA_15	B06	PD_14	AB03
DMC0_LDM	K20	GND	M11	PB_00	C12	PD_15	Y04
DMC0_LDQS	K22	GND	M12	PB_01	C11	PE_00	AA04
$\overline{\text{DMC0\_LDQS}}$	K21	GND	M13	PB_02	C10	PE_01	AB04
DMC0_ODT	J20	GND	M14	PB_03	C09	PE_02	Y05
$\overline{\text{DMC0\_RAS}}$	H20	GND	M15	PB_04	C08	PE_03	AA05
DMC0_UDM	G20	GND	M19	PB_05	C07	PE_04	AB05
DMC0_UDQS	G21	GND	N08	PB_06	C06	PE_05	Y06
$\overline{\text{DMC0\_UDQS}}$	G22	GND	N09	PB_07	A05	PE_06	Y07
$\overline{\text{DMC0\_WE}}$	N20	GND	N10	PB_08	B05	PE_07	Y08

AUTOMOTIVE PRODUCTS

The models in the following table are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the product specifications section of this data sheet carefully. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Model[1]	Max. Core Clock	Temperature Range[2]	Package Description	Package Option
ADBF606WCBCZ4xx	400 MHz	–40°C to +105°C	349-Ball CSP_BGA	BC-349-1
ADBF607WCBCZ5xx	500 MHz	–40°C to +105°C	349-Ball CSP_BGA	BC-349-1
ADBF608WCBCZ5xx	500 MHz	–40°C to +105°C	349-Ball CSP_BGA	BC-349-1
ADBF609WCBCZ5xx	500 MHz	–40°C to +105°C	349-Ball CSP_BGA	BC-349-1

[1] Z =RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 52 for the junction temperature (T_J) specification which is the only temperature specification.

ORDERING GUIDE

Model[1]	Max. Core Clock	Temperature Range[2]	Package Description	Package Option
ADSP-BF606KBCZ-4	400 MHz	0°C to +70°C	349-Ball CSP_BGA	BC-349-1
ADSP-BF606BBCZ-4	400 MHz	–40°C to +85°C	349-Ball CSP_BGA	BC-349-1
ADSP-BF607KBCZ-5	500 MHz	0°C to +70°C	349-Ball CSP_BGA	BC-349-1
ADSP-BF607BBCZ-5	500 MHz	–40°C to +85°C	349-Ball CSP_BGA	BC-349-1
ADSP-BF608KBCZ-5	500 MHz	0°C to +70°C	349-Ball CSP_BGA	BC-349-1
ADSP-BF608BBCZ-5	500 MHz	–40°C to +85°C	349-Ball CSP_BGA	BC-349-1
ADSP-BF609KBCZ-5	500 MHz	0°C to +70°C	349-Ball CSP_BGA	BC-349-1
ADSP-BF609BBCZ-5	500 MHz	–40°C to +85°C	349-Ball CSP_BGA	BC-349-1

[1] Z =RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 52 for the junction temperature (T_J) specification which is the only temperature specification.

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