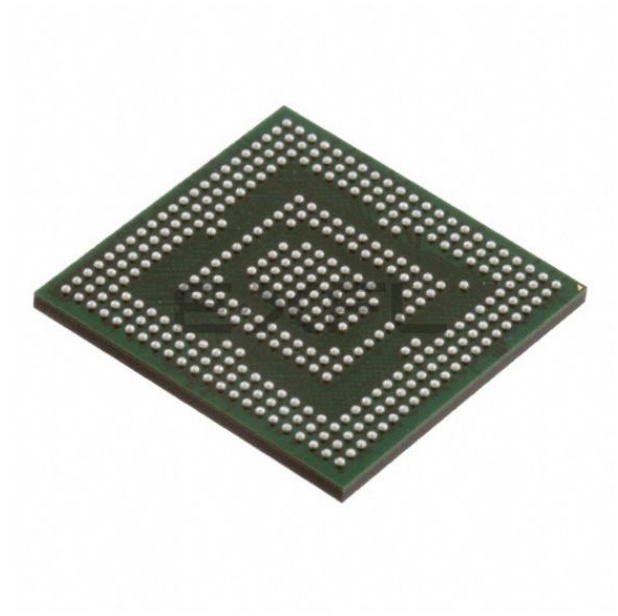

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Dual Core
Interface	CAN, EBI/EMI, Ethernet, I²C, SPI, SPORT, UART/USART, USB OTG
Clock Rate	400MHz
Non-Volatile Memory	ROM (64kB)
On-Chip RAM	552kB
Voltage - I/O	1.8V, 3.3V
Voltage - Core	1.25V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	349-LFBGA, CSPBGA
Supplier Device Package	349-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf606bbcz-4

TABLE OF CONTENTS

REVISION HISTORY

2/14—Rev. 0 to Rev. A

Added the system clock output specification and additional peripheral external clocks in Clock Related Operating Conditions on Page 53. These changes affect the following peripheral timing sections.

Enhanced Parallel Peripheral Interface Timing 74
Link Ports 78
Serial Ports—External Clock 80
Serial Peripheral Interface (SPI) Port—Master Timing 86
Serial Peripheral Interface (SPI) Port—Slave Timing 88
ADC Controller Module (ACM) Timing 96

Additional revisions include the following.

Corrected S0SEL and S1SEL in Figure 8 Clock Relationships and Divider Values 54

Revised the dynamic and static current tables CCLK Dynamic Current per core (mA, with ASF = 1) 57
Static Current—IDD_DEEPSLEEP (mA) 58

Corrected the t_{WARE} parameter in Asynchronous Page Mode Read 64

Corrected the timing diagram in Bus Request/Bus Grant . 69

Corrected the signal names in the following figures:
DDR2 SDRAM Clock and Control Cycle Timing 69
DDR2 SDRAM Controller Input AC Timing 70
Mobile DDR SDRAM Clock and Control Cycle Timing ... 72

Added Figure 29 and updated Table 42 in Enhanced Parallel Peripheral Interface Timing 74

Corrected the t_{HSPIDM}, t_{SDSCIM}, t_{SPICLK}, t_{HDSM}, and t_{SPITDM} specifications in Serial Peripheral Interface (SPI) Port—Master Timing 86

Corrected the t_{HDSPID} specification in Serial Peripheral Interface (SPI) Port—Slave Timing 88

Corrected $t_{SRDYSCKM1}$ in Serial Peripheral Interface (SPI) Port—SPI_RDY Timing 92

Revised all parameters in Timer Cycle Timing 94

Corrected the timing diagram in ADC Controller Module (ACM) Timing 96

Removed TWI signals in footnote 3 in JTAG Test And Emulation Port Timing 101

Added models to Automotive Products 112

- A 32-bit threshold block with 16 thresholds, a histogram, and run-length encoding
- Two 32-bit integral blocks that support regular and diagonal integrals
- An up- and down-scaling unit with independent scaling ratios for horizontal and vertical components
- Input and output formatters for compatibility with many data formats, including Bayer input format

The PVP can form a pipe of all the constituent algorithmic modules and is dynamically reconfigurable to form different pipeline structures.

The PVP supports the simultaneous processing of up to four data streams. The memory pipe stream operates on data received by DMA from any L1, L2, or L3 memory. The three camera pipe streams operate on a common input received directly from any of the three PPI inputs. Optionally, the PIXC can convert color data received by the PPI and forward luma values to the PVP's monochrome engine. Each stream has a dedicated DMA output. This preprocessing concept ensures careful use of available power and bandwidth budgets and frees up the processor cores for other tasks.

The PVP provides for direct core MMR access to all control/status registers. Two hardware interrupts interface to the system event controller. For optimal performance, the PVP allows register programming through its control DMA interface, as well as outputting selected status registers through the status DMA interface. This mechanism enables the PVP to automatically process job lists completely independent of the Blackfin cores.

Pixel Compositor (PIXC)

The pixel compositor (PIXC) provides image overlays with transparent-color support, alpha blending, and color space conversion capabilities for output to TFT LCDs and NTSC/PAL video encoders. It provides all of the control to allow two data streams from two separate data buffers to be combined, blended, and converted into appropriate forms for both LCD panels and digital video outputs. The main image buffer provides the basic background image, which is presented in the data stream. The overlay image buffer allows the user to add multiple foreground text, graphics, or video objects on top of the main image or video data stream.

Parallel Peripheral Interface (PPI)

The processor provides up to three parallel peripheral interfaces (PPIs), supporting data widths up to 24 bits. The PPI supports direct connection to TFT LCD panels, parallel analog-to-digital and digital-to-analog converters, video encoders and decoders, image sensor modules and other general-purpose peripherals.

The following features are supported in the PPI module:

- Programmable data length: 8 bits, 10 bits, 12 bits, 14 bits, 16 bits, 18 bits, and 24 bits per clock.
- Various framed, non-framed, and general-purpose operating modes. Frame syncs can be generated internally or can be supplied by an external device.
- ITU-656 status word error detection and correction for ITU-656 receive modes and ITU-656 preamble and status word decode.
- Optional packing and unpacking of data to/from 32 bits from/to 8 bits, 16 bits and 24 bits. If packing/unpacking is enabled, endianness can be configured to change the order of packing/unpacking of bytes/words.
- RGB888 can be converted to RGB666 or RGB565 for transmit modes.
- Various de-interleaving/interleaving modes for receiving/transmitting 4:2:2 YCrCb data.
- Configurable LCD data enable (DEN) output available on Frame Sync 3.

PROCESSOR SAFETY FEATURES

The ADSP-BF60x processor has been designed for functional safety applications. While the level of safety is mainly dominated by the system concept, the following primitives are provided by the devices to build a robust safety concept.

Dual Core Supervision

The processor has been implemented as dual-core devices to separate critical tasks to large independency. Software models support mutual supervision of the cores in symmetrical fashion.

Multi-Parity-Bit-Protected L1 Memories

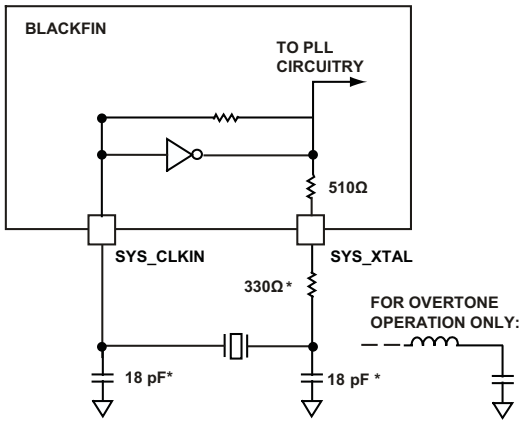
In the processor's L1 memory space, whether SRAM or cache, each word is protected by multiple parity bits to detect the single event upsets that occur in all RAMs. This applies both to L1 instruction and data memory spaces.

ECC-Protected L2 Memories

Error correcting codes (ECC) are used to correct single event upsets. The L2 memory is protected with a Single Error Correct-Double Error Detect (SEC-DED) code. By default ECC is enabled, but it can be disabled on a per-bank basis. Single-bit errors are transparently corrected. Dual-bit errors can issue a system event or fault if enabled. ECC protection is fully transparent to the user, even if L2 memory is read or written by 8-bit or 16-bit entities.

CRC-Protected Memories

While parity bit and ECC protection mainly protect against random soft errors in L1 and L2 memory cells, the CRC engines can be used to protect against systematic errors (pointer errors) and static content (instruction code) of L1, L2 and even L3 memories (DDR2, LPDDR). The processors feature two CRC engines which are embedded in the memory-to-memory DMA controllers. CRC check sums can be calculated or compared on the fly during memory transfers, or one or multiple memory regions can be continuously scrubbed by single DMA work unit as per DMA descriptor chain instructions. The CRC engine also protects data loaded during the boot process.



NOTE: VALUES MARKED WITH * MUST BE CUSTOMIZED, DEPENDING ON THE CRYSTAL AND LAYOUT. PLEASE ANALYZE CAREFULLY. FOR FREQUENCIES ABOVE 33 MHz, THE SUGGESTED CAPACITOR VALUE OF 18pF SHOULD BE TREATED AS A MAXIMUM, AND THE SUGGESTED RESISTOR VALUE SHOULD BE REDUCED TO 0 Ω.

Figure 6. External Crystal Connection

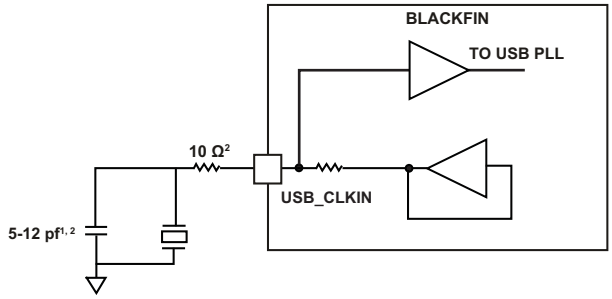
The two capacitors and the series resistor shown in Figure 6 fine tune phase and amplitude of the sine frequency. The capacitor and resistor values shown in Figure 6 are typical values only. The capacitor values are dependent upon the crystal manufacturers' load capacitance recommendations and the PCB physical layout. The resistor value depends on the drive level specified by the crystal manufacturer. The user should verify the customized values based on careful investigations on multiple devices over temperature range.

A third-overtone crystal can be used for frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone by adding a tuned inductor circuit as shown in Figure 6. A design procedure for third-overtone operation is discussed in detail in application note (EE-168) Using Third Overtone Crystals with the ADSP-218x DSP on the Analog Devices website (www.analog.com)—use site search on "EE-168."

USB Crystal Oscillator

The USB can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator. If an external clock is used, it should be a TTL compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor's USB_CLKIN pin. Alternatively, because the processor includes an on-chip oscillator circuit, an external crystal may be used.

For fundamental frequency operation, use the circuit shown in Figure 7. A parallel-resonant, fundamental frequency, microprocessor grade crystal is connected between the USB_CLKIN pin and ground. A load capacitor is placed in parallel with the crystal. The combined capacitive value of the board trace parasitic, the case capacitance of the crystal (from crystal manufacturer) and the parallel capacitor in the diagram should be in the range of 8 pF to 15 pF.



NOTES:
1. CAPACITANCE VALUE SHOWN INCLUDES BOARD PARASITICS
2. VALUES ARE A PRELIMINARY ESTIMATE.

Figure 7. External USB Crystal Connection

The crystal should be chosen so that its rated load capacitance matches the nominal total capacitance on this node. A series resistor may be added between the USB_CLKIN pin and the parallel crystal and capacitor combination, in order to further reduce the drive level of the crystal.

The parallel capacitor and the series resistor shown in Figure 7 fine tune phase and amplitude of the sine frequency. The capacitor and resistor values shown in Figure 7 are typical values only. The capacitor values are dependent upon the crystal manufacturers' load capacitance recommendations and the PCB physical layout. The resistor value depends on the drive level specified by the crystal manufacturer. The user should verify the customized values based on careful investigations on multiple devices over temperature range.

Clock Generation

The clock generation unit (CGU) generates all on-chip clocks and synchronization signals. Multiplication factors are programmed to the PLL to define the PLLCLK frequency. Programmable values divide the PLLCLK frequency to generate the core clock (CCLK), the system clocks (SYSCLK, SCLK0 and SCLK1), the LPDDR or DDR2 clock (DCLK) and the output clock (OCLK). This is illustrated in Figure 8 on Page 54.

Writing to the CGU control registers does not affect the behavior of the PLL immediately. Registers are first programmed with a new value, and the PLL logic executes the changes so that it transitions smoothly from the current conditions to the new ones.

SYS_CLKIN oscillations start when power is applied to the V_{DD_EXT} pins. The rising edge of $\overline{\text{SYS\_HWRST}}$ can be applied after all voltage supplies are within specifications (see Operating Conditions on Page 52), and SYS_CLKIN oscillations are stable.

Clock Out/External Clock

The SYS_CLKOUT output pin has programmable options to output divided-down versions of the on-chip clocks. By default, the SYS_CLKOUT pin drives a buffered version of the SYS_CLKIN input. Clock generation faults (for example PLL unlock) may trigger a reset by hardware. The clocks shown in Table 3 can be outputs from SYS_CLKOUT.

Table 6. Detailed Signal Descriptions (Continued)

Signal Name	Direction	Description
RSI_CLK	Output	**Clock** The clock signal applied to the connected device from the RSI.
RSI_CMD	I/O	**Command** Used to send commands to and receive responses from the connected device.
RSI_Dn	I/O	**Data n** Bidirectional data bus.
SMC_ABEn	Output	**Byte Enable n** Indicate whether the lower or upper byte of a memory is being accessed. When an asynchronous write is made to the upper byte of a 16-bit memory, SMC_ABE1 =0 and SMC_ABE0 =1. When an asynchronous write is made to the lower byte of a 16-bit memory, SMC_ABE1 =1 and SMC_ABE0 =0.
SMC_AMSn	Output	**Memory Select n** Typically connects to the chip select of a memory device.
SMC_Ann	Output	**Address n** Address bus.
SMC_AOE	Output	**Output Enable** Asserts at the beginning of the setup period of a read access.
SMC_ARDY	Input	**Asynchronous Ready** Flow control signal used by memory devices to indicate to the SMC when further transactions may proceed.
SMC_ARE	Output	**Read Enable** Asserts at the beginning of a read access.
SMC_AWE	Output	**Write Enable** Asserts for the duration of a write access period.
SMC_BG	Output	**Bus Grant** Output used to indicate to an external device that it has been granted control of the SMC buses.
SMC_BGH	Output	**Bus Grant Hang** Output used to indicate that the SMC has a pending transaction which requires control of the bus to be restored before it can be completed.
SMC_BR	Input	**Bus Request** Input used by an external device to indicate that it is requesting control of the SMC buses.
SMC_Dnn	I/O	**Data n** Bidirectional data bus.
SMC_NORCLK	Output	**NOR Clock** Clock for synchronous burst mode.
SMC_NORDV	Output	**NOR Data Valid** Asserts for the duration of a synchronous burst mode read setup period.
SMC_NORWT	Input	**NOR Wait** Flow control signal used by memory devices in synchronous burst mode to indicate to the SMC when further transactions may proceed.
SPI_CLK	I/O	**Clock** Input in slave mode, output in master mode.
SPI_D2	I/O	**Data 2** Used to transfer serial data in quad mode. Open drain in ODM mode.
SPI_D3	I/O	**Data 3** Used to transfer serial data in quad mode. Open drain in ODM mode.
SPI_MISO	I/O	**Master In, Slave Out** Used to transfer serial data. Operates in the same direction as SPI_MOSI in dual and quad modes. Open drain in ODM mode.
SPI_MOSI	I/O	**Master Out, Slave In** Used to transfer serial data. Operates in the same direction as SPI_MISO in dual and quad modes. Open drain in ODM mode.
SPI_RDY	I/O	**Ready** Optional flow signal. Output in slave mode, input in master mode.
SPI_SELn	Output	**Slave Select Output n** Used in master mode to enable the desired slave.
SPI_SS	Input	**Slave Select Input** Slave mode: acts as the slave select input. Master mode: optionally serves as an error detection input for the SPI when there are multiple masters.
SPT_ACLK	I/O	**Channel A Clock** Data and frame sync are driven/sampled with respect to this clock. This signal can be either internally or externally generated.
SPT_AD0	I/O	**Channel A Data 0** Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
SPT_AD1	I/O	**Channel A Data 1** Secondary bidirectional data I/O. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
SPT_AFS	I/O	**Channel A Frame Sync** The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally.
SPT_ATDV	Output	**Channel A Transmit Data Valid** This signal is optional and only active when SPORT is configured in multi-channel transmit mode. It is asserted during enabled slots.
SPT_BCLK	I/O	**Channel B Clock** Data and frame sync are driven/sampled with respect to this clock. This signal can be either internally or externally generated.
SPT_BD0	I/O	**Channel B Data 0** Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.

Table 7. ADSP-BF60x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
DMC0_DQ00	DMC Data 0	Not Muxed	DMC0_DQ00
DMC0_DQ01	DMC Data 1	Not Muxed	DMC0_DQ01
DMC0_DQ02	DMC Data 2	Not Muxed	DMC0_DQ02
DMC0_DQ03	DMC Data 3	Not Muxed	DMC0_DQ03
DMC0_DQ04	DMC Data 4	Not Muxed	DMC0_DQ04
DMC0_DQ05	DMC Data 5	Not Muxed	DMC0_DQ05
DMC0_DQ06	DMC Data 6	Not Muxed	DMC0_DQ06
DMC0_DQ07	DMC Data 7	Not Muxed	DMC0_DQ07
DMC0_DQ08	DMC Data 8	Not Muxed	DMC0_DQ08
DMC0_DQ09	DMC Data 9	Not Muxed	DMC0_DQ09
DMC0_DQ10	DMC Data 10	Not Muxed	DMC0_DQ10
DMC0_DQ11	DMC Data 11	Not Muxed	DMC0_DQ11
DMC0_DQ12	DMC Data 12	Not Muxed	DMC0_DQ12
DMC0_DQ13	DMC Data 13	Not Muxed	DMC0_DQ13
DMC0_DQ14	DMC Data 14	Not Muxed	DMC0_DQ14
DMC0_DQ15	DMC Data 15	Not Muxed	DMC0_DQ15
DMC0_LDM	DMC Data Mask for Lower Byte	Not Muxed	DMC0_LDM
DMC0_LDQS	DMC Data Strobe for Lower Byte	Not Muxed	DMC0_LDQS
$\overline{\text{DMC0\_LDQS}}$	DMC Data Strobe for Lower Byte (complement)	Not Muxed	$\overline{\text{DMC0\_LDQS}}$
DMC0_ODT	DMC On-die Termination	Not Muxed	DMC0_ODT
$\overline{\text{DMC0\_RAS}}$	DMC Row Address Strobe	Not Muxed	$\overline{\text{DMC0\_RAS}}$
DMC0_UDM	DMC Data Mask for Upper Byte	Not Muxed	DMC0_UDM
DMC0_UDQS	DMC Data Strobe for Upper Byte	Not Muxed	DMC0_UDQS
$\overline{\text{DMC0\_UDQS}}$	DMC Data Strobe for Upper Byte (complement)	Not Muxed	$\overline{\text{DMC0\_UDQS}}$
$\overline{\text{DMC0\_WE}}$	DMC Write Enable	Not Muxed	$\overline{\text{DMC0\_WE}}$
ETH0_CRS	EMAC0 Carrier Sense/RMII Receive Data Valid	C	PC_05
ETH0_MDC	EMAC0 Management Channel Clock	C	PC_06
ETH0_MDIO	EMAC0 Management Channel Serial Data	C	PC_07
ETH0_PTPPPS	EMAC0 PTP Pulse-Per-Second Output	B	PB_15
ETH0_REFCLK	EMAC0 Reference Clock	B	PB_14
ETH0_RXD0	EMAC0 Receive Data 0	C	PC_00
ETH0_RXD1	EMAC0 Receive Data 1	C	PC_01
ETH0_TXD0	EMAC0 Transmit Data 0	C	PC_02
ETH0_TXD1	EMAC0 Transmit Data 1	C	PC_03
ETH0_TXEN	EMAC0 Transmit Enable	B	PB_13
ETH1_CRS	EMAC1 Carrier Sense/RMII Receive Data Valid	E	PE_13
ETH1_MDC	EMAC1 Management Channel Clock	E	PE_10
ETH1_MDIO	EMAC1 Management Channel Serial Data	E	PE_11
ETH1_PTPPPS	EMAC1 PTP Pulse-Per-Second Output	C	PC_09
ETH1_REFCLK	EMAC1 Reference Clock	G	PG_06
ETH1_RXD0	EMAC1 Receive Data 0	G	PG_00
ETH1_RXD1	EMAC1 Receive Data 1	E	PE_15
ETH1_TXD0	EMAC1 Transmit Data 0	G	PG_03
ETH1_TXD1	EMAC1 Transmit Data 1	G	PG_02
ETH1_TXEN	EMAC1 Transmit Enable	G	PG_05
ETH_PTPAUXIN	EMAC0/EMAC1 PTP Auxiliary Trigger Input	C	PC_11

Table 7. ADSP-BF60x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SYS_BMODE2	Boot Mode Control 2	Not Muxed	SYS_BMODE2
SYS_CLKIN	Clock/Crystal Input	Not Muxed	SYS_CLKIN
SYS_CLKOUT	Processor Clock Output	Not Muxed	SYS_CLKOUT
SYS_EXTWAKE	External Wake Control	Not Muxed	SYS_EXTWAKE
SYS_FAULT	Fault Output	Not Muxed	SYS_FAULT
$\overline{\text{SYS\_FAULT}}$	Complementary Fault Output	Not Muxed	$\overline{\text{SYS\_FAULT}}$
$\overline{\text{SYS\_HWRST}}$	Processor Hardware Reset Control	Not Muxed	$\overline{\text{SYS\_HWRST}}$
$\overline{\text{SYS\_IDLE0}}$	Core 0 Idle Indicator	G	PG_15
$\overline{\text{SYS\_IDLE1}}$	Core 1 Idle Indicator	G	PG_14
$\overline{\text{SYS\_NMI}}$	Non-maskable Interrupt	Not Muxed	$\overline{\text{SYS\_NMI\_RESOUT}}$
SYS_PWRGD	Power Good Indicator	Not Muxed	SYS_PWRGD
$\overline{\text{SYS\_RESOUT}}$	Reset Output	Not Muxed	$\overline{\text{SYS\_NMI\_RESOUT}}$
$\overline{\text{SYS\_SLEEP}}$	Processor Sleep Indicator	G	PG_15
SYS_TDA	Thermal Diode Anode	Not Muxed	SYS_TDA
SYS_TDK	Thermal Diode Cathode	Not Muxed	SYS_TDK
SYS_XTAL	Crystal Output	Not Muxed	SYS_XTAL
TM0_ACI0	TIMER0 Alternate Capture Input 0	D	PD_08
TM0_ACI1	TIMER0 Alternate Capture Input 1	G	PG_14
TM0_ACI2	TIMER0 Alternate Capture Input 2	G	PG_04
TM0_ACI3	TIMER0 Alternate Capture Input 3	D	PD_07
TM0_ACI4	TIMER0 Alternate Capture Input 4	G	PG_15
TM0_ACI5	TIMER0 Alternate Capture Input 5	D	PD_06
TM0_ACI6	TIMER0 Alternate Capture Input 6	B	PB_13
TM0_ACLK0	TIMER0 Alternate Clock 0	B	PB_10
TM0_ACLK1	TIMER0 Alternate Clock 1	B	PB_12
TM0_ACLK2	TIMER0 Alternate Clock 2	B	PB_09
TM0_ACLK3	TIMER0 Alternate Clock 3	B	PB_11
TM0_ACLK4	TIMER0 Alternate Clock 4	B	PB_06
TM0_ACLK5	TIMER0 Alternate Clock 5	D	PD_13
TM0_ACLK6	TIMER0 Alternate Clock 6	D	PD_14
TM0_ACLK7	TIMER0 Alternate Clock 7	D	PD_05
TM0_CLK	TIMER0 Clock	G	PG_13
TM0_TMR0	TIMER0 Timer 0	E	PE_14
TM0_TMR1	TIMER0 Timer 1	G	PG_04
TM0_TMR2	TIMER0 Timer 2	G	PG_01
TM0_TMR3	TIMER0 Timer 3	G	PG_08
TM0_TMR4	TIMER0 Timer 4	G	PG_09
TM0_TMR5	TIMER0 Timer 5	G	PG_07
TM0_TMR6	TIMER0 Timer 6	G	PG_11
TM0_TMR7	TIMER0 Timer 7	G	PG_12
TWI0_SCL	TWI0 Serial Clock	Not Muxed	TWI0_SCL
TWI0_SDA	TWI0 Serial Data	Not Muxed	TWI0_SDA
TWI1_SCL	TWI1 Serial Clock	Not Muxed	TWI1_SCL
TWI1_SDA	TWI1 Serial Data	Not Muxed	TWI1_SDA
$\overline{\text{UART0\_CTS}}$	UART0 Clear to Send	D	PD_10
$\overline{\text{UART0\_RTS}}$	UART0 Request to Send	D	PD_09

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PD_12	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 12 | SPI1 Slave Select Output b | EPPI0 Data 20 | SPORT1 Channel A Data 1 | SPI1 Slave Select Input. Notes: No notes.
PD_13	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 13 | SPI1 Master Out, Slave In | TIMER0 Alternate Clock 5. Notes: No notes.
PD_14	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 14 | SPI1 Master In, Slave Out | TIMER0 Alternate Clock 6. Notes: No notes.
PD_15	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 15 | SPI1 Slave Select Output b | EPPI0 Data 21 | SPORT1 Channel A Data 0. Notes: No notes.
PE_00	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 0 | SPI1 Data 3 | EPPI0 Data 18 | SPORT1 Channel B Data 1. Notes: No notes.
PE_01	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 1 | SPI1 Data 2 | EPPI0 Data 19 | SPORT1 Channel B Data 0. Notes: No notes.
PE_02	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 2 | SPI1 Ready | EPPI0 Data 22 | SPORT1 Channel A Clock. Notes: No notes.
PE_03	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 3 | EPPI0 Data 16 | SPORT1 Channel B Frame Sync | ACM0 Frame Sync. Notes: No notes.
PE_04	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 4 | EPPI0 Data 17 | SPORT1 Channel B Clock | ACM0 Clock. Notes: No notes.
PE_05	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 5 | EPPI0 Data 23 | SPORT1 Channel A Frame Sync. Notes: No notes.
PE_06	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 6 | SPORT1 Channel A Transmit Data Valid | EPPI0 Frame Sync 3 (FIELD) | LP3 Clock. Notes: No notes.
PE_07	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 7 | SPORT1 Channel B Transmit Data Valid | EPPI0 Frame Sync 2 (VSYNC) | LP3 Acknowledge. Notes: No notes.
PE_08	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 8 | PWM0 Sync | EPPI0 Frame Sync 1 (HSYNC) | LP2 Acknowledge | ACM0 External Trigger 0. Notes: No notes.
PE_09	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 9 | EPPI0 Clock | LP2 Clock | PWM0 Shutdown Input. Notes: No notes.

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PG_12	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PG Position 12 | SPORT2 Channel B Data 0 | TIMER0 Timer 7 | CNT0 Count Down and Gate. Notes: No notes.
PG_13	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PG Position 13 | UART1 Clear to Send | TIMER0 Clock. Notes: No notes.
PG_14	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PG Position 14 | UART1 Receive | SYS Core 1 Idle Indicator | TIMER0 Alternate Capture Input 1. Notes: No notes.
PG_15	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PG Position 15 | UART1 Transmit | SYS Core 0 Idle Indicator | SYS Processor Sleep Indicator | TIMER0 Alternate Capture Input 4. Notes: No notes.
SMC0_A01	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Address 1. Notes: No notes.
SMC0_A02	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Address 2. Notes: No notes.
$\overline{\text{SMC0\_AMS0}}$	I/O	A	pu	pu	none	pu	none	VDD_EXT	Desc: SMC0 Memory Select 0. Notes: No notes.
$\overline{\text{SMC0\_AOE\_}}$ NORDV	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 NOR Data Valid | SMC0 Output Enable. Notes: No notes.
SMC0_ARDY_ NORWT	I/O	na	none	none	none	none	none	VDD_EXT	Desc: SMC0 NOR Wait | SMC0 Asynchronous Ready. Notes: Requires an external pull-up resistor.
$\overline{\text{SMC0\_ARE}}$	I/O	A	pu	pu	none	pu	none	VDD_EXT	Desc: SMC0 Read Enable. Notes: No notes.
$\overline{\text{SMC0\_AWE}}$	I/O	A	pu	pu	none	pu	none	VDD_EXT	Desc: SMC0 Write Enable. Notes: No notes.
$\overline{\text{SMC0\_BR}}$	I/O	na	none	none	none	none	none	VDD_EXT	Desc: SMC0 Bus Request. Notes: Requires an external pull-up resistor.
SMC0_D00	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Data 0. Notes: No notes.
SMC0_D01	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Data 1. Notes: No notes.
SMC0_D02	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Data 2. Notes: No notes.
SMC0_D03	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Data 3. Notes: No notes.
SMC0_D04	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Data 4. Notes: No notes.
SMC0_D05	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Data 5. Notes: No notes.

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
USB0_DP	I/O	F	none	none	none	none	none	VDD_USB	Desc: USB0 Data +. Notes: Pull low if not using USB. For complete documentation of hibernate behavior when USB is used, see the USB chapter in the processor hardware reference.
USB0_ID	I/O	na	none	none	none	pu	none	VDD_USB	Desc: USB0 OTG ID. Notes: If USB is not used, connect to ground. When USB is being used, the internal pull-up resistor that is present during hibernate is programmable. See the USB chapter in the processor hardware reference. Active during reset.
USB0_VBC	I/O	E	none	none	none	wk	none	VDD_USB	Desc: USB0 VBUS Control. Notes: If USB is not used, pull low.
USB0_VBUS	I/O	G	none	none	none	none	none	VDD_USB	Desc: USB0 Bus Voltage. Notes: If USB is not used, connect to ground.
VDD_DMC	s	na	none	none	none	none	none	na	Desc: VDD for DMC. Notes: If the DMC is not used, connect to VDD_INT.
VDD_EXT	s	na	none	none	none	none	none	na	Desc: External VDD. Notes: Must be powered.
VDD_INT	s	na	none	none	none	none	none	na	Desc: Internal VDD. Notes: Must be powered.
VDD_TD	s	na	none	none	none	none	none	na	Desc: VDD for Thermal Diode. Notes: If the thermal diode is not used, connect to ground.
VDD_USB	s	na	none	none	none	none	none	na	Desc: VDD for USB. Notes: If USB is not used, connect to VDD_EXT.
VREF_DMC	s	na	none	none	none	none	none	na	Desc: VREF for DMC. Notes: If the DMC is not used, connect to VDD_INT.

PROCESSOR — ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 23 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 23. Absolute Maximum Ratings

Parameter	Rating
Internal Supply Voltage (V_{DD_INT})	–0.33 V to 1.32 V
External (I/O) Supply Voltage (V_{DD_EXT})	–0.33 V to 3.63 V
Thermal Diode Supply Voltage (V_{DD_TD})	–0.33 V to 3.63 V
DDR2 Controller Supply Voltage (V_{DD_DMC})	–0.33 V to 1.90 V
USB PHY Supply Voltage (V_{DD_USB})	–0.33 V to 3.63 V
Input Voltage[1, 2, 3]	–0.33 V to 3.63 V
TWI Input Voltage[2, 4]	–0.33 V to 5.50 V
USB0_Dx Input Voltage[5]	–0.33 V to 5.25 V
USB0_VBUS Input Voltage[5]	–0.33 V to 6.00 V
DDR2 Input Voltage[6]	–0.33 V to 1.90 V
Output Voltage Swing	–0.33 V to V_{DD_EXT} + 0.5 V
I_{OH}/I_{OL} Current per Signal[1]	12.5 mA (max)
Storage Temperature Range	–65°C to +150°C
Junction Temperature Under Bias	+125°C

[1] Applies to 100% transient duty cycle.
[2] Applies only when V_{DD_EXT} is within specifications. When V_{DD_EXT} is outside specifications, the range is V_{DD_EXT} ± 0.2 V.
[3] For other duty cycles see Table 24.
[4] Applies to balls TWI_SCL and TWI_SDA.
[5] If the USB is not used, connect USB0_Dx and USB0_VBUS according to Table 15 on Page 37.
[6] Applies only when V_{DD_DMC} is within specifications. When V_{DD_DMC} is outside specifications, the range is V_{DD_DMC} ± 0.2 V.

Table 24. Maximum Duty Cycle for Input Transient Voltage[1, 2]

Maximum Duty Cycle (%)[2]	V_{IN} Min (V)[3]	V_{IN} Max (V)[3]
100	–0.33	3.63
50	–0.50	3.80
40	–0.56	3.86
25	–0.67	3.97
20	–0.73	4.03
15	–0.80	4.10
10	–0.90	4.20

[1] Applies to all signal balls with the exception of SYS_CLKIN, SYS_XTAL, SYS_EXT_WAKE, USB0_DP, USB0_DM, USB0_VBUS, TWI signals, and DMC0 signals.
[2] Applies only when V_{DD_EXT} is within specifications. When V_{DD_EXT} is outside specifications, the range is V_{DD_EXT} ± 0.2 V.
[3] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the specified voltages, and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PROCESSOR — PACKAGE INFORMATION

The information presented in Figure 9 and Table 25 provides details about package branding. For a complete listing of product availability, see Automotive Products on Page 112.

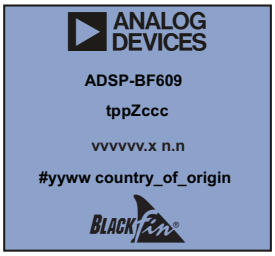


Figure 9. Product Information on Package

Table 25. Package Brand Information

Brand Key	Field Description
ADSP-BF609	Product Model
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Designation
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

Asynchronous Read

Table 28. Asynchronous Memory Read (BxMODE = b#00)

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Timing Requirements				
$t_{SDATARE}$	DATA in Setup Before $\overline{SMC0\_ARE}$ High	8.2		ns
$t_{HDATARE}$	DATA in Hold After $\overline{SMC0\_ARE}$ High	0		ns
$t_{DARDYARE}$	SMC0_ARDY Valid After $\overline{SMC0\_ARE}$ Low[1, 2]		(RAT – 2.5) × t_{SCLK0} – 17.5	ns
Switching Characteristics				
$t_{ADDRARE}$	SMC0_Ax/$\overline{SMC0\_AMSx}$ Assertion Before $\overline{SMC0\_ARE}$ Low[3]	(PREST + RST + PREAT) × t_{SCLK0} – 2		ns
t_{AOEARE}	$\overline{SMC0\_AOE}$ Assertion Before $\overline{SMC0\_ARE}$ Low	(RST + PREAT) × t_{SCLK0} – 2		ns
t_{HARE}	Output[4] Hold After $\overline{SMC0\_ARE}$ High[5]	RHT × t_{SCLK0} –2		ns
t_{WARE}	$\overline{SMC0\_ARE}$ Active Low Width[6]	RAT × t_{SCLK0} – 2		ns
$t_{DAREARDY}$	$\overline{SMC0\_ARE}$ High Delay After SMC0_ARDY Assertion[1]	2.5 × t_{SCLK0}	3.5 × t_{SCLK0} + 17.5	ns

[1] SMC0_BxCTL.ARDYEN bit = 1.
[2] RAT value set using the SMC_BxTIM.RAT bits.
[3] PREST, RST, and PREAT values set using the SMC_BxETIM.PREST bits, SMC_BxTIM.RST bits, and the SMC_BxETIM.PREAT bits.
[4] Output signals are SMC0_Ax, $\overline{SMC0\_AMS}$, $\overline{SMC0\_AOE}$, $\overline{SMC0\_ABEx}$.
[5] RHT value set using the SMC_BxTIM.RHT bits.
[6] SMC0_BxCTL.ARDYEN bit = 0.

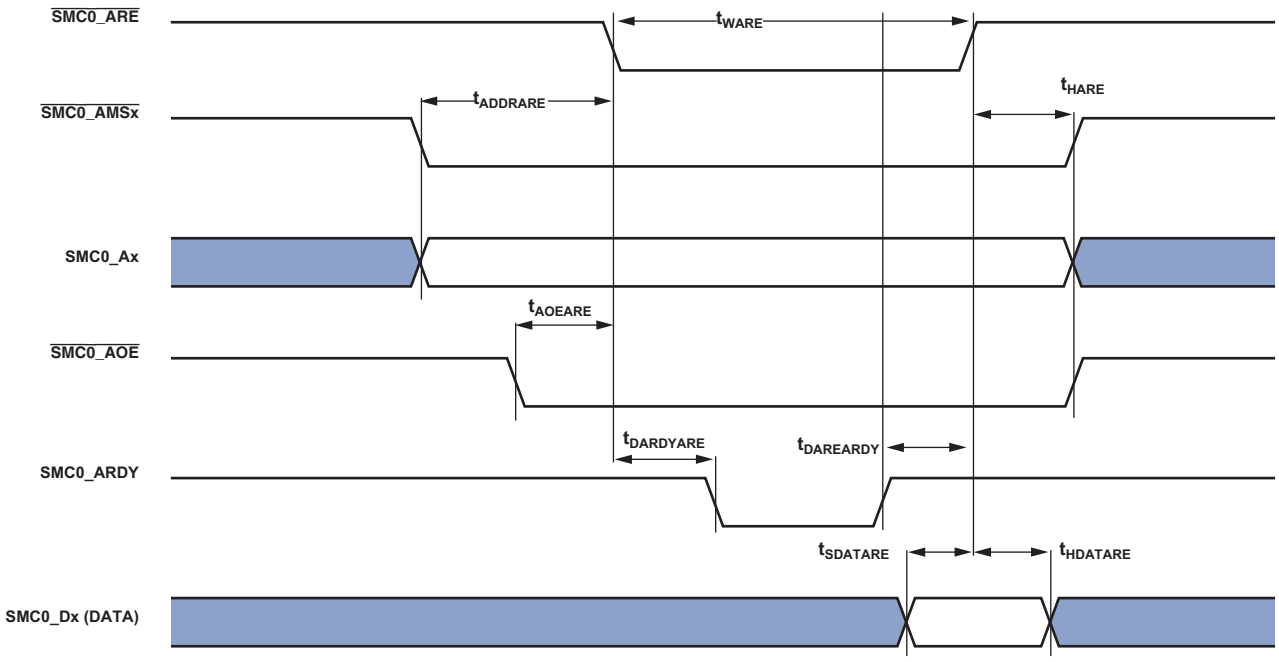


Figure 12. Asynchronous Read

Bus Request/Bus Grant

Table 35. Bus Request/Bus Grant

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Switching Characteristics				
t_{DBGBR}	$\overline{SMC0\_BG}$ Delay After $\overline{SMC0\_BR}$	2.5 × t_{SCLK0}	3.5 × t_{SCLK0} + 17.5	ns
t_{ENGDAT}	DATA Enable After $\overline{SMC0\_BG}$ Deassertion	–3		ns
t_{DBGDAT}	DATA Disable After $\overline{SMC0\_BG}$ Assertion		3	ns

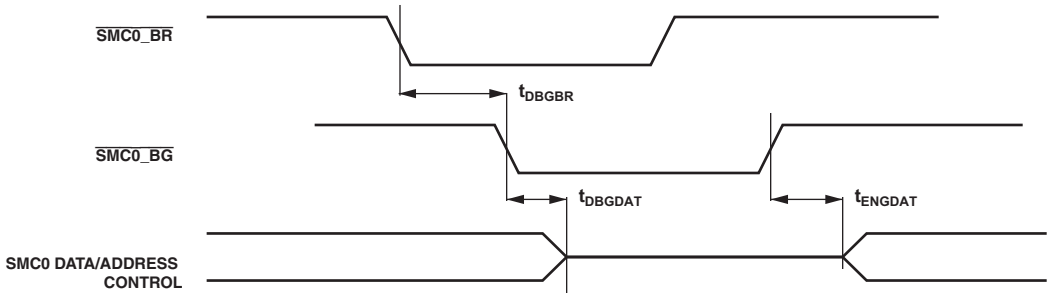
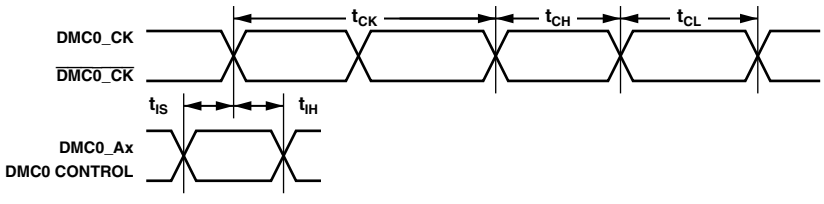


Figure 18. Bus Request/Bus Grant

DDR2 SDRAM Clock and Control Cycle Timing

Table 36. DDR2 SDRAM Read Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		250 MHz Min	Max	Unit
Switching Characteristics				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	4		ns
t_{CH}	Minimum Clock Pulse Width	0.45	0.55	t_{CK}
t_{CL}	Maximum Clock Pulse Width	0.45	0.55	t_{CK}
t_{IS}	Control/Address Setup Relative to DMC0_CK Rise	350		ps
t_{IH}	Control/Address Hold Relative to DMC0_CK Rise	475		ps



NOTE: CONTROL = $\overline{DMC0\_CS0}$, DMC0_CKE, $\overline{DMC0\_RAS}$, $\overline{DMC0\_CAS}$, AND $\overline{DMC0\_WE}$.
ADDRESS = DMC0_A00–13, AND DMC0_BA0–1.

Figure 19. DDR2 SDRAM Clock and Control Cycle Timing

DDR2 SDRAM Write Cycle Timing

Table 38. DDR2 SDRAM Write Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		250 MHz[1] Min	250 MHz[1] Max	Unit
Switching Characteristics				
t_{DQSS}[2]	DMC0_DQS Latching Rising Transitions to Associated Clock Edges	–0.15	0.15	t_{CK}
t_{DS}	Last Data Valid to DMC0_DQS Delay	0.15		ns
t_{DH}	DMC0_DQS to First Data Invalid Delay	0.3		ns
t_{DSS}	DMC0_DQS Falling Edge to Clock Setup Time	0.25		t_{CK}
t_{DSH}	DMC0_DQS Falling Edge Hold Time From DMC0_CK	0.25		t_{CK}
t_{DQSH}	DMC0_DQS Input High Pulse Width	0.35		t_{CK}
t_{DQSL}	DMC0_DQS Input Low Pulse Width	0.35		t_{CK}
t_{WPRE}	Write Preamble	0.35		t_{CK}
t_{WPST}	Write Postamble	0.4		t_{CK}
t_{IPW}	Address and Control Output Pulse Width	0.6		t_{CK}
t_{DIPW}	DMC0_DQ and DMC0_DM Output Pulse Width	0.35		t_{CK}

[1] In order to ensure proper operation of the DDR2, all the DDR2 guidelines have to be strictly followed.
[2] Write command to first DMC0_DQS delay = WL × t_{CK} + t_{DQSS}.

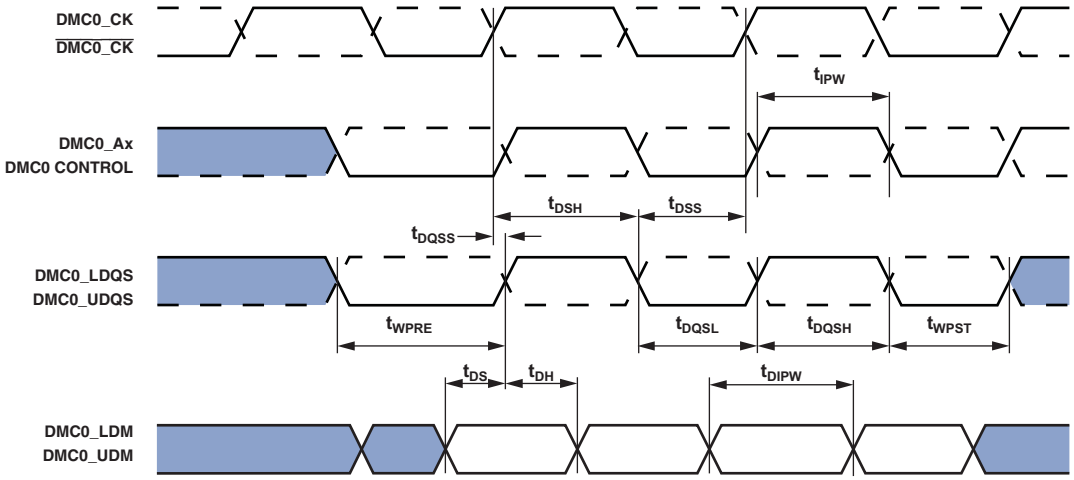


Figure 21. DDR2 SDRAM Controller Output AC Timing

Table 48. Serial Ports—Enable and Three-State

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Switching Characteristics						
t_{DDTEN}	Data Enable from External Transmit SPT_CLK[1]	1		1		ns
t_{DDTTE}	Data Disable from External Transmit SPT_CLK[1]		18.8		14	ns
t_{DDTIN}	Data Enable from Internal Transmit SPT_CLK[1]	–1		–1		ns
t_{DDTTI}	Data Disable from Internal Transmit SPT_CLK[1]		2.8		2.8	ns

[1] Referenced to drive edge.

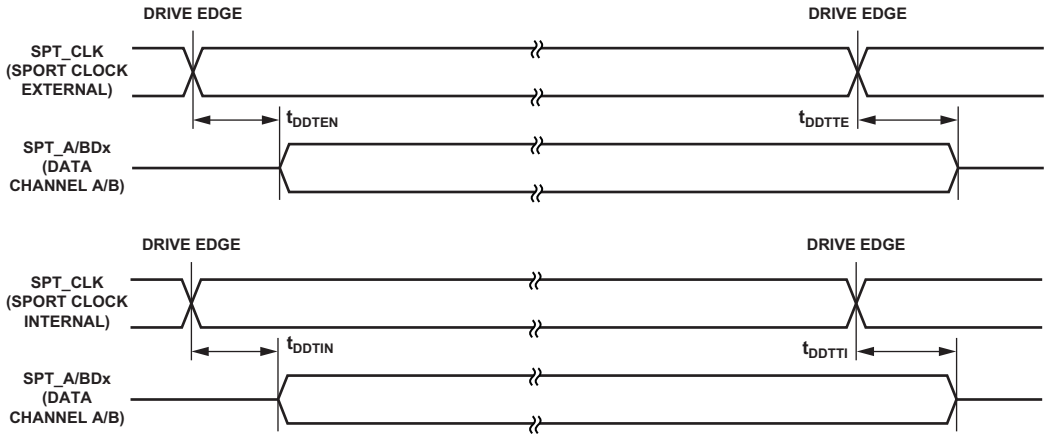


Figure 37. Serial Ports—Enable and Three-State

The SPT_TDV output signal becomes active in SPORT multi-channel mode. During transmit slots (enabled with active channel selection registers) the SPT_TDV is asserted for communication with external devices.

Table 49. Serial Ports—TDV (Transmit Data Valid)

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Switching Characteristics						
t_{DRDVEN}	Data-Valid Enable Delay from Drive Edge of External Clock[1]	2		2		ns
t_{DFDVEN}	Data-Valid Disable Delay from Drive Edge of External Clock[1]		18.8		14	ns
t_{DRDVIN}	Data-Valid Enable Delay from Drive Edge of Internal Clock[1]	–1		–1		ns
t_{DFDVIN}	Data-Valid Disable Delay from Drive Edge of Internal Clock[1]		3.5		3.5	ns

[1] Referenced to drive edge.

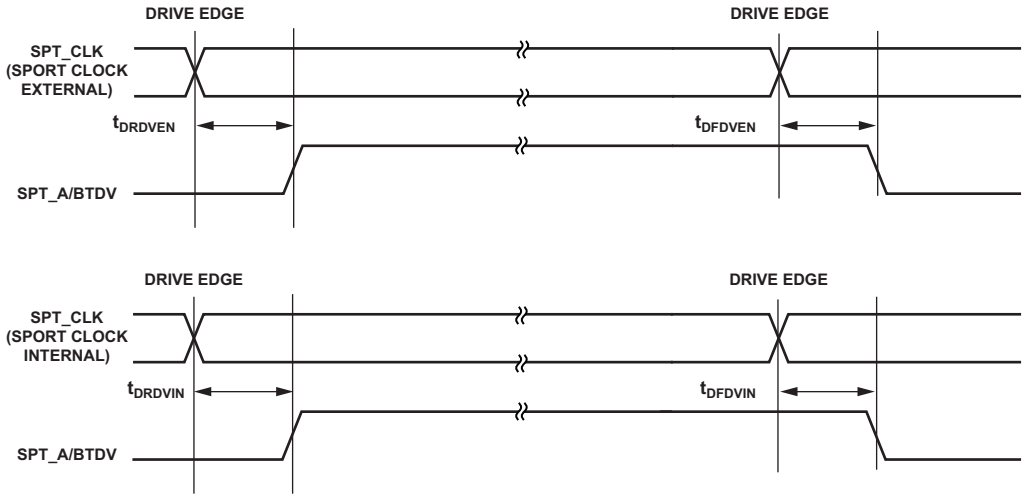


Figure 38. Serial Ports—Transmit Data Valid Internal and External Clock

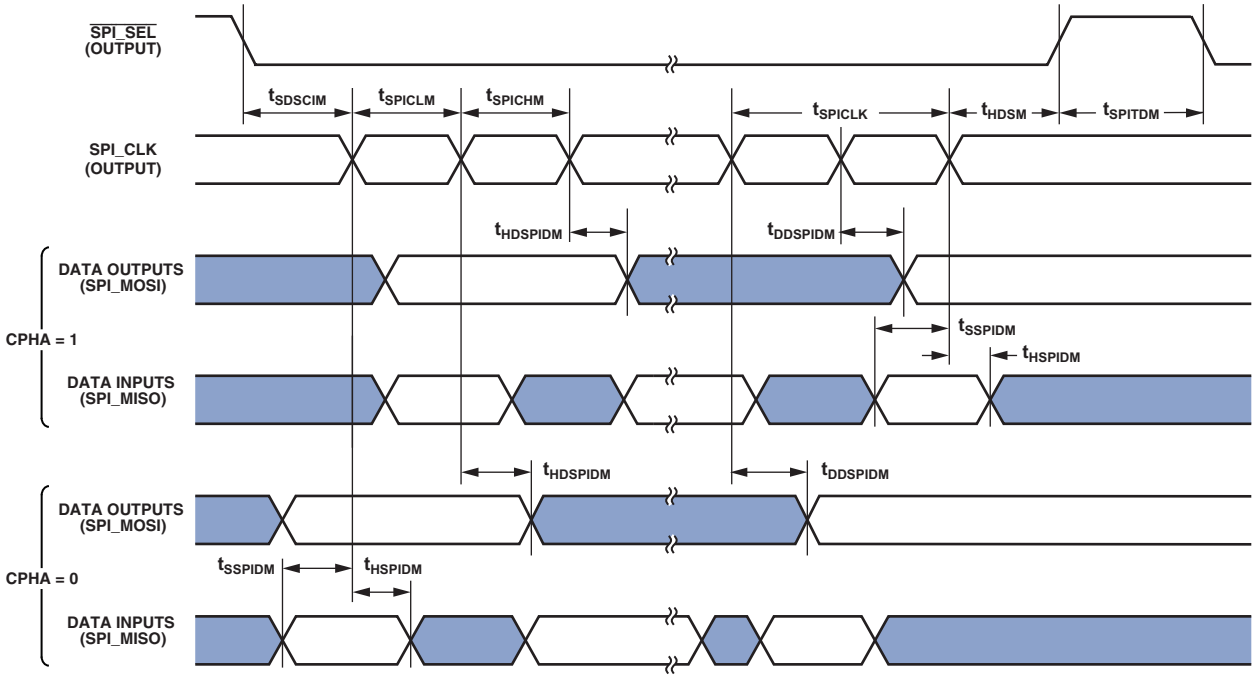


Figure 40. Serial Peripheral Interface (SPI) Port—Master Timing

Serial Peripheral Interface (SPI) Port—Slave Timing

Table 52 and Figure 41 describe SPI port slave operations. Note that:

- In dual mode data transmit the SPI_MOSI signal is also an output.
- In quad mode data transmit the SPI_MOSI, SPI_D2, and SPI_D3 signals are also outputs.
- In dual mode data receive the SPI_MISO signal is also an input.
- In quad mode data receive the SPI_MISO, SPI_D2, and SPI_D3 signals are also inputs.
- In SPI slave mode the SPI clock is supplied externally and is called $f_{SPICLKEXT}$:

$$t_{SPICLKEXT} = \frac{1}{f_{SPICLKEXT}}$$

Table 52. Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{SPICHS}	SPI_CLK High Period[1]	$(0.5 \times t_{SPICLKEXT}) - 1.5$		$(0.5 \times t_{SPICLKEXT}) - 1.5$		ns
t_{SPICLS}	SPI_CLK Low Period[1]	$(0.5 \times t_{SPICLKEXT}) - 1.5$		$(0.5 \times t_{SPICLKEXT}) - 1.5$		ns
t_{SPICLK}	SPI_CLK Period[1]	$t_{SPICLKEXT} - 1.5$		$t_{SPICLKEXT} - 1.5$		ns
t_{HDS}	Last SPI_CLK Edge to $\overline{\text{SPI\_SS}}$ Not Asserted	5		5		ns
t_{SPITDS}	Sequential Transfer Delay	$0.5 \times t_{SPICLK} - 1.5$		$0.5 \times t_{SPICLK} - 1.5$		ns
t_{SDSCI}	$\overline{\text{SPI\_SS}}$ Assertion to First SPI_CLK Edge	11.9		10.5		ns
t_{SSPID}	Data Input Valid to SPI_CLK Edge (Data Input Setup)	2.0		2.0		ns
t_{HSPID}	SPI_CLK Sampling Edge to Data Input Invalid	1.6		1.6		ns
Switching Characteristics						
t_{DSOE}	$\overline{\text{SPI\_SS}}$ Assertion to Data Out Active	0	18.8	0	14	ns
t_{DSDHI}	$\overline{\text{SPI\_SS}}$ Deassertion to Data High Impedance	0	16.3	0	12.5	ns
t_{DDSPID}	SPI_CLK Edge to Data Out Valid (Data Out Delay)		18.8		14	ns
t_{HDSPID}	SPI_CLK Edge to Data Out Invalid (Data Out Hold)	1.5		1.5		ns

[1] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPI_CLK. For the external SPI_CLK ideal maximum frequency see the $f_{SPICLKTEXT}$ specification in the Clock Related Operating Conditions table on Page 53.

Serial Peripheral Interface (SPI) Port—SPI_RDY Slave Timing

Table 53. SPI Port—SPI_RDY Slave Timing

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Switching Characteristics				
$t_{DSPISCKRDYSR}$	SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Receive	$2.5 \times t_{SCLK1}$	$3.5 \times t_{SCLK1} + 17.5$	ns
$t_{DSPISCKRDYST}$	SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Transmit	$3.5 \times t_{SCLK1}$	$4.5 \times t_{SCLK1} + 17.5$	ns

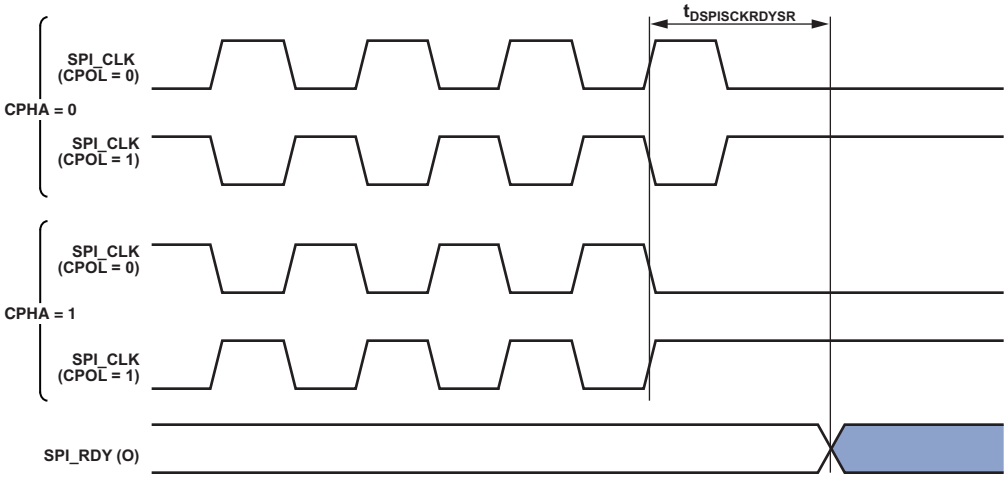


Figure 42. SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Receive (FCCH = 0)

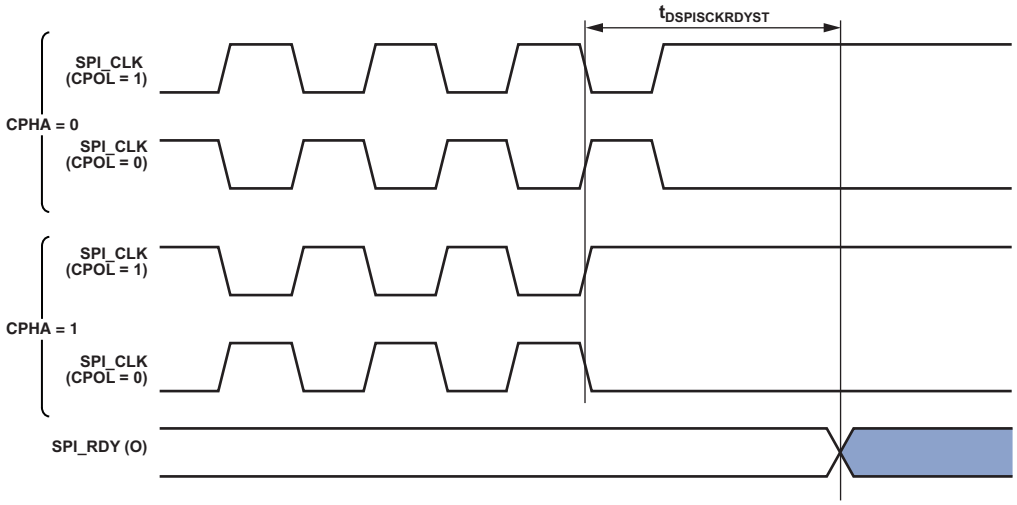


Figure 43. SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Transmit (FCCH = 1)

ADSP-BF60x 349-BALL CSP_BGA BALL ASSIGNMENTS

The 349-Ball CSP_BGA Ball Assignment (Numerical by Ball Number) table lists the CSP_BGA package by ball number for the ADSP-BF609.

The 349-Ball CSP_BGA Ball Assignment (Alphabetical by Pin Name) table lists the CSP_BGA package by signal.

349-BALL CSP_BGA BALL ASSIGNMENT (NUMERICAL BY BALL NUMBER)

Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name
A01	GND	B21	GND	F06	V_{DD_EXT}	H22	DMC0_DQ14
A02	USB0_DM	B22	$\overline{\text{SMC0_AOE}}$_NORDV	F07	V_{DD_INT}	J01	GND
A03	USB0_DP	C01	USB0_CLKIN	F08	V_{DD_INT}	J02	SYS_PWRGD
A04	PB_10	C02	USB0_VBC	F09	V_{DD_INT}	J03	SYS_BMODE0
A05	PB_07	C03	GND	F10	V_{DD_INT}	J06	V_{DD_EXT}
A06	PA_14	C04	PB_12	F11	V_{DD_EXT}	J09	GND
A07	PA_12	C05	PB_09	F12	V_{DD_EXT}	J10	GND
A08	PA_10	C06	PB_06	F13	V_{DD_INT}	J11	GND
A09	PA_08	C07	PB_05	F14	V_{DD_INT}	J12	GND
A10	PA_06	C08	PB_04	F15	V_{DD_INT}	J13	GND
A11	PA_04	C09	PB_03	F16	V_{DD_INT}	J14	GND
A12	PA_02	C10	PB_02	F17	V_{DD_DMC}	J17	V_{DD_DMC}
A13	PA_00	C11	PB_01	F20	$\overline{\text{DMC0\_CS0}}$	J20	DMC0_ODT
A14	SMC0_A01	C12	PB_00	F21	DMC0_DQ15	J21	DMC0_DQ12
A15	SMC0_D00	C13	$\overline{\text{SMC0\_BR}}$	F22	DMC0_DQ08	J22	DMC0_DQ11
A16	$\overline{\text{SMC0\_AMS0}}$	C14	SMC0_D06	G01	GND	K01	PC_00
A17	SMC0_D03	C15	SMC0_D12	G02	$\overline{\text{SYS\_HWRST}}$	K02	SYS_EXTWAKE
A18	SMC0_D04	C16	$\overline{\text{SMC0\_ARE}}$	G03	SYS_BMODE2	K03	PB_13
A19	SMC0_D07	C17	SMC0_D08	G06	V_{DD_EXT}	K06	V_{DD_EXT}
A20	SMC0_D10	C18	SMC0_D11	G07	V_{DD_EXT}	K08	GND
A21	$\overline{\text{SMC0\_AWE}}$	C19	SMC0_D14	G08	V_{DD_INT}	K09	GND
A22	GND	C20	GND	G09	V_{DD_INT}	K10	GND
B01	USB0_VBUS	C21	TWI1_SCL	G10	V_{DD_EXT}	K11	GND
B02	GND	C22	TWI0_SCL	G11	V_{DD_EXT}	K12	GND
B03	USB0_ID	D01	JTG_TDI	G12	V_{DD_EXT}	K13	GND
B04	PB_11	D02	JTG_TDO	G13	V_{DD_EXT}	K14	GND
B05	PB_08	D03	JTG_TCK	G14	V_{DD_INT}	K15	GND
B06	PA_15	D11	V_{DD_EXT}	G15	V_{DD_INT}	K17	V_{DD_DMC}
B07	PA_13	D12	GND	G16	V_{DD_DMC}	K20	DMC0_LDM
B08	PA_11	D20	SMC0_ARDY_NORWT	G17	V_{DD_DMC}	K21	$\overline{\text{DMC0\_LDQS}}$
B09	PA_09	D21	TWI1_SDA	G20	DMC0_UDM	K22	DMC0_LDQS
B10	PA_07	D22	TWI0_SDA	G21	DMC0_UDQS	L01	PC_02
B11	PA_05	E01	$\overline{\text{JTG\_TRST}}$	G22	$\overline{\text{DMC0\_UDQS}}$	L02	PC_01
B12	PA_03	E02	$\overline{\text{JTG\_EMU}}$	H01	SYS_CLKIN	L03	PB_14
B13	PA_01	E03	JTG_TMS	H02	SYS_XTAL	L04	V_{DD_EXT}
B14	SMC0_A02	E05	V_{DD_USB}	H03	SYS_BMODE1	L06	V_{DD_EXT}
B15	SMC0_D01	E20	$\overline{\text{DMC0\_CAS}}$	H06	V_{DD_EXT}	L08	GND
B16	SMC0_D15	E21	DMC0_DQ10	H07	V_{DD_EXT}	L09	GND
B17	SMC0_D09	E22	DMC0_DQ13	H16	V_{DD_DMC}	L10	GND
B18	SMC0_D02	F01	$\overline{\text{SYS\_FAULT}}$	H17	V_{DD_DMC}	L11	GND
B19	SMC0_D13	F02	SYS_FAULT	H20	$\overline{\text{DMC0\_RAS}}$	L12	GND
B20	SMC0_D05	F03	$\overline{\text{SYS\_NMI\_RESOUT}}$	H21	DMC0_DQ09	L13	GND

AUTOMOTIVE PRODUCTS

The models in the following table are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the product specifications section of this data sheet carefully. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Model[1]	Max. Core Clock	Temperature Range[2]	Package Description	Package Option
ADBF606WCBCZ4xx	400 MHz	–40°C to +105°C	349-Ball CSP_BGA	BC-349-1
ADBF607WCBCZ5xx	500 MHz	–40°C to +105°C	349-Ball CSP_BGA	BC-349-1
ADBF608WCBCZ5xx	500 MHz	–40°C to +105°C	349-Ball CSP_BGA	BC-349-1
ADBF609WCBCZ5xx	500 MHz	–40°C to +105°C	349-Ball CSP_BGA	BC-349-1

[1] Z =RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 52 for the junction temperature (T_J) specification which is the only temperature specification.

ORDERING GUIDE

Model[1]	Max. Core Clock	Temperature Range[2]	Package Description	Package Option
ADSP-BF606KBCZ-4	400 MHz	0°C to +70°C	349-Ball CSP_BGA	BC-349-1
ADSP-BF606BBCZ-4	400 MHz	–40°C to +85°C	349-Ball CSP_BGA	BC-349-1
ADSP-BF607KBCZ-5	500 MHz	0°C to +70°C	349-Ball CSP_BGA	BC-349-1
ADSP-BF607BBCZ-5	500 MHz	–40°C to +85°C	349-Ball CSP_BGA	BC-349-1
ADSP-BF608KBCZ-5	500 MHz	0°C to +70°C	349-Ball CSP_BGA	BC-349-1
ADSP-BF608BBCZ-5	500 MHz	–40°C to +85°C	349-Ball CSP_BGA	BC-349-1
ADSP-BF609KBCZ-5	500 MHz	0°C to +70°C	349-Ball CSP_BGA	BC-349-1
ADSP-BF609BBCZ-5	500 MHz	–40°C to +85°C	349-Ball CSP_BGA	BC-349-1

[1] Z =RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 52 for the junction temperature (T_J) specification which is the only temperature specification.

D10659-0-02/14(A)