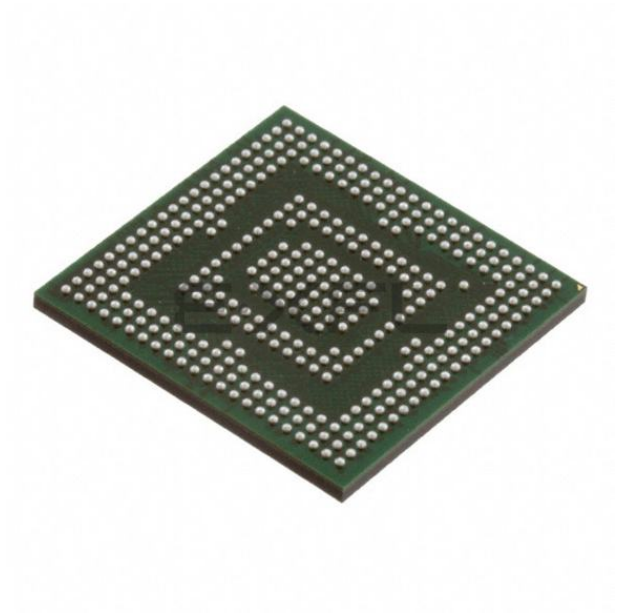

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Dual Core
Interface	CAN, EBI/EMI, Ethernet, I²C, SPI, SPORT, UART/USART, USB OTG
Clock Rate	500MHz
Non-Volatile Memory	ROM (64kB)
On-Chip RAM	808K x 8
Voltage - I/O	1.8V, 3.3V
Voltage - Core	1.25V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	349-LFBGA, CSPBGA
Supplier Device Package	349-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf608bbcz-5

Memory Protection

The Blackfin cores feature a memory protection concept, which grants data and/or instruction accesses from enabled memory regions only. A supervisor mode vs. user mode programming model supports dynamically varying access rights. Increased flexibility in memory page size options supports a simple method of static memory partitioning.

System Protection

All system resources and L2 memory banks can be controlled by either the processor cores, memory-to-memory DMA, or the system debug unit (SDU). A system protection unit (SPU) enables write accesses to specific resources that are locked to any of four masters: Core 0, Core 1, Memory DMA, and the System Debug Unit. System protection is enabled in greater granularity for some modules (L2, SEC and GPIO controllers) through a *global lock* concept.

Watchpoint Protection

The primary purpose of watchpoints and hardware breakpoints is to serve emulator needs. When enabled, they signal an emulator event whenever user-defined system resources are accessed or a core executes from user-defined addresses. Watchpoint events can be configured such that they signal the events to the other Blackfin core or to the fault management unit.

Dual Watchdog

The two on-chip watchdog timers each may supervise one Blackfin core.

Bandwidth Monitor

All DMA channels that operate in memory-to-memory mode (Memory DMA, PVP Memory Pipe DMA, PIXC DMA) are equipped with a bandwidth monitor mechanism. They can signal a system event or fault when transactions tend to starve because system buses are fully loaded with higher-priority traffic.

Signal Watchdogs

The eight general-purpose timers feature two new modes to monitor off-chip signals. The Watchdog Period mode monitors whether external signals toggle with a period within an expected range. The Watchdog Width mode monitors whether the pulse widths of external signals are in an expected range. Both modes help to detect incorrect undesired toggling (or lack thereof) of system-level signals.

Up/Down Count Mismatch Detection

The up/down counter can monitor external signal pairs, such as request/grant strobes. If the edge count mismatch exceeds the expected range, the up/down counter can flag this to the processor or to the fault management unit.

Fault Management

The fault management unit is part of the system event controller (SEC). Any system event, whether a dual-bit uncorrectable ECC error, or any peripheral status interrupt, can be defined as being a "fault". Additionally, the system events can be defined as an interrupt to the cores. If defined as such, the SEC forwards the event to the fault management unit which may automatically reset the entire device for reboot, or simply toggle the SYS_FAULT output pins to signal off-chip hardware. Optionally, the fault management unit can delay the action taken via a keyed sequence, to provide a final chance for the Blackfin cores to resolve the crisis and to prevent the fault action from being taken.

ADDITIONAL PROCESSOR PERIPHERALS

The processor contains a rich set of peripherals connected to the core via several high-bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the block diagram on Page 1). The processors contain high-speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

The following sections describe additional peripherals that were not described in the previous sections.

Timers

The processor includes several timers which are described in the following sections.

General-Purpose Timers

There is one GP timer unit and it provides eight general-purpose programmable timers. Each timer has an external pin that can be configured either as a pulse width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input on the TMRx pins, an external clock TMRCLK input pin, or to the internal SCLK0.

The timer units can be used in conjunction with the UARTs and the CAN controller to measure the width of the pulses in the data stream to provide a software auto-baud detect function for the respective serial channels.

The timers can generate interrupts to the processor core, providing periodic events for synchronization to either the system clock or to external signals. Timer events can also trigger other peripherals via the TRU (for instance, to signal a fault).

Core Timers

Each processor core also has its own dedicated timer. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generating periodic operating system interrupts.

Watchdog Timers

Each core includes a 32-bit timer, which may be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state, via generation of a hardware reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before

CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

The following publications that describe the ADSP-BF606/ADSP-BF607/ADSP-BF608/ADSP-BF609 processors (and related processors) can be ordered from any Analog Devices sales office or accessed electronically on our website:

- *Getting Started With Blackfin Processors*
- *ADSP-BF60x Blackfin Processor Hardware Reference*
- *Blackfin Processor Programming Reference*
- *ADSP-BF60x Blackfin Processor Anomaly List*

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http:\\www.analog.com\circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

Table 6. Detailed Signal Descriptions (Continued)

Signal Name	Direction	Description
RSI_CLK	Output	**Clock** The clock signal applied to the connected device from the RSI.
RSI_CMD	I/O	**Command** Used to send commands to and receive responses from the connected device.
RSI_Dn	I/O	**Data n** Bidirectional data bus.
SMC_ABEn	Output	**Byte Enable n** Indicate whether the lower or upper byte of a memory is being accessed. When an asynchronous write is made to the upper byte of a 16-bit memory, SMC_ABE1 =0 and SMC_ABE0 =1. When an asynchronous write is made to the lower byte of a 16-bit memory, SMC_ABE1 =1 and SMC_ABE0 =0.
SMC_AMSn	Output	**Memory Select n** Typically connects to the chip select of a memory device.
SMC_Ann	Output	**Address n** Address bus.
SMC_AOE	Output	**Output Enable** Asserts at the beginning of the setup period of a read access.
SMC_ARDY	Input	**Asynchronous Ready** Flow control signal used by memory devices to indicate to the SMC when further transactions may proceed.
SMC_ARE	Output	**Read Enable** Asserts at the beginning of a read access.
SMC_AWE	Output	**Write Enable** Asserts for the duration of a write access period.
SMC_BG	Output	**Bus Grant** Output used to indicate to an external device that it has been granted control of the SMC buses.
SMC_BGH	Output	**Bus Grant Hang** Output used to indicate that the SMC has a pending transaction which requires control of the bus to be restored before it can be completed.
SMC_BR	Input	**Bus Request** Input used by an external device to indicate that it is requesting control of the SMC buses.
SMC_Dnn	I/O	**Data n** Bidirectional data bus.
SMC_NORCLK	Output	**NOR Clock** Clock for synchronous burst mode.
SMC_NORDV	Output	**NOR Data Valid** Asserts for the duration of a synchronous burst mode read setup period.
SMC_NORWT	Input	**NOR Wait** Flow control signal used by memory devices in synchronous burst mode to indicate to the SMC when further transactions may proceed.
SPI_CLK	I/O	**Clock** Input in slave mode, output in master mode.
SPI_D2	I/O	**Data 2** Used to transfer serial data in quad mode. Open drain in ODM mode.
SPI_D3	I/O	**Data 3** Used to transfer serial data in quad mode. Open drain in ODM mode.
SPI_MISO	I/O	**Master In, Slave Out** Used to transfer serial data. Operates in the same direction as SPI_MOSI in dual and quad modes. Open drain in ODM mode.
SPI_MOSI	I/O	**Master Out, Slave In** Used to transfer serial data. Operates in the same direction as SPI_MISO in dual and quad modes. Open drain in ODM mode.
SPI_RDY	I/O	**Ready** Optional flow signal. Output in slave mode, input in master mode.
SPI_SELn	Output	**Slave Select Output n** Used in master mode to enable the desired slave.
SPI_SS	Input	**Slave Select Input** Slave mode: acts as the slave select input. Master mode: optionally serves as an error detection input for the SPI when there are multiple masters.
SPT_ACLK	I/O	**Channel A Clock** Data and frame sync are driven/sampled with respect to this clock. This signal can be either internally or externally generated.
SPT_AD0	I/O	**Channel A Data 0** Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
SPT_AD1	I/O	**Channel A Data 1** Secondary bidirectional data I/O. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
SPT_AFS	I/O	**Channel A Frame Sync** The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally.
SPT_ATDV	Output	**Channel A Transmit Data Valid** This signal is optional and only active when SPORT is configured in multi-channel transmit mode. It is asserted during enabled slots.
SPT_BCLK	I/O	**Channel B Clock** Data and frame sync are driven/sampled with respect to this clock. This signal can be either internally or externally generated.
SPT_BD0	I/O	**Channel B Data 0** Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.

Table 6. Detailed Signal Descriptions (Continued)

Signal Name	Direction	Description
SPT_BD1	I/O	**Channel B Data 1** Secondary bidirectional data I/O. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
SPT_BFS	I/O	**Channel B Frame Sync** The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally.
SPT_BTDV	Output	**Channel B Transmit Data Valid** This signal is optional and only active when SPORT is configured in multi-channel transmit mode. It is asserted during enabled slots.
SYS_BMODEn	Input	**Boot Mode Control n** Selects the boot mode of the processor.
SYS_CLKIN	Input	**Clock/Crystal Input** Connect to an external clock source or crystal.
SYS_CLKOUT	Output	**Processor Clock Output** Outputs internal clocks. Clocks may be divided down. See the CGU chapter in the processor hardware reference for more details.
SYS_EXTWAKE	Output	**External Wake Control** Drives low during hibernate and high all other times. Typically connected to the enable input of the voltage regulator controlling the V_{DD_INT} supply.
$\overline{\text{SYS\_FAULT}}$	I/O	**Complementary Fault** Complement of SYS_FAULT.
SYS_FAULT	I/O	**Fault** Indicates internal faults or senses external faults depending on the operating mode.
$\overline{\text{SYS\_HWRST}}$	Input	**Processor Hardware Reset Control** Resets the device when asserted.
$\overline{\text{SYS\_IDLEn}}$	Output	**Core n Idle Indicator** When low indicates that core n is in idle mode or being held in reset.
$\overline{\text{SYS\_NMI}}$	Input	**Non-maskable Interrupt** Priority depends on the core that receives the interrupt. See the processor hardware and programming references for more details.
SYS_PWRGD	Input	**Power Good Indicator** When high it indicates to the processor that the V_{DD_INT} level is within specifications such that it is safe to begin booting upon return from hibernate.
$\overline{\text{SYS\_RESOUT}}$	Output	**Reset Output** Indicates that the device is in the reset state.
$\overline{\text{SYS\_SLEEP}}$	Output	**Processor Sleep Indicator** When low indicates that the processor is in the deep sleep power saving mode.
SYS_TDA	Input	**Thermal Diode Anode** May be used by an external temperature sensor to measure the die temperature.
SYS_TDK	Input	**Thermal Diode Cathode** May be used by an external temperature sensor to measure the die temperature.
SYS_XTAL	Output	**Crystal Output** Drives an external crystal. Must be left unconnected if an external clock is driving CLKIN.
TMR_ACIn	Input	**Alternate Capture Input n** Provides an additional input for WIDCAP, WATCHDOG, and PININT modes.
TMR_ACLKn	Input	**Alternate Clock n** Provides an additional time base for use by an individual timer.
TMR_CLK	Input	**Clock** Provides an additional global time base for use by all the GP timers.
TMR_TMRn	I/O	**Timer n** The main input/output signal for each timer.
TWI_SCL	I/O	**Serial Clock** Clock output when master, clock input when slave.
TWI_SDA	I/O	**Serial Data** Receives or transmits data.
$\overline{\text{UART\_CTS}}$	Input	**Clear to Send** Flow control signal.
$\overline{\text{UART\_RTS}}$	Output	**Request to Send** Flow control signal.
$\overline{\text{UART\_RX}}$	Input	**Receive** Receive input. Typically connects to a transceiver that meets the electrical requirements of the device being communicated with.
$\overline{\text{UART\_TX}}$	Output	**Transmit** Transmit output. Typically connects to a transceiver that meets the electrical requirements of the device being communicated with.
USB_CLKIN	Input	**Clock/Crystal Input** This clock input is multiplied by a PLL to form the USB clock. See Universal Serial Bus (USB) On-The-Go—Receive and Transmit Timing for frequency/tolerance information.
USB_DM	I/O	**Data –** Bidirectional differential data line.
USB_DP	I/O	**Data +** Bidirectional differential data line.
USB_ID	Input	**OTG ID** Senses whether the controller is a host or device. This signal is pulled low when an A-type plug is sensed (signifying that the USB controller is the A device), but the input is high when a B-type plug is sensed (signifying that the USB controller is the B device).
USB_VBC	Output	**VBUS Control** Controls an external voltage source to supply VBUS when in host mode. May be configured as open drain. Polarity is configurable as well.
USB_VBUS	I/O	**Bus Voltage** Connects to bus voltage in host and device modes.

Table 7. ADSP-BF60x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SYS_BMODE2	Boot Mode Control 2	Not Muxed	SYS_BMODE2
SYS_CLKIN	Clock/Crystal Input	Not Muxed	SYS_CLKIN
SYS_CLKOUT	Processor Clock Output	Not Muxed	SYS_CLKOUT
SYS_EXTWAKE	External Wake Control	Not Muxed	SYS_EXTWAKE
SYS_FAULT	Fault Output	Not Muxed	SYS_FAULT
$\overline{\text{SYS\_FAULT}}$	Complementary Fault Output	Not Muxed	$\overline{\text{SYS\_FAULT}}$
$\overline{\text{SYS\_HWRST}}$	Processor Hardware Reset Control	Not Muxed	$\overline{\text{SYS\_HWRST}}$
$\overline{\text{SYS\_IDLE0}}$	Core 0 Idle Indicator	G	PG_15
$\overline{\text{SYS\_IDLE1}}$	Core 1 Idle Indicator	G	PG_14
$\overline{\text{SYS\_NMI}}$	Non-maskable Interrupt	Not Muxed	$\overline{\text{SYS\_NMI\_RESOUT}}$
SYS_PWRGD	Power Good Indicator	Not Muxed	SYS_PWRGD
$\overline{\text{SYS\_RESOUT}}$	Reset Output	Not Muxed	$\overline{\text{SYS\_NMI\_RESOUT}}$
$\overline{\text{SYS\_SLEEP}}$	Processor Sleep Indicator	G	PG_15
SYS_TDA	Thermal Diode Anode	Not Muxed	SYS_TDA
SYS_TDK	Thermal Diode Cathode	Not Muxed	SYS_TDK
SYS_XTAL	Crystal Output	Not Muxed	SYS_XTAL
TM0_ACI0	TIMER0 Alternate Capture Input 0	D	PD_08
TM0_ACI1	TIMER0 Alternate Capture Input 1	G	PG_14
TM0_ACI2	TIMER0 Alternate Capture Input 2	G	PG_04
TM0_ACI3	TIMER0 Alternate Capture Input 3	D	PD_07
TM0_ACI4	TIMER0 Alternate Capture Input 4	G	PG_15
TM0_ACI5	TIMER0 Alternate Capture Input 5	D	PD_06
TM0_ACI6	TIMER0 Alternate Capture Input 6	B	PB_13
TM0_ACLK0	TIMER0 Alternate Clock 0	B	PB_10
TM0_ACLK1	TIMER0 Alternate Clock 1	B	PB_12
TM0_ACLK2	TIMER0 Alternate Clock 2	B	PB_09
TM0_ACLK3	TIMER0 Alternate Clock 3	B	PB_11
TM0_ACLK4	TIMER0 Alternate Clock 4	B	PB_06
TM0_ACLK5	TIMER0 Alternate Clock 5	D	PD_13
TM0_ACLK6	TIMER0 Alternate Clock 6	D	PD_14
TM0_ACLK7	TIMER0 Alternate Clock 7	D	PD_05
TM0_CLK	TIMER0 Clock	G	PG_13
TM0_TMR0	TIMER0 Timer 0	E	PE_14
TM0_TMR1	TIMER0 Timer 1	G	PG_04
TM0_TMR2	TIMER0 Timer 2	G	PG_01
TM0_TMR3	TIMER0 Timer 3	G	PG_08
TM0_TMR4	TIMER0 Timer 4	G	PG_09
TM0_TMR5	TIMER0 Timer 5	G	PG_07
TM0_TMR6	TIMER0 Timer 6	G	PG_11
TM0_TMR7	TIMER0 Timer 7	G	PG_12
TWI0_SCL	TWI0 Serial Clock	Not Muxed	TWI0_SCL
TWI0_SDA	TWI0 Serial Data	Not Muxed	TWI0_SDA
TWI1_SCL	TWI1 Serial Clock	Not Muxed	TWI1_SCL
TWI1_SDA	TWI1 Serial Data	Not Muxed	TWI1_SDA
$\overline{\text{UART0\_CTS}}$	UART0 Clear to Send	D	PD_10
$\overline{\text{UART0\_RTS}}$	UART0 Request to Send	D	PD_09

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PA_00	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 0 | SMC0 Address 3 | EPPI2 Data 0 | LP0 Data 0. Notes: No notes.
PA_01	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 1 | SMC0 Address 4 | EPPI2 Data 1 | LP0 Data 1. Notes: No notes.
PA_02	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 2 | SMC0 Address 5 | EPPI2 Data 2 | LP0 Data 2. Notes: No notes.
PA_03	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 3 | SMC0 Address 6 | EPPI2 Data 3 | LP0 Data 3. Notes: No notes.
PA_04	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 4 | SMC0 Address 7 | EPPI2 Data 4 | LP0 Data 4. Notes: No notes.
PA_05	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 5 | SMC0 Address 8 | EPPI2 Data 5 | LP0 Data 5. Notes: No notes.
PA_06	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 6 | SMC0 Address 9 | EPPI2 Data 6 | LP0 Data 6. Notes: No notes.
PA_07	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 7 | SMC0 Address 10 | EPPI2 Data 7 | LP0 Data 7. Notes: No notes.
PA_08	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 8 | SMC0 Address 11 | EPPI2 Data 8 | LP1 Data 0. Notes: No notes.
PA_09	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 9 | SMC0 Address 12 | EPPI2 Data 9 | LP1 Data 1. Notes: No notes.
PA_10	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 10 | SMC0 Address 14 | EPPI2 Data 10 | LP1 Data 2. Notes: No notes.
PA_11	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 11 | SMC0 Address 15 | EPPI2 Data 11 | LP1 Data 3. Notes: No notes.
PA_12	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 12 | SMC0 Address 17 | EPPI2 Data 12 | LP1 Data 4. Notes: No notes.
PA_13	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 13 | SMC0 Address 18 | EPPI2 Data 13 | LP1 Data 5. Notes: No notes.
PA_14	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 14 | SMC0 Address 19 | EPPI2 Data 14 | LP1 Data 6. Notes: No notes.
PA_15	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 15 | SMC0 Address 20 | EPPI2 Data 15 | LP1 Data 7. Notes: May be used to wake the processor from hibernate or deep sleep mode.

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PB_00	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 0 | SMC0 NOR Clock | EPPI2 Clock | LP0 Clock. Notes: No notes.
PB_01	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 1 | SMC0 Memory Select 1 | EPPI2 Frame Sync 1 (HSYNC) | LP0 Acknowledge. Notes: No notes.
PB_02	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 2 | SMC0 Address 13 | EPPI2 Frame Sync 2 (VSYNC) | LP1 Acknowledge. Notes: No notes.
PB_03	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 3 | SMC0 Address 16 | EPPI2 Frame Sync 3 (FIELD) | LP1 Clock. Notes: No notes.
PB_04	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 4 | SMC0 Memory Select 2 | SMC0 Byte Enable 0 | SPORT0 Channel A Frame Sync. Notes: No notes.
PB_05	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 5 | SMC0 Memory Select 3 | SMC0 Byte Enable 1 | SPORT0 Channel A Clock. Notes: No notes.
PB_06	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 6 | SMC0 Address 21 | SPORT0 Channel A Transmit Data Valid | TIMER0 Alternate Clock 4. Notes: No notes.
PB_07	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 7 | SMC0 Address 22 | EPPI2 Data 16 | SPORT0 Channel B Frame Sync. Notes: No notes.
PB_08	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 8 | SMC0 Address 23 | EPPI2 Data 17 | SPORT0 Channel B Clock. Notes: No notes.
PB_09	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 9 | SMC0 Bus Grant Hang | SPORT0 Channel A Data 0 | TIMER0 Alternate Clock 2. Notes: No notes.
PB_10	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 10 | SMC0 Address 24 | SPORT0 Channel B Data 1 | TIMER0 Alternate Clock 0. Notes: No notes.
PB_11	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 11 | SMC0 Address 25 | SPORT0 Channel B Data 0 | TIMER0 Alternate Clock 3. Notes: No notes.
PB_12	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 12 | SMC0 Bus Grant | SPORT0 Channel B Transmit Data Valid | SPORT0 Channel A Data 1 | TIMER0 Alternate Clock 1. Notes: No notes.

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PC_13	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PC Position 13 | SPI0 Slave Select Output b | EPPI1 Data 13 | ETH PTP Clock Input. Notes: No notes.
PC_14	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PC Position 14 | SPI1 Slave Select Output b | EPPI1 Data 14. Notes: No notes.
PC_15	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PC Position 15 | SPI0 Slave Select Output b | EPPI1 Data 15. Notes: May be used to wake the processor from hibernate or deep sleep mode.
PD_00	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 0 | SPI0 Data 2 | EPPI1 Data 16 | SPI0 Slave Select Output b. Notes: No notes.
PD_01	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 1 | SPI0 Data 3 | EPPI1 Data 17 | SPI0 Slave Select Output b. Notes: No notes.
PD_02	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 2 | SPI0 Master In, Slave Out. Notes: No notes.
PD_03	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 3 | SPI0 Master Out, Slave In. Notes: No notes.
PD_04	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 4 | SPI0 Clock. Notes: No notes.
PD_05	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 5 | SPI1 Clock | TIMER0 Alternate Clock 7. Notes: No notes.
PD_06	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 6 | EPPI1 Frame Sync 2 (VSYNC) | ETH0 RMII Management Data Interrupt | TIMER0 Alternate Capture Input 5. Notes: May be used to wake the processor from hibernate or deep sleep mode.
PD_07	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 7 | UART0 Transmit | TIMER0 Alternate Capture Input 3. Notes: No notes.
PD_08	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 8 | UART0 Receive | TIMER0 Alternate Capture Input 0. Notes: No notes.
PD_09	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 9 | SPI1 Slave Select Output b | UART0 Request to Send | SPI0 Slave Select Output b. Notes: No notes.
PD_10	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 10 | SPI0 Ready | UART0 Clear to Send | SPI1 Slave Select Output b. Notes: No notes.
PD_11	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 11 | SPI0 Slave Select Output b | SPI0 Slave Select Input. Notes: No notes.

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PD_12	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 12 | SPI1 Slave Select Output b | EPPI0 Data 20 | SPORT1 Channel A Data 1 | SPI1 Slave Select Input. Notes: No notes.
PD_13	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 13 | SPI1 Master Out, Slave In | TIMER0 Alternate Clock 5. Notes: No notes.
PD_14	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 14 | SPI1 Master In, Slave Out | TIMER0 Alternate Clock 6. Notes: No notes.
PD_15	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 15 | SPI1 Slave Select Output b | EPPI0 Data 21 | SPORT1 Channel A Data 0. Notes: No notes.
PE_00	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 0 | SPI1 Data 3 | EPPI0 Data 18 | SPORT1 Channel B Data 1. Notes: No notes.
PE_01	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 1 | SPI1 Data 2 | EPPI0 Data 19 | SPORT1 Channel B Data 0. Notes: No notes.
PE_02	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 2 | SPI1 Ready | EPPI0 Data 22 | SPORT1 Channel A Clock. Notes: No notes.
PE_03	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 3 | EPPI0 Data 16 | SPORT1 Channel B Frame Sync | ACM0 Frame Sync. Notes: No notes.
PE_04	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 4 | EPPI0 Data 17 | SPORT1 Channel B Clock | ACM0 Clock. Notes: No notes.
PE_05	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 5 | EPPI0 Data 23 | SPORT1 Channel A Frame Sync. Notes: No notes.
PE_06	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 6 | SPORT1 Channel A Transmit Data Valid | EPPI0 Frame Sync 3 (FIELD) | LP3 Clock. Notes: No notes.
PE_07	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 7 | SPORT1 Channel B Transmit Data Valid | EPPI0 Frame Sync 2 (VSYNC) | LP3 Acknowledge. Notes: No notes.
PE_08	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 8 | PWM0 Sync | EPPI0 Frame Sync 1 (HSYNC) | LP2 Acknowledge | ACM0 External Trigger 0. Notes: No notes.
PE_09	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 9 | EPPI0 Clock | LP2 Clock | PWM0 Shutdown Input. Notes: No notes.

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PF_03	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 3 | PWM0 Channel B High Side | EPPI0 Data 3 | LP2 Data 3. Notes: No notes.
PF_04	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 4 | PWM0 Channel C Low Side | EPPI0 Data 4 | LP2 Data 4. Notes: No notes.
PF_05	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 5 | PWM0 Channel C High Side | EPPI0 Data 5 | LP2 Data 5. Notes: No notes.
PF_06	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 6 | PWM0 Channel D Low Side | EPPI0 Data 6 | LP2 Data 6. Notes: No notes.
PF_07	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 7 | PWM0 Channel D High Side | EPPI0 Data 7 | LP2 Data 7. Notes: No notes.
PF_08	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 8 | SPI1 Slave Select Output b | EPPI0 Data 8 | LP3 Data 0. Notes: No notes.
PF_09	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 9 | SPI1 Slave Select Output b | EPPI0 Data 9 | LP3 Data 1. Notes: No notes.
PF_10	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 10 | ACM0 Address 4 | EPPI0 Data 10 | LP3 Data 2. Notes: No notes.
PF_11	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 11 | EPPI0 Data 11 | LP3 Data 3 | PWM0 Shutdown Input. Notes: No notes.
PF_12	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 12 | ACM0 Address 2 | EPPI0 Data 12 | LP3 Data 4. Notes: No notes.
PF_13	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 13 | ACM0 Address 3 | EPPI0 Data 13 | LP3 Data 5. Notes: No notes.
PF_14	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 14 | EPPI0 Data 14 | ACM0 Address 0 | LP3 Data 6. Notes: No notes.
PF_15	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 15 | ACM0 Address 1 | EPPI0 Data 15 | LP3 Data 7. Notes: No notes.
PG_00	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PG Position 0 | PWM1 Channel B High Side | RSI0 Data 2 | ETH1 Receive Data 0. Notes: Has an optional internal pull-up resistor for use with RSI. See the RSI chapter in the processor hardware reference for more details.
PG_01	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PG Position 1 | SPORT2 Channel A Frame Sync | TIMER0 Timer 2 | CAN0 Transmit. Notes: No notes.

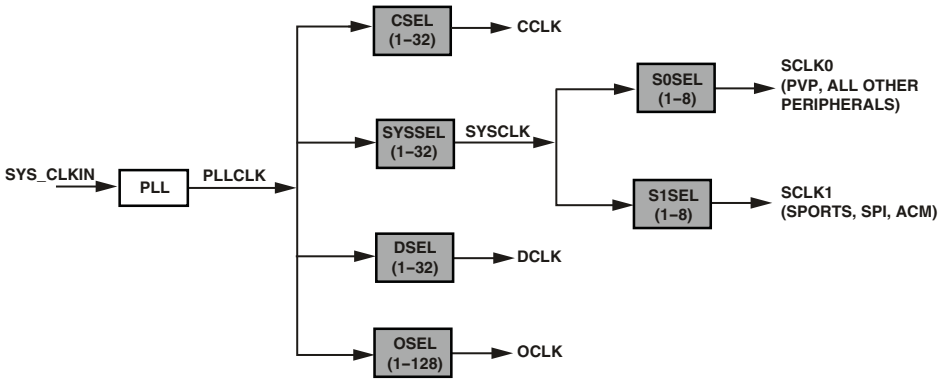
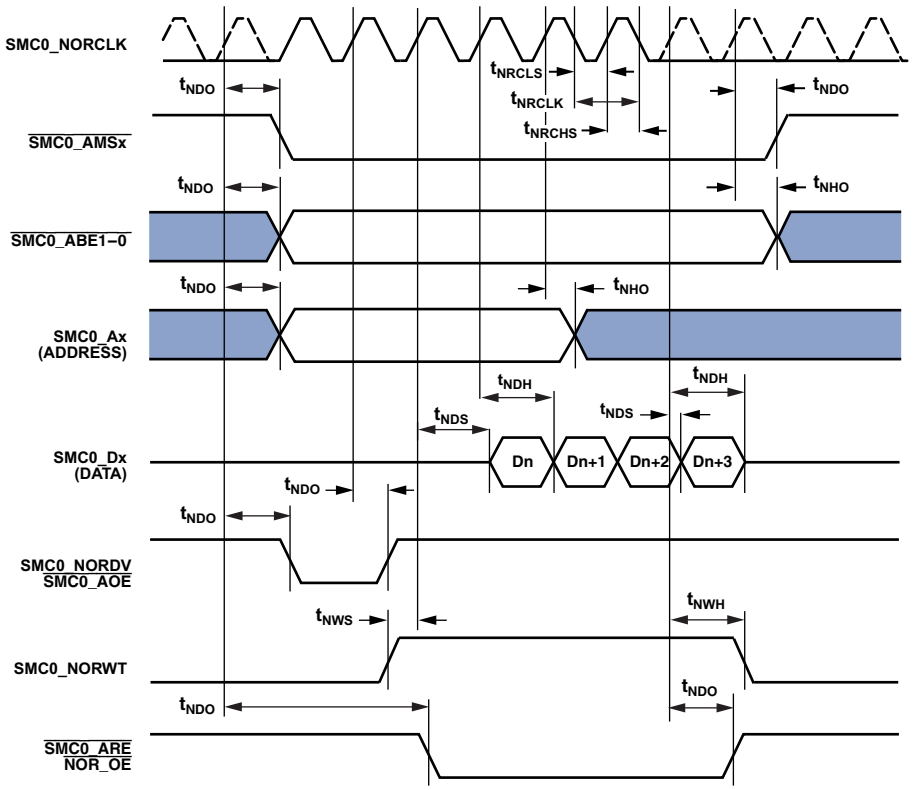


Figure 8. Clock Relationships and Divider Values

Parameter		Test Conditions	Min	Typical	Max	Unit
I_{DD_IDLE}[23]	V_{DD_INT} Current in Idle	f_{CCLK} = 500 MHz ASFC0 = 0.14 (Idle) ASFC1 = 0 (Disabled) f_{SYSCLK} = 250 MHz, $f_{SCLK0/1}$ = 125 MHz f_{DCLK} = 0 MHz (DDR Disabled) f_{USBCLK} = 0 MHz (USB Disabled) No PVP or DMA activity T_J = 25°C		137		mA
I_{DD_TYP}[23]	V_{DD_INT} Current	f_{CCLK} = 500 MHz ASFC0 = 1.0 (Full-on Typical) ASFC1 = 0.86 (App) f_{SYSCLK} = 250 MHz, $f_{SCLK0/1}$ = 125 MHz f_{DCLK} = 250 MHz f_{USBCLK} = 0 MHz (USB Disabled) DMA Data Rate = 124 MB/s Medium PVP Activity T_J = 25°C		357		mA
$I_{DD\_HIBERNATE}$[22, 24]	Hibernate State Current	V_{DD_INT} = 0 V, V_{DD_EXT} = V_{DD_TD} = V_{DD_USB} = 3.3 V, V_{DD_DMC} = 1.8 V, V_{REF_DMC} = 0.9 V, T_J = 25°C, f_{CLKIN} = 0 MHz		40		µA
$I_{DD\_HIBERNATE}$[22, 24]	Hibernate State Current Without USB	V_{DD_INT} = 0 V, V_{DD_EXT} = V_{DD_TD} = V_{DD_USB} = 3.3 V, V_{DD_DMC} = 1.8 V, V_{REF_DMC} = 0.9 V, T_J = 25°C, f_{CLKIN} = 0 MHz, USB protection disabled (USB0_PHY_CTL.DIS=1)		10		µA
I_{DD_INT}[23]	V_{DD_INT} Current	f_{CCLK} > 0 MHz $f_{SCLK0/1}$ ≥ 0 MHz			See I_{DDINT_TOT} equation on Page 57	mA

[1] Applies to all output and bidirectional signals except DMC0 signals, TWI signals and USB0 signals.
[2] Applies to all DMC0 output and bidirectional signals in DDR2 full drive strength mode.
[3] Applies to all DMC0 output and bidirectional signals in DDR2 half drive strength mode.
[4] Applies to all DMC0 output and bidirectional signals in LPDDR full drive strength mode.
[5] Applies to all DMC0 output and bidirectional signals in LPDDR three-quarter drive strength mode.
[6] Applies to all DMC0 output and bidirectional signals in LPDDR half drive strength mode.
[7] Applies to all DMC0 output and bidirectional signals in LPDDR one-quarter drive strength mode.
[8] Applies to all output and bidirectional signals except DMC0 signals and USB0 signals.
[9] Applies to signals SMC0_ARDY, $\overline{\text{SMC0\_BR}}$, SYS_BMODE0–2, SYS_CLKIN, SYS_HWRST, SYS_PWRGD, JTG_TDI, and $\overline{\text{JTG\_TMS}}$.
[10] Applies to signals JTG_TCK and $\overline{\text{JTG\_TRST}}$.
[11] Applies to signals SMC0_ARDY, $\overline{\text{SMC0\_BR}}$, SYS_BMODE0–2, SYS_CLKIN, SYS_HWRST, SYS_PWRGD, JTG_TCK, and $\overline{\text{JTG\_TRST}}$.
[12] Applies to signals JTG_TDI, JTG_TMS.
[13] Applies to signal USB0_CLKIN.
[14] Applies to signals PA0–15, PB0–15, PC0–15, PD0–15, PE0–15, PF0–15, PG0–15, $\overline{\text{SMC0\_AMS0}}$, $\overline{\text{SMC0\_ARE}}$, $\overline{\text{SMC0\_AWE}}$, $\overline{\text{SMC0\_A0E}}$, SMC0_A01–02, SMC0_D00–15, SYS_FAULT, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{JTG\_EMU}}$, JTG_TDO, USB0_DM, USB0_DP, USB0_ID, USB0_VBC, USB0_VBUS.
[15] Applies to DMC0_A[00:13], $\overline{\text{DMC0\_BA}}$[0:2], $\overline{\text{DMC0\_CAS}}$, $\overline{\text{DMC0\_CS0}}$, DMC0_DQ[00:15], DMC0_LQDS, $\overline{\text{DMC0\_LDQS}}$, DMC0_UDQS, $\overline{\text{DMC0\_UDQS}}$, DMC0_LDM, DMC0_UDM, DMC0_ODT, $\overline{\text{DMC0\_RAS}}$, and $\overline{\text{DMC0\_WE}}$.
[16] Applies to signals PA0–15, PB0–15, PC0–15, PD0–15, PE0–15, PF0–15, PG0–15, $\overline{\text{SMC0\_A0E}}$, SMC0_A01–02, SMC0_D00–15, SYS_FAULT, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{JTG\_EMU}}$, JTG_TDO, USB0_DM, USB0_DP, USB0_ID, USB0_VBC, USB0_VBUS, DMC0_A00–13, DMC0_BA0–2, $\overline{\text{DMC0\_CAS}}$, $\overline{\text{DMC0\_CS0}}$, DMC0_DQ00–15, DMC0_LQDS, $\overline{\text{DMC0\_LDQS}}$, DMC0_UDQS, $\overline{\text{DMC0\_UDQS}}$, DMC0_LDM, DMC0_UDM, DMC0_ODT, $\overline{\text{DMC0\_RAS}}$, $\overline{\text{DMC0\_WE}}$, and TWI signals.
[17] Applies to signals $\overline{\text{SMC0\_AMS0}}$, $\overline{\text{SMC0\_ARE}}$, $\overline{\text{SMC0\_AWE}}$, and when RSI pull-up resistors are enabled, PE10–13, 15 and PG00, 02, 03, 05.
[18] Applies to all TWI signals.
[19] Applies to all signals, except DMC0 and TWI signals.
[20] Guaranteed, but not tested.
[21] Applies to all DMC0 signals.
[22] See the *ADSP-BF60x Blackfin Processor Hardware Reference Manual* for definition of deep sleep and hibernate operating modes.
[23] Additional information can be found at Total Internal Power Dissipation on Page 57.
[24] Applies to V_{DD_EXT}, V_{DD_DMC}, V_{DD_USB} and V_{DD_TD} supply signals only. Clock inputs are tied high or low.



NOTE: SMC0_NORCLK dotted line represents a free running version of SMC0_NORCLK that is not visible on the SMC0_NORCLK pin.

Figure 15. Synchronous Burst AC Interface Timing

Link Ports

In link port receive mode the link port clock is supplied externally and is called $f_{LCLKREXT}$:

$$t_{LCLKREXT} = \frac{1}{f_{LCLKREXT}}$$

In link port transmit mode the programmed link port clock ($f_{LCLKTPROG}$) frequency in MHz is set by the following equation where VALUE is a field in the LP_DIV register that can be set from 1 to 255:

$$f_{LCLKTPROG} = \frac{f_{SCLK0}}{(VALUE \times 2)}$$

In the case where VALUE = 0, $f_{LCLKTPROG} = f_{SCLK0}$. For all settings of VALUE the following equation also holds:

$$t_{LCLKTPROG} = \frac{1}{f_{LCLKTPROG}}$$

Calculation of link receiver data setup and hold relative to link clock is required to determine the maximum allowable skew that can be introduced in the transmission path length difference between LP_Dx (data) and LP_CLK. Setup skew is the maximum delay that can be introduced in LP_Dx relative to LP_CLK:
(setup skew = $t_{LCLKTWH}$ min – t_{DLDCH} – t_{SLDCL}). Hold skew is the maximum delay that can be introduced in LP_CLK relative to LP_Dx: (hold skew = $t_{LCLKTWL}$ min – t_{HLDCH} – t_{HLDCL}).

Table 44. Link Ports—Receive

Parameter		V_{DD_EXT} 1.8 V Nominal/3.3 V Nominal Min	Max	Unit
Timing Requirements				
t_{SLDCL}	Data Setup Before LP_CLK Low	2		ns
t_{HLDCL}	Data Hold After LP_CLK Low	3		ns
t_{LCLKIW}	LP_CLK Period[1]	$t_{LCLKREXT}$ – 1.5		ns
$t_{LCLKRWL}$	LP_CLK Width Low[1]	(0.5 × $t_{LCLKREXT}$) – 1.5		ns
$t_{LCLKRWH}$	LP_CLK Width High[1]	(0.5 × $t_{LCLKREXT}$) – 1.5		ns
Switching Characteristic				
t_{DLALC}	LP_ACK Low Delay After LP_CLK Low[2]	1.5 × t_{SCLK0} + 4	2.5 × t_{SCLK0} + 12	ns

[1] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external LP_CLK. For the external LP_CLK ideal maximum frequency see the $f_{LCLKTEXT}$ specification in Table 17 on Page 53 in Clock Related Operating Conditions.
[2] LP_ACK goes low with t_{DLALC} relative to rise of LP_CLK after first byte, but does not go low if the receiver's link buffer is not about to fill.

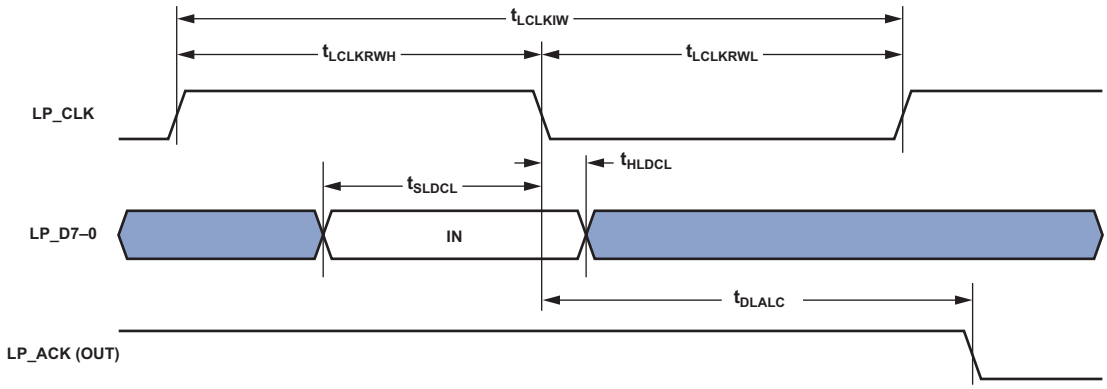


Figure 34. Link Ports—Receive

ADC Controller Module (ACM) Timing

Table 61 and Figure 53 describe ACM operations.

When internally generated, the programmed ACM clock ($f_{ACLKPROG}$) frequency in MHz is set by the following equation where CKDIV is a field in the ACM_TC0 register and ranges from 1 to 255:

$$f_{ACLKPROG} = \frac{f_{SCLK1}}{CKDIV + 1}$$

$$t_{ACLKPROG} = \frac{1}{f_{ACLKPROG}}$$

Setup cycles (SC) in Table 61 is also a field in the ACM_TC0 register and ranges from 0 to 4095. Hold Cycles (HC) is a field in the ACM_TC1 register that ranges from 0 to 15.

Table 61. ACM Timing

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Timing Requirements				
t_{SDR}	SPORT DRxPRI/DRxSEC Setup Before ACMx_CLK	3		ns
t_{HDR}	SPORT DRxPRI/DRxSEC Hold After ACMx_CLK	1.5		ns
Switching Characteristics				
t_{SCTLCS}	ACM Controls (ACMx_A[4:0]) Setup Before Assertion of $\overline{CS}$	(SC + 1) × t_{SCLK1} – 3		ns
t_{HCTLCS}	ACM Control (ACMx_A[4:0]) Hold After De-assertion of $\overline{CS}$	HC × t_{ACLK} + 0.1		ns
t_{ACLKW}	ACM Clock Pulse Width[1]	(0.5 × $t_{ACLKPROG}$) – 1.5		ns
t_{ACLK}	ACM Clock Period[1]	$t_{ACLKPROG}$ – 1.5		ns
$t_{HCSACLK}$	$\overline{CS}$ Hold to ACMx_CLK Edge	–0.1		ns
$t_{SCSACLK}$	$\overline{CS}$ Setup to ACMx_CLK Edge	t_{ACLK} – 3.5		ns

[1] See Table 17 on Page 53 in Clock Related Operating Conditions for details on the minimum period that may be programmed for $t_{ACLKPROG}$.

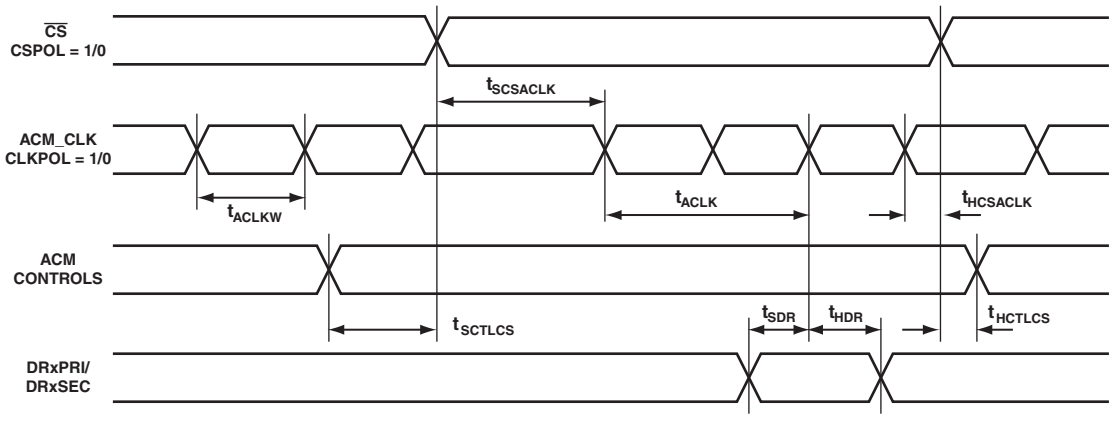


Figure 53. ACM Timing

Table 66. 10/100 Ethernet MAC Controller Timing: RMII Station Management

Parameter[1]		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Timing Requirements				
t_{MDIOS}	ETHx_MDIO Input Valid to ETHx_MDC Rising Edge (Setup)	14		ns
t_{MDCIH}	ETHx_MDC Rising Edge to ETHx_MDIO Input Invalid (Hold)	0		ns
Switching Characteristics				
t_{MDCOV}	ETHx_MDC Falling Edge to ETHx_MDIO Output Valid		t_{SCLK0} + 5	ns
t_{MDCOH}	ETHx_MDC Falling Edge to ETHx_MDIO Output Invalid (Hold)	t_{SCLK0} −1		ns

[1] ETHx_MDC/ETHx_MDIO is a 2-wire serial bidirectional port for controlling one or more external PHYs. ETHx_MDC is an output clock whose minimum period is programmable as a multiple of the system clock SCLK0. ETHx_MDIO is a bidirectional data line.

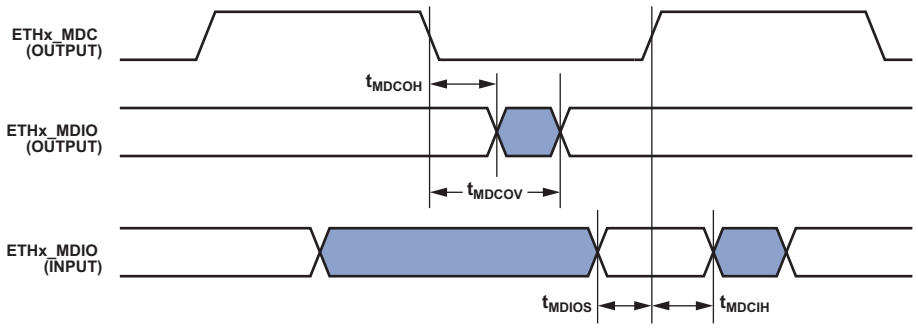


Figure 57. 10/100 Ethernet MAC Controller Timing: RMII Station Management

JTAG Test And Emulation Port Timing

Table 67 and Figure 58 describe JTAG port operations.

Table 67. JTAG Port Timing

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{TCK}	JTG_TCK Period	20		20		ns
t_{STAP}	JTG_TDI, JTG_TMS Setup Before JTG_TCK High	4		4		ns
t_{HTAP}	JTG_TDI, JTG_TMS Hold After JTG_TCK High	4		4		ns
t_{SSYS}	System Inputs Setup Before JTG_TCK High[1]	12		12		ns
t_{HSYS}	System Inputs Hold After JTG_TCK High[1]	5		5		ns
t_{TRSTW}	$\overline{\text{JTG\_TRST}}$ Pulse Width (measured in JTG_TCK cycles)[2]	4		4		T_{CK}
Switching Characteristics						
t_{DTDO}	JTG_TDO Delay from JTG_TCK Low		18		13.5	ns
t_{DSYS}	System Outputs Delay After JTG_TCK Low[3]		22		17	ns

[1] System Inputs = DMC0_DQ00–15, DMC0_LDQS, $\overline{\text{DMC0\_LDQS}}$, DMC0_UDQS, $\overline{\text{DMC0\_UDQS}}$, PA_15–0, PB_15–0, PC_15–0, PD_15–0, PE_15–0, PF_15–0, PG_15–0, SMC0_ARDY_NORWT, $\overline{\text{SMC0\_BR}}$, SMC0_D15–0, SYS_BMODE0–2, $\overline{\text{SYS\_HWRST}}$, SYS_FAULT, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{SYS\_NMI\_RESOUT}}$, SYS_PWRGD, TWI0_SCL, TWI0_SDA, TWI1_SCL, TWI1_SDA.

[2] 50 MHz Maximum.

[3] System Outputs = DMC0_A00–13, DMC0_BA0–2, $\overline{\text{DMC0\_CAS}}$, DMC0_CK, $\overline{\text{DMC0\_CK}}$, DMC0_CKE, $\overline{\text{DMC0\_CS0}}$, DMC0_DQ00–15, DMC0_LDM, DMC0_LDQS, $\overline{\text{DMC0\_LDQS}}$, DMC0_ODT, $\overline{\text{DMC0\_RAS}}$, DMC0_UDM, DMC0_UDQS, $\overline{\text{DMC0\_UDQS}}$, $\overline{\text{DMC0\_WE}}$, $\overline{\text{JTG\_EMU}}$, PA_15–0, PB_15–0, PC_15–0, PD_15–0, PE_15–0, PF_15–0, PG_15–0, $\overline{\text{SMC0\_AMS0}}$, $\overline{\text{SMC0\_AOE\_NORDV}}$, $\overline{\text{SMC0\_ARE}}$, $\overline{\text{SMC0\_AWE}}$, SMC0_A01, SMC0_A02, SMC0_D15–0, SYS_CLKOUT, SYS_FAULT, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{SYS\_NMI\_RESOUT}}$.

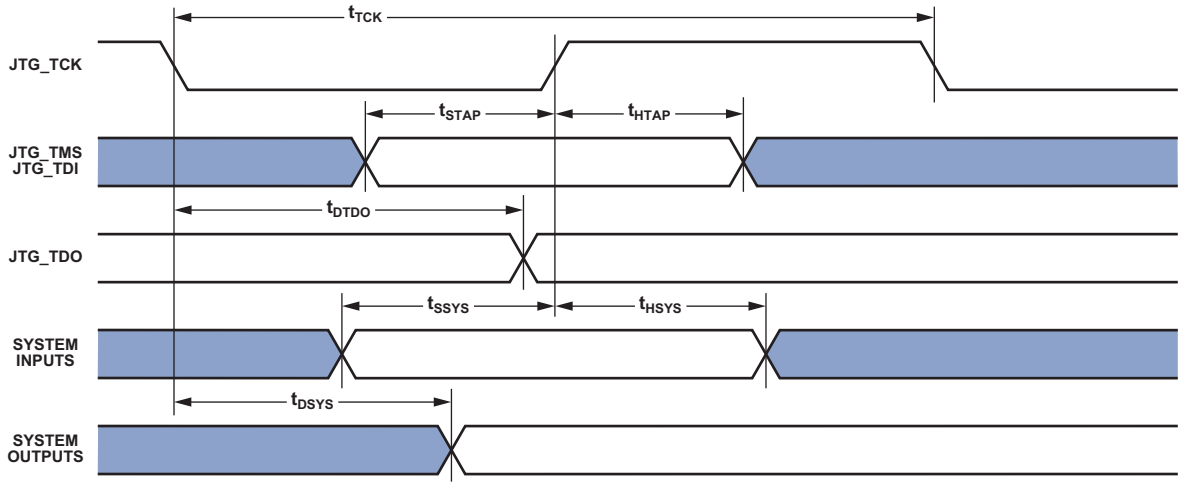


Figure 58. JTAG Port Timing

OUTPUT DRIVE CURRENTS

Figure 59 through Figure 64 show typical current-voltage characteristics for the output drivers of the ADSP-BF60x Blackfin processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

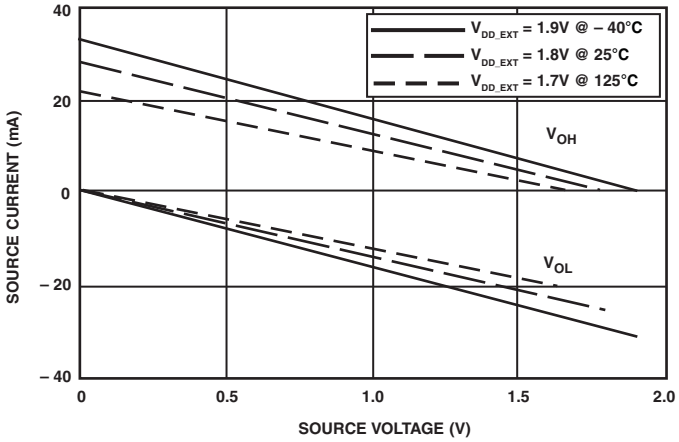


Figure 59. Driver Type A Current (1.8 V V_{DD_EXT})

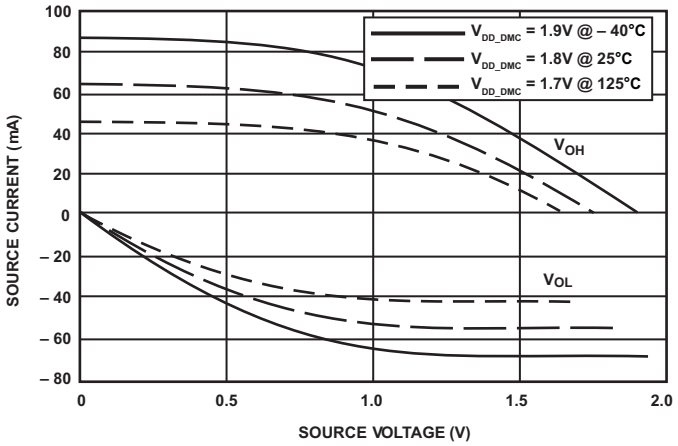


Figure 61. Driver Type B Current (1.8 V V_{DD_DMC})

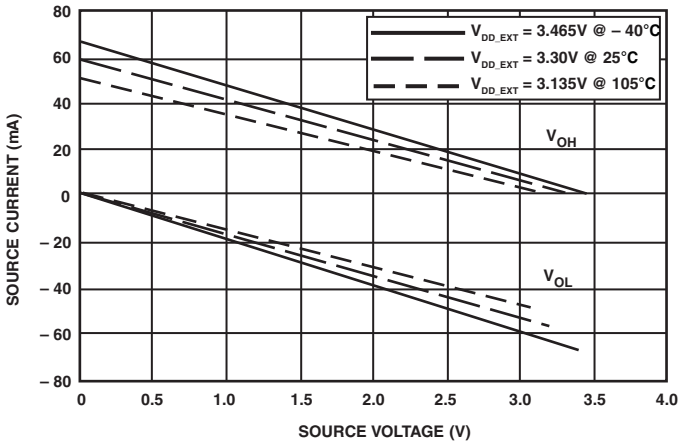


Figure 60. Driver Type A Current (3.3 V V_{DD_EXT})

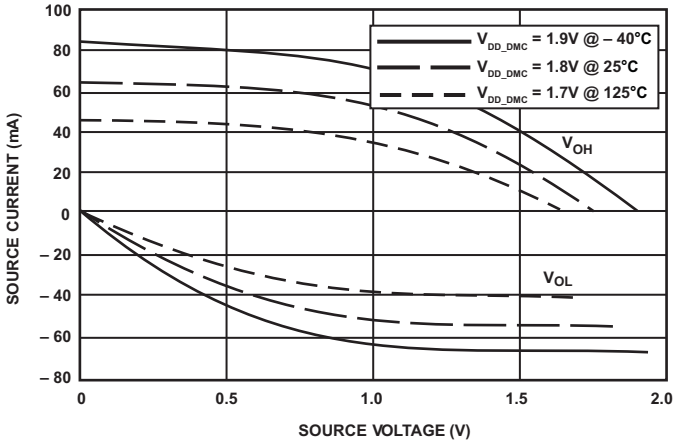


Figure 62. Driver Type C Current (1.8 V V_{DD_DMC})

The time t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.25 V for V_{DDEXT}/V_{DDMEM} (nominal) = 2.5 V/3.3 V and 0.15 V for V_{DDEXT}/V_{DDMEM} (nominal) = 1.8V.

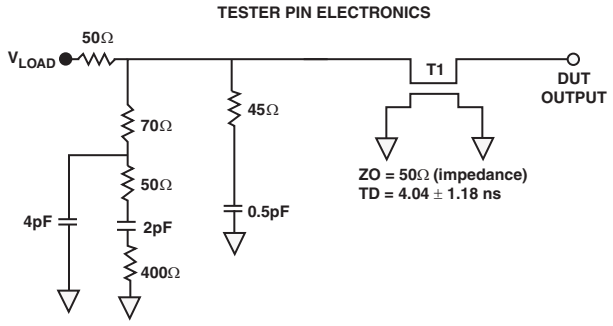
The time $t_{DIS\_MEASURED}$ is the interval from when the reference signal switches, to when the output voltage decays ΔV from the measured output high or output low voltage.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the processor's output voltage and the input threshold for the device requiring the hold time. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time is t_{DECAY} plus the various output disable times as specified in the Timing Specifications on Page 60.

Capacitive Loading

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all pins (see Figure 67). V_{LOAD} is equal to $(V_{DD\_EXT})/2$.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 67. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

The graphs of Figure 68 through Figure 70 show how output rise and fall times vary with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.

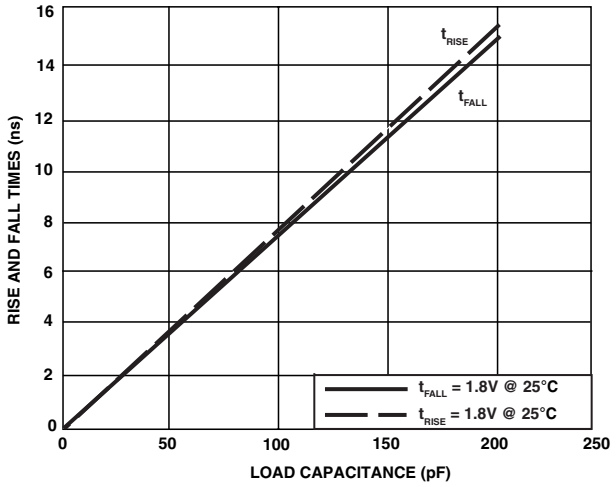


Figure 68. Driver Type A Typical Rise and Fall Times (10%-90%) vs. Load Capacitance (V_{DD_EXT} = 1.8 V)

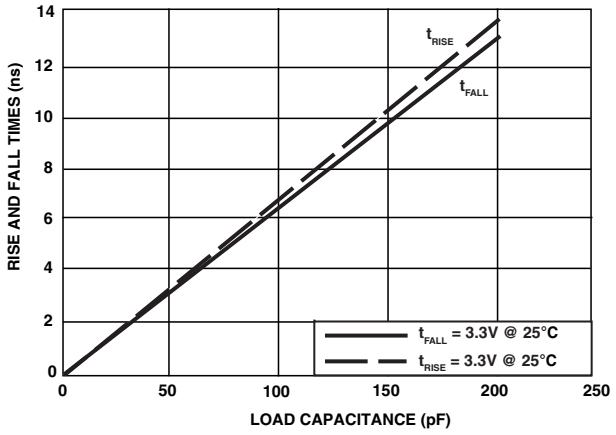


Figure 69. Driver Type A Typical Rise and Fall Times (10%-90%) vs. Load Capacitance (V_{DD_EXT} = 3.3 V)

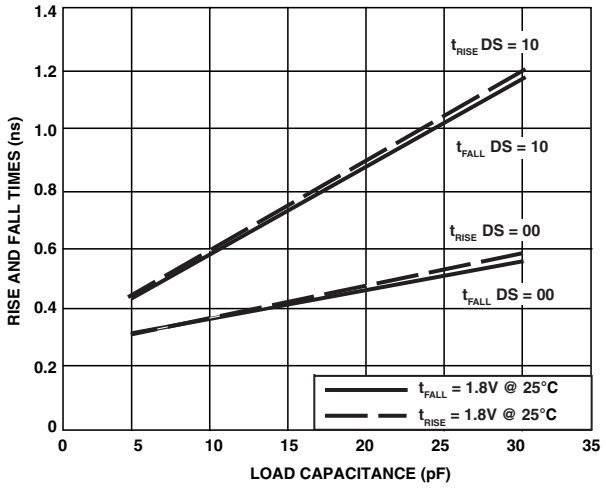


Figure 70. Driver Type B & C Typical Rise and Fall Times (10%-90%) vs. Load Capacitance (V_{DD_DMC} = 1.8 V)

349-BALL CSP_BGA BALL CONFIGURATION

Figure 71 shows an overview of signal placement on the 349-ball CSP_BGA package.

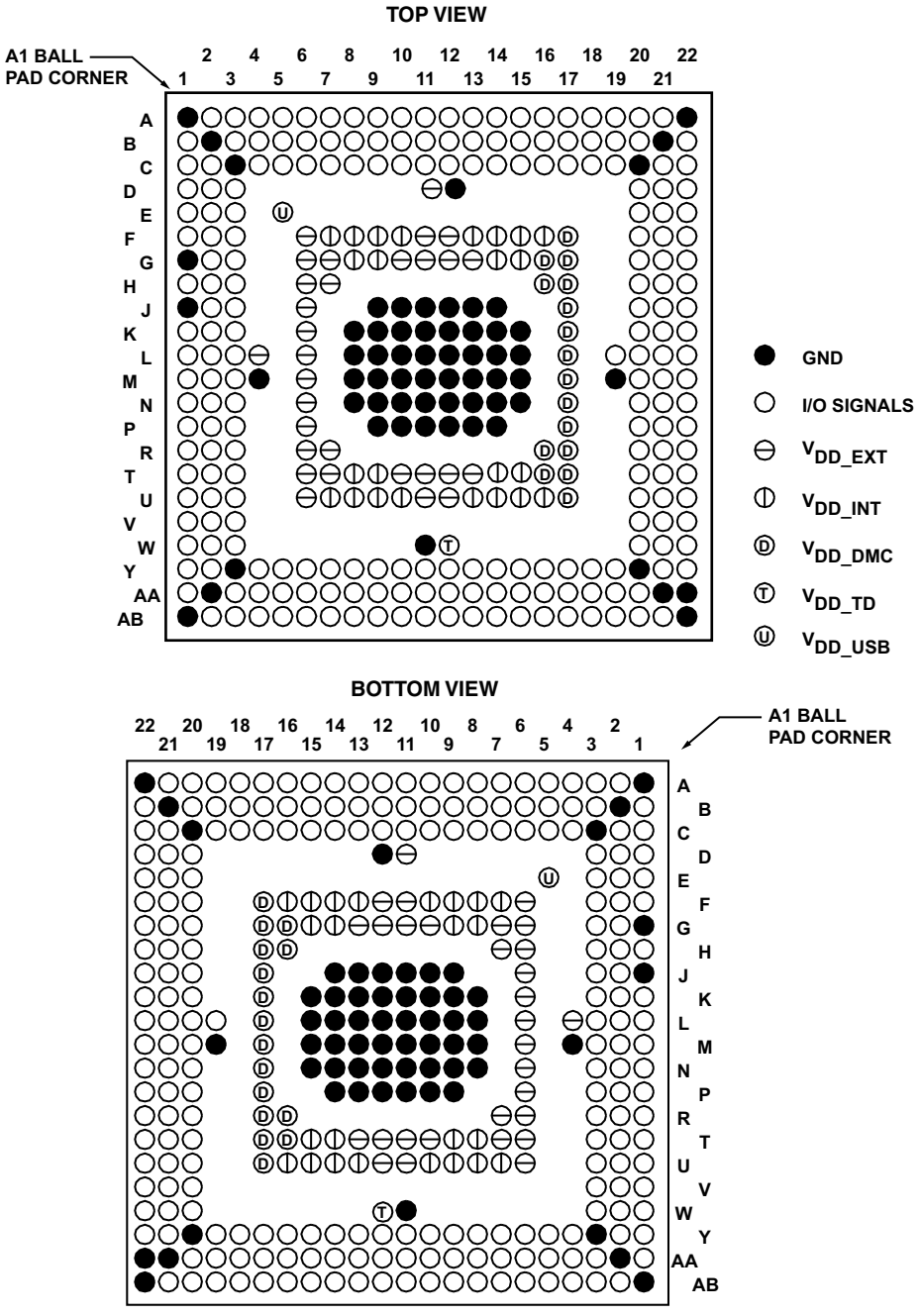


Figure 71. 349-Ball CSP_BGA Ball Configuration