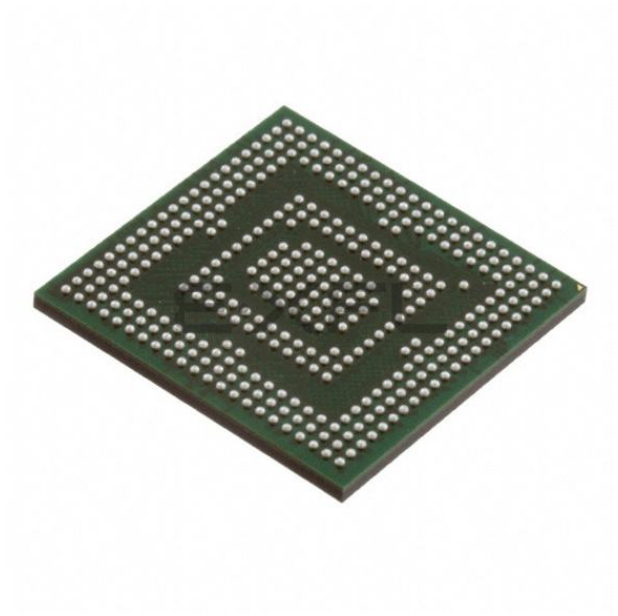

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Dual Core
Interface	CAN, EBI/EMI, Ethernet, I²C, SPI, SPORT, UART/USART, USB OTG
Clock Rate	500MHz
Non-Volatile Memory	ROM (64kB)
On-Chip RAM	808K x 8
Voltage - I/O	1.8V, 3.3V
Voltage - Core	1.25V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	349-LFBGA, CSPBGA
Supplier Device Package	349-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf608kbcz-5

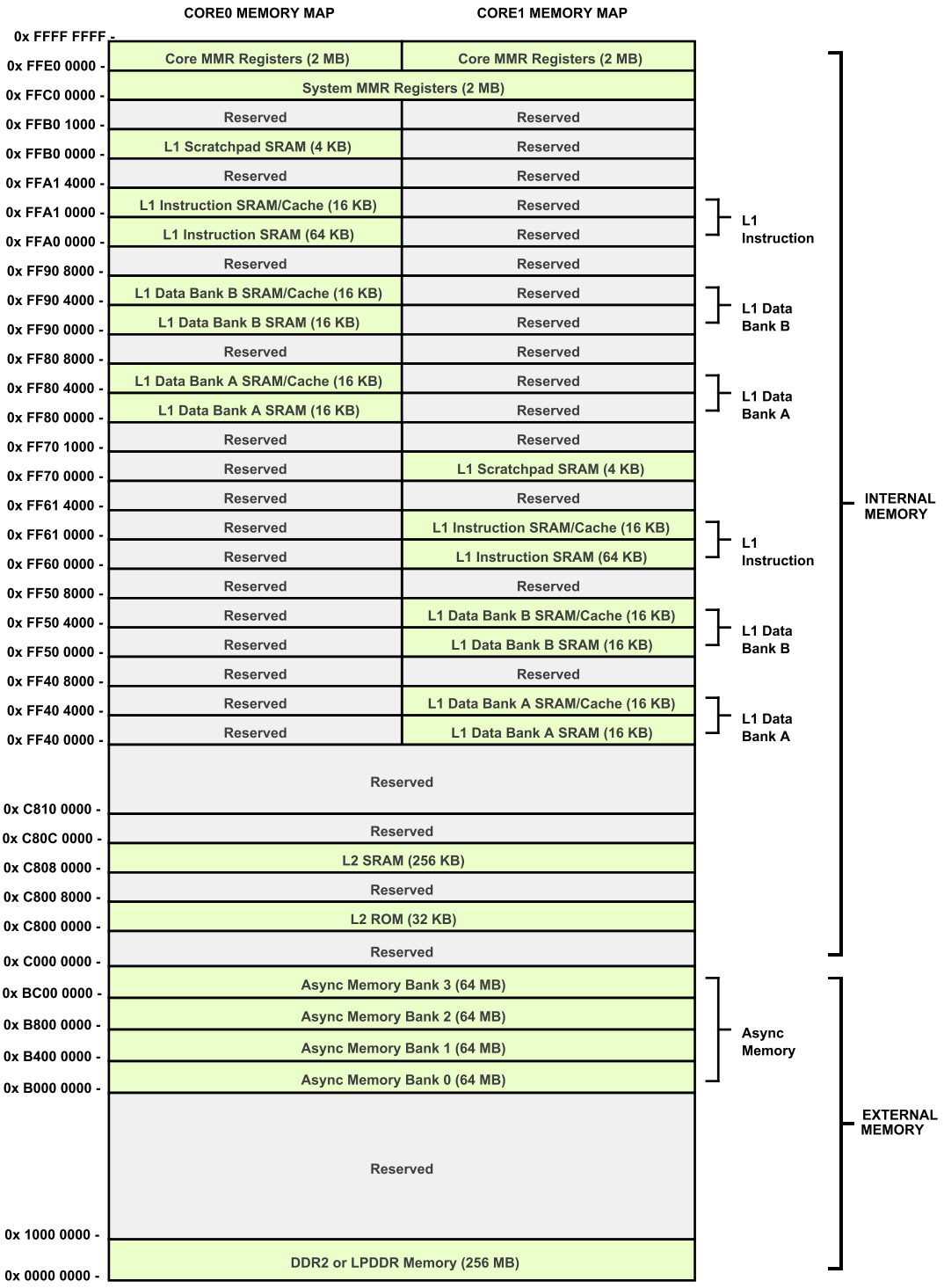


Figure 4. ADSP-BF607/ADSP-BF608/ADSP-BF609 Internal/External Memory Map

Table 6. Detailed Signal Descriptions (Continued)

Signal Name	Direction	Description
RSI_CLK	Output	**Clock** The clock signal applied to the connected device from the RSI.
RSI_CMD	I/O	**Command** Used to send commands to and receive responses from the connected device.
RSI_Dn	I/O	**Data n** Bidirectional data bus.
SMC_ABEn	Output	**Byte Enable n** Indicate whether the lower or upper byte of a memory is being accessed. When an asynchronous write is made to the upper byte of a 16-bit memory, SMC_ABE1 =0 and SMC_ABE0 =1. When an asynchronous write is made to the lower byte of a 16-bit memory, SMC_ABE1 =1 and SMC_ABE0 =0.
SMC_AMSn	Output	**Memory Select n** Typically connects to the chip select of a memory device.
SMC_Ann	Output	**Address n** Address bus.
SMC_AOE	Output	**Output Enable** Asserts at the beginning of the setup period of a read access.
SMC_ARDY	Input	**Asynchronous Ready** Flow control signal used by memory devices to indicate to the SMC when further transactions may proceed.
SMC_ARE	Output	**Read Enable** Asserts at the beginning of a read access.
SMC_AWE	Output	**Write Enable** Asserts for the duration of a write access period.
SMC_BG	Output	**Bus Grant** Output used to indicate to an external device that it has been granted control of the SMC buses.
SMC_BGH	Output	**Bus Grant Hang** Output used to indicate that the SMC has a pending transaction which requires control of the bus to be restored before it can be completed.
SMC_BR	Input	**Bus Request** Input used by an external device to indicate that it is requesting control of the SMC buses.
SMC_Dnn	I/O	**Data n** Bidirectional data bus.
SMC_NORCLK	Output	**NOR Clock** Clock for synchronous burst mode.
SMC_NORDV	Output	**NOR Data Valid** Asserts for the duration of a synchronous burst mode read setup period.
SMC_NORWT	Input	**NOR Wait** Flow control signal used by memory devices in synchronous burst mode to indicate to the SMC when further transactions may proceed.
SPI_CLK	I/O	**Clock** Input in slave mode, output in master mode.
SPI_D2	I/O	**Data 2** Used to transfer serial data in quad mode. Open drain in ODM mode.
SPI_D3	I/O	**Data 3** Used to transfer serial data in quad mode. Open drain in ODM mode.
SPI_MISO	I/O	**Master In, Slave Out** Used to transfer serial data. Operates in the same direction as SPI_MOSI in dual and quad modes. Open drain in ODM mode.
SPI_MOSI	I/O	**Master Out, Slave In** Used to transfer serial data. Operates in the same direction as SPI_MISO in dual and quad modes. Open drain in ODM mode.
SPI_RDY	I/O	**Ready** Optional flow signal. Output in slave mode, input in master mode.
SPI_SELn	Output	**Slave Select Output n** Used in master mode to enable the desired slave.
SPI_SS	Input	**Slave Select Input** Slave mode: acts as the slave select input. Master mode: optionally serves as an error detection input for the SPI when there are multiple masters.
SPT_ACLK	I/O	**Channel A Clock** Data and frame sync are driven/sampled with respect to this clock. This signal can be either internally or externally generated.
SPT_AD0	I/O	**Channel A Data 0** Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
SPT_AD1	I/O	**Channel A Data 1** Secondary bidirectional data I/O. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
SPT_AFS	I/O	**Channel A Frame Sync** The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally.
SPT_ATDV	Output	**Channel A Transmit Data Valid** This signal is optional and only active when SPORT is configured in multi-channel transmit mode. It is asserted during enabled slots.
SPT_BCLK	I/O	**Channel B Clock** Data and frame sync are driven/sampled with respect to this clock. This signal can be either internally or externally generated.
SPT_BD0	I/O	**Channel B Data 0** Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.

GP I/O MULTIPLEXING FOR 349-BALL CSP_BGA

Table 8 through Table 14 identifies the pin functions that are multiplexed on the general-purpose I/O pins of the 349-ball CSP_BGA package.

Table 8. Signal Multiplexing for Port A

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function Input Tap
PA_00	SMC0_A03	PPI2_D00	LP0_D0	
PA_01	SMC0_A04	PPI2_D01	LP0_D1	
PA_02	SMC0_A05	PPI2_D02	LP0_D2	
PA_03	SMC0_A06	PPI2_D03	LP0_D3	
PA_04	SMC0_A07	PPI2_D04	LP0_D4	
PA_05	SMC0_A08	PPI2_D05	LP0_D5	
PA_06	SMC0_A09	PPI2_D06	LP0_D6	
PA_07	SMC0_A10	PPI2_D07	LP0_D7	
PA_08	SMC0_A11	PPI2_D08	LP1_D0	
PA_09	SMC0_A12	PPI2_D09	LP1_D1	
PA_10	SMC0_A14	PPI2_D10	LP1_D2	
PA_11	SMC0_A15	PPI2_D11	LP1_D3	
PA_12	SMC0_A17	PPI2_D12	LP1_D4	
PA_13	SMC0_A18	PPI2_D13	LP1_D5	
PA_14	SMC0_A19	PPI2_D14	LP1_D6	
PA_15	SMC0_A20	PPI2_D15	LP1_D7	

Table 9. Signal Multiplexing for Port B

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function Input Tap
PB_00	SMC0_NORCLK	PPI2_CLK	LP0_CLK	
PB_01	$\overline{\text{SMC0\_AMS1}}$	PPI2_FS1	LP0_ACK	
PB_02	SMC0_A13	PPI2_FS2	LP1_ACK	
PB_03	SMC0_A16	PPI2_FS3	LP1_CLK	
PB_04	$\overline{\text{SMC0\_AMS2}}$	$\overline{\text{SMC0\_ABE0}}$	SPT0_AFS	
PB_05	$\overline{\text{SMC0\_AMS3}}$	$\overline{\text{SMC0\_ABE1}}$	SPT0_ACLK	
PB_06	SMC0_A21	SPT0_ATDV		TM0_ACLK4
PB_07	SMC0_A22	PPI2_D16	SPT0_BFS	
PB_08	SMC0_A23	PPI2_D17	SPT0_BCLK	
PB_09	$\overline{\text{SMC0\_BGH}}$		SPT0_AD0	TM0_ACLK2
PB_10	SMC0_A24		SPT0_BD1	TM0_ACLK0
PB_11	SMC0_A25		SPT0_BD0	TM0_ACLK3
PB_12	$\overline{\text{SMC0\_BG}}$	SPT0_BTDV	SPT0_AD1	TM0_ACLK1
PB_13	ETH0_TXEN	PPI1_FS1		TM0_ACI6
PB_14	ETH0_REFCLK	PPI1_CLK		
PB_15	ETH0_PTPPPS	PPI1_FS3		

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
DMC0_DQ13	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 13. Notes: No notes.
DMC0_DQ14	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 14. Notes: No notes.
DMC0_DQ15	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 15. Notes: No notes.
DMC0_LDM	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Mask for Lower Byte. Notes: No notes.
DMC0_LDQS	I/O	C	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Lower Byte. Notes: For LPDDR, a 100k ohm pull-down resistor is required.
$\overline{\text{DMC0\_LDQS}}$	I/O	C	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Lower Byte (complement). Notes: For single ended DDR2, connect to VREF_DMC. For LPDDR, leave unconnected.
DMC0_ODT	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 On-die termination. Notes: For LPDDR, leave unconnected.
$\overline{\text{DMC0\_RAS}}$	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Row Address Strobe. Notes: No notes.
DMC0_UDM	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Mask for Upper Byte. Notes: No notes.
DMC0_UDQS	I/O	C	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Upper Byte. Notes: For LPDDR, a 100k ohm pull-down resistor is required.
$\overline{\text{DMC0\_UDQS}}$	I/O	C	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Upper Byte (complement). Notes: For single ended DDR2, connect to VREF_DMC. For LPDDR, leave unconnected.
$\overline{\text{DMC0\_WE}}$	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Write Enable. Notes: No notes.
GND	g	na	none	none	none	none	none	na	Desc: Ground. Notes: No notes.
$\overline{\text{JTG\_EMU}}$	I/O	A	none	none	none	none	none	VDD_EXT	Desc: Emulation Output. Notes: No notes.
JTG_TCK	I/O	na	pd	none	none	none	none	VDD_EXT	Desc: JTG Clock. Notes: Functional during reset.
JTG_TDI	I/O	na	pu	none	none	none	none	VDD_EXT	Desc: JTG Serial Data Input. Notes: Functional during reset.
JTG_TDO	I/O	A	none	none	none	none	none	VDD_EXT	Desc: JTG Serial Data Output. Notes: Functional during reset, three-state when $\overline{\text{JTG\_TRST}}$ is asserted.
JTG_TMS	I/O	na	pu	none	none	none	none	VDD_EXT	Desc: JTG Mode Select. Notes: Functional during reset.
$\overline{\text{JTG\_TRST}}$	I/O	na	pd	none	none	none	none	VDD_EXT	Desc: JTG Reset. Notes: Functional during reset.

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PF_03	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 3 | PWM0 Channel B High Side | EPPI0 Data 3 | LP2 Data 3. Notes: No notes.
PF_04	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 4 | PWM0 Channel C Low Side | EPPI0 Data 4 | LP2 Data 4. Notes: No notes.
PF_05	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 5 | PWM0 Channel C High Side | EPPI0 Data 5 | LP2 Data 5. Notes: No notes.
PF_06	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 6 | PWM0 Channel D Low Side | EPPI0 Data 6 | LP2 Data 6. Notes: No notes.
PF_07	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 7 | PWM0 Channel D High Side | EPPI0 Data 7 | LP2 Data 7. Notes: No notes.
PF_08	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 8 | SPI1 Slave Select Output b | EPPI0 Data 8 | LP3 Data 0. Notes: No notes.
PF_09	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 9 | SPI1 Slave Select Output b | EPPI0 Data 9 | LP3 Data 1. Notes: No notes.
PF_10	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 10 | ACM0 Address 4 | EPPI0 Data 10 | LP3 Data 2. Notes: No notes.
PF_11	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 11 | EPPI0 Data 11 | LP3 Data 3 | PWM0 Shutdown Input. Notes: No notes.
PF_12	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 12 | ACM0 Address 2 | EPPI0 Data 12 | LP3 Data 4. Notes: No notes.
PF_13	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 13 | ACM0 Address 3 | EPPI0 Data 13 | LP3 Data 5. Notes: No notes.
PF_14	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 14 | EPPI0 Data 14 | ACM0 Address 0 | LP3 Data 6. Notes: No notes.
PF_15	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 15 | ACM0 Address 1 | EPPI0 Data 15 | LP3 Data 7. Notes: No notes.
PG_00	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PG Position 0 | PWM1 Channel B High Side | RSI0 Data 2 | ETH1 Receive Data 0. Notes: Has an optional internal pull-up resistor for use with RSI. See the RSI chapter in the processor hardware reference for more details.
PG_01	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PG Position 1 | SPORT2 Channel A Frame Sync | TIMER0 Timer 2 | CAN0 Transmit. Notes: No notes.

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PG_12	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PG Position 12 | SPORT2 Channel B Data 0 | TIMER0 Timer 7 | CNT0 Count Down and Gate. Notes: No notes.
PG_13	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PG Position 13 | UART1 Clear to Send | TIMER0 Clock. Notes: No notes.
PG_14	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PG Position 14 | UART1 Receive | SYS Core 1 Idle Indicator | TIMER0 Alternate Capture Input 1. Notes: No notes.
PG_15	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PG Position 15 | UART1 Transmit | SYS Core 0 Idle Indicator | SYS Processor Sleep Indicator | TIMER0 Alternate Capture Input 4. Notes: No notes.
SMC0_A01	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Address 1. Notes: No notes.
SMC0_A02	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Address 2. Notes: No notes.
$\overline{\text{SMC0\_AMS0}}$	I/O	A	pu	pu	none	pu	none	VDD_EXT	Desc: SMC0 Memory Select 0. Notes: No notes.
$\overline{\text{SMC0\_AOE\_}}$ NORDV	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 NOR Data Valid | SMC0 Output Enable. Notes: No notes.
SMC0_ARDY_ NORWT	I/O	na	none	none	none	none	none	VDD_EXT	Desc: SMC0 NOR Wait | SMC0 Asynchronous Ready. Notes: Requires an external pull-up resistor.
$\overline{\text{SMC0\_ARE}}$	I/O	A	pu	pu	none	pu	none	VDD_EXT	Desc: SMC0 Read Enable. Notes: No notes.
$\overline{\text{SMC0\_AWE}}$	I/O	A	pu	pu	none	pu	none	VDD_EXT	Desc: SMC0 Write Enable. Notes: No notes.
$\overline{\text{SMC0\_BR}}$	I/O	na	none	none	none	none	none	VDD_EXT	Desc: SMC0 Bus Request. Notes: Requires an external pull-up resistor.
SMC0_D00	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Data 0. Notes: No notes.
SMC0_D01	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Data 1. Notes: No notes.
SMC0_D02	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Data 2. Notes: No notes.
SMC0_D03	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Data 3. Notes: No notes.
SMC0_D04	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Data 4. Notes: No notes.
SMC0_D05	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Data 5. Notes: No notes.

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
SYS_PWRGD	I/O	na	none	none	none	none	none	VDD_EXT	Desc: SYS Power Good Indicator. Notes: If hibernate is not used or the internal Power Good Counter is used, connect to VDD_EXT.
SYS_TDA	a	na	none	none	none	none	none	VDD_TD	Desc: SYS Thermal Diode Anode. Notes: Active during reset and hibernate. If the thermal diode is not used, connect to ground.
SYS_TDK	a	na	none	none	none	none	none	VDD_TD	Desc: SYS Thermal Diode Cathode. Notes: Active during reset and hibernate. If the thermal diode is not used, connect to ground.
SYS_XTAL	a	na	none	none	none	none	none	VDD_EXT	Desc: SYS Crystal Output. Notes: Leave unconnected if an oscillator is used to provide SYS_CLKIN. Active during reset. State during hibernate is controlled by DPM_HIB_DIS.
TWI0_SCL	I/O	D	none	none	none	none	none	VDD_EXT	Desc: TWI0 Serial Clock. Notes: Open drain, requires external pull-up resistor. Consult Version 2.1 of the I2C specification for the proper resistor value. If TWI is not used, connect to ground.
TWI0_SDA	I/O	D	none	none	none	none	none	VDD_EXT	Desc: TWI0 Serial Data. Notes: Open drain, requires external pull-up resistor. Consult Version 2.1 of the I2C specification for the proper resistor value. If TWI is not used, connect to ground.
TWI1_SCL	I/O	D	none	none	none	none	none	VDD_EXT	Desc: TWI1 Serial Clock. Notes: Open drain, requires external pull-up resistor. Consult Version 2.1 of the I2C specification for the proper resistor value. If TWI is not used, connect to ground.
TWI1_SDA	I/O	D	none	none	none	none	none	VDD_EXT	Desc: TWI1 Serial Data. Notes: Open drain, requires external pull-up resistor. See the I2C-Bus Specification, Version 2.1,January 2000 for the proper resistor value. If TWI is not used, connect to ground.
USB0_CLKIN	a	na	none	none	none	none	none	VDD_USB	Desc: USB0 Clock/Crystal Input. Notes: If USB is not used, connect to ground. Active during reset.
USB0_DM	I/O	F	none	none	none	none	none	VDD_USB	Desc: USB0 Data –. Notes: Pull low if not using USB. For complete documentation of hibernate behavior when USB is used, see the USB chapter in the processor hardware reference.

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
USB0_DP	I/O	F	none	none	none	none	none	VDD_USB	Desc: USB0 Data +. Notes: Pull low if not using USB. For complete documentation of hibernate behavior when USB is used, see the USB chapter in the processor hardware reference.
USB0_ID	I/O	na	none	none	none	pu	none	VDD_USB	Desc: USB0 OTG ID. Notes: If USB is not used, connect to ground. When USB is being used, the internal pull-up resistor that is present during hibernate is programmable. See the USB chapter in the processor hardware reference. Active during reset.
USB0_VBC	I/O	E	none	none	none	wk	none	VDD_USB	Desc: USB0 VBUS Control. Notes: If USB is not used, pull low.
USB0_VBUS	I/O	G	none	none	none	none	none	VDD_USB	Desc: USB0 Bus Voltage. Notes: If USB is not used, connect to ground.
VDD_DMC	s	na	none	none	none	none	none	na	Desc: VDD for DMC. Notes: If the DMC is not used, connect to VDD_INT.
VDD_EXT	s	na	none	none	none	none	none	na	Desc: External VDD. Notes: Must be powered.
VDD_INT	s	na	none	none	none	none	none	na	Desc: Internal VDD. Notes: Must be powered.
VDD_TD	s	na	none	none	none	none	none	na	Desc: VDD for Thermal Diode. Notes: If the thermal diode is not used, connect to ground.
VDD_USB	s	na	none	none	none	none	none	na	Desc: VDD for USB. Notes: If USB is not used, connect to VDD_EXT.
VREF_DMC	s	na	none	none	none	none	none	na	Desc: VREF for DMC. Notes: If the DMC is not used, connect to VDD_INT.

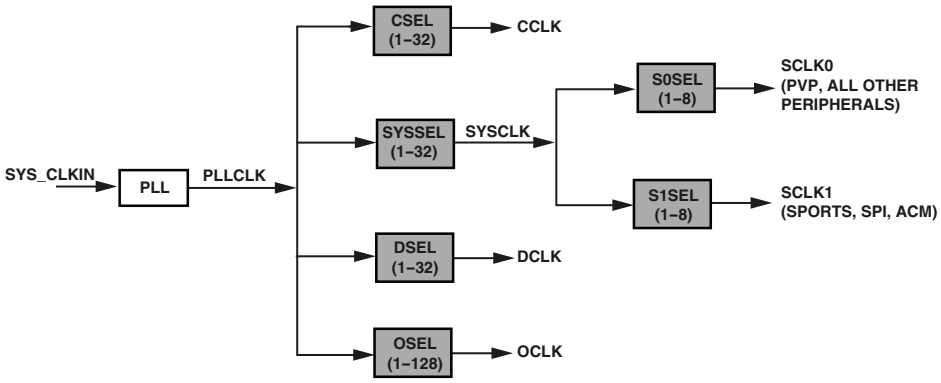


Figure 8. Clock Relationships and Divider Values

Total Internal Power Dissipation

Total power dissipation has two components:

1. Static, including leakage current (deep sleep)
2. Dynamic, due to transistor switching characteristics for each clock domain

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. The following equation describes the internal current consumption.

$$I_{DDINT\_TOT} = I_{DDINT\_CCLK\_DYN} + I_{DDINT\_SYSCLK\_DYN} + I_{DDINT\_SCLK0\_DYN} + I_{DDINT\_SCLK1\_DYN} + I_{DDINT\_DCLK\_DYN} + I_{DDINT\_USBCLK\_DYN} + I_{DDINT\_DMA\_DR\_DYN} + I_{DDINT\_DEEPSLEEP} + I_{DDINT\_PVP\_DYN}$$

$I_{DDINT\_DEEPSLEEP}$ is the only item present that is part of the static power dissipation component. $I_{DDINT\_DEEPSLEEP}$ is specified as a function of voltage (V_{DD_INT}) and temperature (see Table 21).

There are eight different items that contribute to the dynamic power dissipation. These components fall into three broad categories: application-dependent currents, clock currents and data transmission currents.

Application-Dependent Current

The application-dependent currents include the dynamic current in the core clock domain and the dynamic current of the PVP.

Core clock (CCLK) use is subject to an activity scaling factor (ASF) that represents application code running on the processor cores and L1/L2 memories (Table 20). The ASF is combined with the CCLK frequency and V_{DD_INT} dependent data in Table 19 to calculate this portion.

$I_{DDINT\_CCLK\_DYN}$ (mA) = Table 19 × (ASFC0 + ASFC1)

The dynamic current of the PVP is determined by selecting the appropriate use case from Table 22.

$I_{DDINT\_PVP\_DYN}$ (mA) = Table 22

Clock Current

The dynamic clock currents provide the total power dissipated by all transistors switching in the clock paths. The power dissipated by each clock domain is dependent on voltage (V_{DD_INT}), operating frequency and a unique scaling factor.

$I_{DDINT\_SYSCLK\_DYN}$ (mA) = 0.187 × f_{SYSCLK} (MHz) × V_{DD_INT} (V)

$I_{DDINT\_SCLK0\_DYN}$ (mA) = 0.217 × f_{SCLK0} (MHz) × V_{DD_INT} (V)

$I_{DDINT\_SCLK1\_DYN}$ (mA) = 0.042 × f_{SCLK1} (MHz) × V_{DD_INT} (V)

$I_{DDINT\_DCLK\_DYN}$ (mA) = 0.024 × f_{DCLK} (MHz) × V_{DD_INT} (V)

The dynamic component of the USB clock is a unique case. The USB clock contributes a near constant current value when used.

$I_{DDINT\_USBCLK\_DYN}$ (mA) = 5 mA (if USB enabled)

Data Transmission Current

The data transmission current represents the power dissipated when transmitting data. This current is expressed in terms of data rate. The calculation is performed by adding the data rate (MB/s) of each DMA and core driven access to peripherals and L2/external memory. This number is then multiplied by a coefficient and V_{DD_INT}. The following equation provides an estimate of all data transmission current.

$I_{DDINT\_DMA\_DR\_DYN}$(mA) = 0.0578 × data rate (MB/s) × V_{DD_INT} (V)

For details on using this equation see the related Engineer Zone material.

Table 19. CCLK Dynamic Current per core (mA, with ASF = 1)

	Voltage (V_{DD_INT})						
f_{CCLK} (MHz)	**1.190**	**1.200**	**1.225**	**1.250**	**1.275**	**1.300**	**1.320**
500	97.9	98.8	101.5	103.9	106.7	109.3	110.8
450	88.6	89.5	91.9	94.1	96.7	98.9	100.6
400	79.3	80.1	82.2	84.3	86.5	88.6	90.1
350	70.0	70.7	72.5	74.4	76.3	78.3	79.4
300	60.6	61.2	63.0	64.6	66.3	68.0	69.1
250	51.3	51.8	53.2	54.7	56.3	57.6	58.5
200	42.0	42.4	43.6	44.8	46.0	47.2	48.2
150	32.5	32.9	34.0	34.8	35.9	37.0	37.4
100	23.2	23.5	24.2	25.0	25.7	26.5	26.9

Table 20. Activity Scaling Factors (ASF)

I_{DDINT} Power Vector	ASF
$I_{DD-PEAK}$	1.34
$I_{DD-HIGH}$	1.25
$I_{DD-FULL-ON-TYP}$	1.00
I_{DD-APP}	0.86
I_{DD-NOP}	0.72
$I_{DD-IDLE}$	0.14

Table 21. Static Current—$I_{DD\_DEEPSLEEP}$ (mA)

	Voltage (V_{DD_INT})						
T_J (°C)	1.190	1.200	1.225	1.250	1.275	1.300	1.320
–40	1.7	1.8	2.2	2.5	2.7	3.1	3.4
–20	4.0	4.2	4.6	5.1	5.6	6.2	6.8
0	8.4	9.0	9.6	10.6	11.5	12.5	13.4
25	19.0	19.8	21.5	23.2	25.3	27.2	29.0
40	29.9	31.7	34.4	36.8	40.0	42.8	45.4
55	46.6	48.9	52.4	56.4	60.6	65.0	68.1
70	66.4	70.4	75.5	80.6	86.2	92.4	97.9
85	93.9	99.3	105.9	113.0	120.7	128.9	136.4
100	137.2	144.2	153.6	163.4	173.9	185.1	194.1
105	153.8	162.4	172.5	183.4	195.2	207.5	217.5
115	193.3	203.7	216.2	229.5	243.9	258.6	271.1
125	236.1	247.2	261.8	277.3	294.0	311.9	326.4

Table 22. $I_{DDINT\_PVP\_DYN}$ (mA)

PVP Activity Level	PVPSF (PVP Scaling Factor)
High	42.4
Medium	20
Low	0

TIMING SPECIFICATIONS

Specifications are subject to change without notice.

Clock and Reset Timing

Table 26 and Figure 10 describe clock and reset operations. Per the CCLK, SYSCLK, SCLK0, SCLK1, DCLK, and OCLK timing specifications in Table 17 on Page 53, combinations of SYS_CLKIN and clock multipliers must not select clock rates in excess of the processor's maximum instruction rate.

Table 26. Clock and Reset Timing

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Timing Requirements				
f_{CKIN}	SYS_CLKIN Frequency (using a crystal)[1, 2, 3]	20	50	MHz
f_{CKIN}	SYS_CLKIN Frequency (using a crystal oscillator)[1, 2, 3]	20	60	MHz
t_{CKINL}	SYS_CLKIN Low Pulse[1]	6.67		ns
t_{CKINH}	SYS_CLKIN High Pulse[1]	6.67		ns
t_{WRST}	$\overline{\text{SYS\_HWRST}}$ Asserted Pulse Width Low[4]	11 × t_{CKIN}		ns

[1] Applies to PLL bypass mode and PLL non bypass mode.
[2] The t_{CKIN} period (see Figure 10) equals $1/f_{CKIN}$.
[3] If the CGU_CTL.DF bit is set, the minimum f_{CKIN} specification is 40 MHz.
[4] Applies after power-up sequence is complete. See Table 27 and Figure 11 for power-up reset timing.

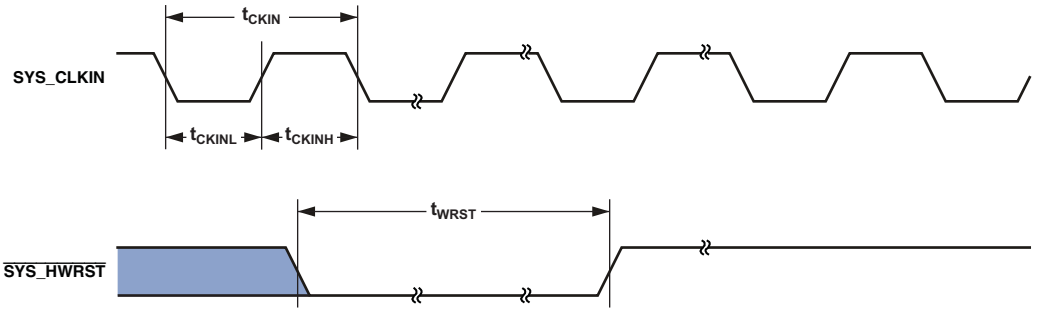


Figure 10. Clock and Reset Timing

Synchronous Burst Flash Read

In synchronous burst mode the programmed NOR burst clock ($f_{NRCLKPROG}$) frequency in MHz is set by the following equation where BCLK is a field in the SMC_BxCTL register that can be set from 0 to 3:

$$f_{NRCLKPROG} = \frac{f_{SCLK0}}{(BCLK + 1)}$$

$$t_{NRCLKPROG} = \frac{1}{f_{NRPCLKPROG}}$$

Table 31. Synchronous Burst AC Timing (BxMODE = b#11)

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Timing Requirements				
t_{NDS}	DATA-In Setup Before SMC0_NORCLK High	3		ns
t_{NDH}	DATA-In Hold After SMC0_NORCLK High	1.5		ns
t_{NWS}	WAIT-In Setup Before SMC0_NORCLK High	3		ns
t_{NWH}	WAIT-In Hold After SMC0_NORCLK High	1.5		ns
Switching Characteristics				
t_{NRCLS}	NOR_CLK Low Period[1]	$0.5 \times t_{NRCLKPROG} - 1$		ns
t_{NRCHS}	NOR_CLK High Period[1]	$0.5 \times t_{NRCLKPROG} - 1$		ns
t_{NRCLK}	NOR_CLK Period[1]	$t_{NRCLKPROG} - 1$		ns
t_{NDO}	Output Delay After SMC0_NORCLK High[2]		6	ns
t_{NHO}	Output Hold After SMC0_NORCLK High[2]	0.8		ns

[1] See Table 17 on Page 53 in Clock Related Operating Conditions for details on the minimum period that may be programmed for $t_{NRCLKPROG}$.
[2] Output = SMC0_Ax (address), SMC0_NORDV, $\overline{\text{SMC0\_ARE}}$, $\overline{\text{SMC0\_AMSx}}$ (N0R_CE).

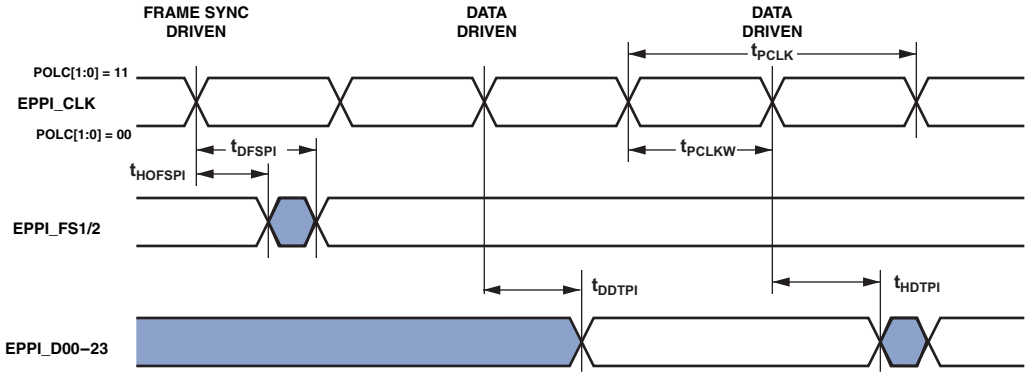


Figure 26. PPI Internal Clock GP Transmit Mode with Internal Frame Sync Timing

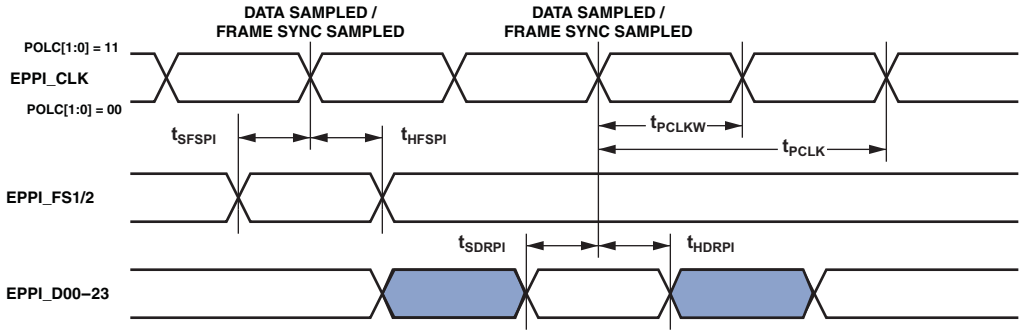


Figure 27. PPI Internal Clock GP Receive Mode with External Frame Sync Timing

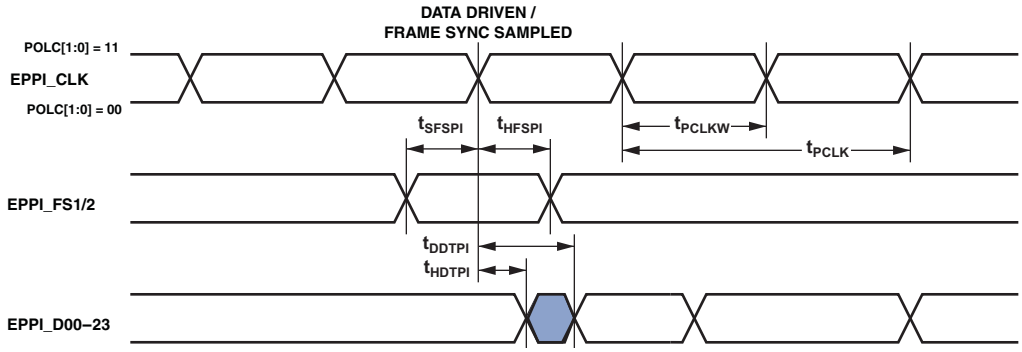


Figure 28. PPI Internal Clock GP Transmit Mode with External Frame Sync Timing

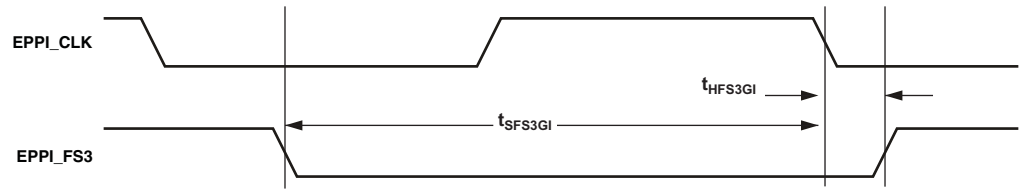
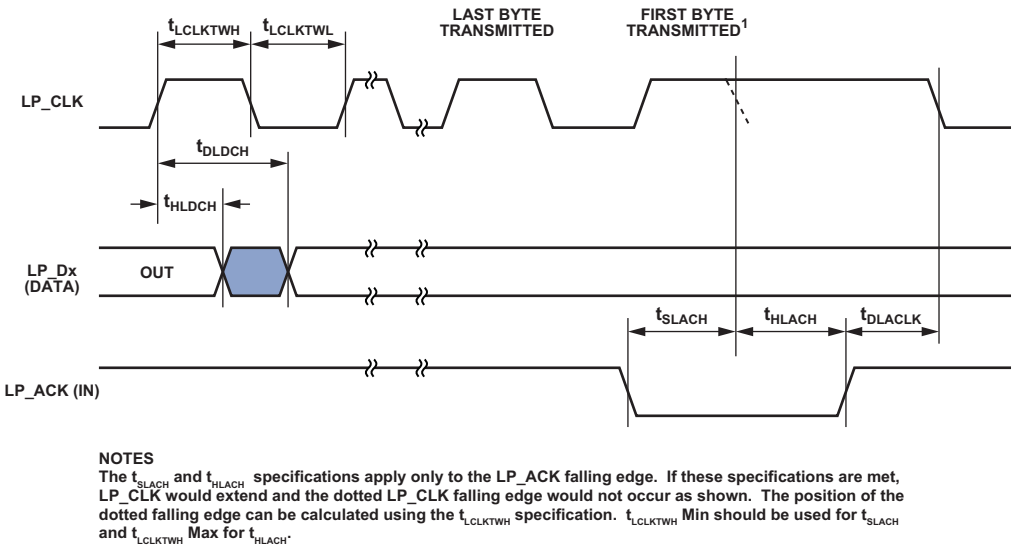


Figure 29. Clock Gating Mode with Internal Clock and External Frame Sync Timing

Table 45. Link Ports—Transmit

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{SLACH}	LP_ACK Setup Before LP_CLK Low	$2 \times t_{SCLK0} + 17.5$		$2 \times t_{SCLK0} + 13.5$		ns
t_{HLACH}	LP_ACK Hold After LP_CLK Low	0		0		ns
Switching Characteristics						
t_{DLDCH}	Data Delay After LP_CLK High		2.5		2.5	ns
t_{HLDCH}	Data Hold After LP_CLK High	–1.5		–1.5		ns
$t_{LCLKTWL}$[1]	LP_CLK Width Low	$0.4 \times t_{LCLKTPROG}$	$0.6 \times t_{LCLKTPROG}$	$0.4 \times t_{LCLKTPROG}$	$0.6 \times t_{LCLKTPROG}$	ns
$t_{LCLKTWH}$[1]	LP_CLK Width High	$0.4 \times t_{LCLKTPROG}$	$0.6 \times t_{LCLKTPROG}$	$0.4 \times t_{LCLKTPROG}$	$0.6 \times t_{LCLKTPROG}$	ns
t_{LCLKTW}[1]	LP_CLK Period	$t_{LCLKTPROG} - 1.2$		$t_{LCLKTPROG} - 1.2$		ns
t_{DLACLK}	LP_CLK Low Delay After LP_ACK High	$t_{SCLK0} + 4$	$(2 \times t_{SCLK0}) + t_{LCLK} + 10$	$t_{SCLK0} + 4$	$(2 \times t_{SCLK0}) + t_{LCLK} + 10$	ns

[1] See Table 17 on Page 53 in Clock Related Operating Conditions for details on the minimum period that may be programmed for $t_{LCLKTPROG}$.



NOTES
The t_{SLACH} and t_{HLACH} specifications apply only to the LP_ACK falling edge. If these specifications are met, LP_CLK would extend and the dotted LP_CLK falling edge would not occur as shown. The position of the dotted falling edge can be calculated using the $t_{LCLKTWH}$ specification. $t_{LCLKTWH}$ Min should be used for t_{SLACH} and $t_{LCLKTWH}$ Max for t_{HLACH}.

Figure 35. Link Ports—Transmit

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) serial clock (SPT_CLK) width. In Figure 36 either the rising edge or the falling edge of SPT_CLK (external or internal) can be used as the active sampling edge.

When externally generated the SPORT clock is called $f_{SPTCLKEXT}$:

$$t_{SPTCLKEXT} = \frac{1}{f_{SPTCLKEXT}}$$

When internally generated, the programmed SPORT clock ($f_{SPTCLKPROG}$) frequency in MHz is set by the following equation where CLKDIV is a field in the SPORT_DIV register that can be set from 0 to 65535:

$$f_{SPTCLKPROG} = \frac{f_{SCLK1}}{(CLKDIV + 1)}$$

$$t_{SPTCLKPROG} = \frac{1}{f_{SPTCLKPROG}}$$

Table 46. Serial Ports—External Clock

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{SFSE}	Frame Sync Setup Before SPT_CLK (Externally Generated Frame Sync in either Transmit or Receive Mode)[1]	2		2		ns
t_{HFSE}	Frame Sync Hold After SPT_CLK (Externally Generated Frame Sync in either Transmit or Receive Mode)[1]	2.7		2.7		ns
t_{SDRE}	Receive Data Setup Before Receive SPT_CLK[1]	2		2		ns
t_{HDRE}	Receive Data Hold After SPT_CLK[1]	2.7		2.7		ns
t_{SCLKW}	SPT_CLK Width[2]	$(0.5 \times t_{SPTCLKEXT}) - 1.5$		$(0.5 \times t_{SPTCLKEXT}) - 1.5$		ns
t_{SPTCLK}	SPT_CLK Period[2]	$t_{SPTCLKEXT} - 1.5$		$t_{SPTCLKEXT} - 1.5$		ns
Switching Characteristics						
t_{DFSE}	Frame Sync Delay After SPT_CLK (Internally Generated Frame Sync in either Transmit or Receive Mode)[3]		19.3		14.5	ns
t_{HOFSE}	Frame Sync Hold After SPT_CLK (Internally Generated Frame Sync in either Transmit or Receive Mode)[3]	2		2		ns
t_{DDTE}	Transmit Data Delay After Transmit SPT_CLK[3]		18.8		14	ns
t_{HDTE}	Transmit Data Hold After Transmit SPT_CLK[3]	2		2		ns

[1] Referenced to sample edge.

[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPT_CLK. For the external SPT_CLK ideal maximum frequency see the $f_{SPTCLKEXT}$ specification in Table 17 on Page 53 in Clock Related Operating Conditions.

[3] Referenced to drive edge.

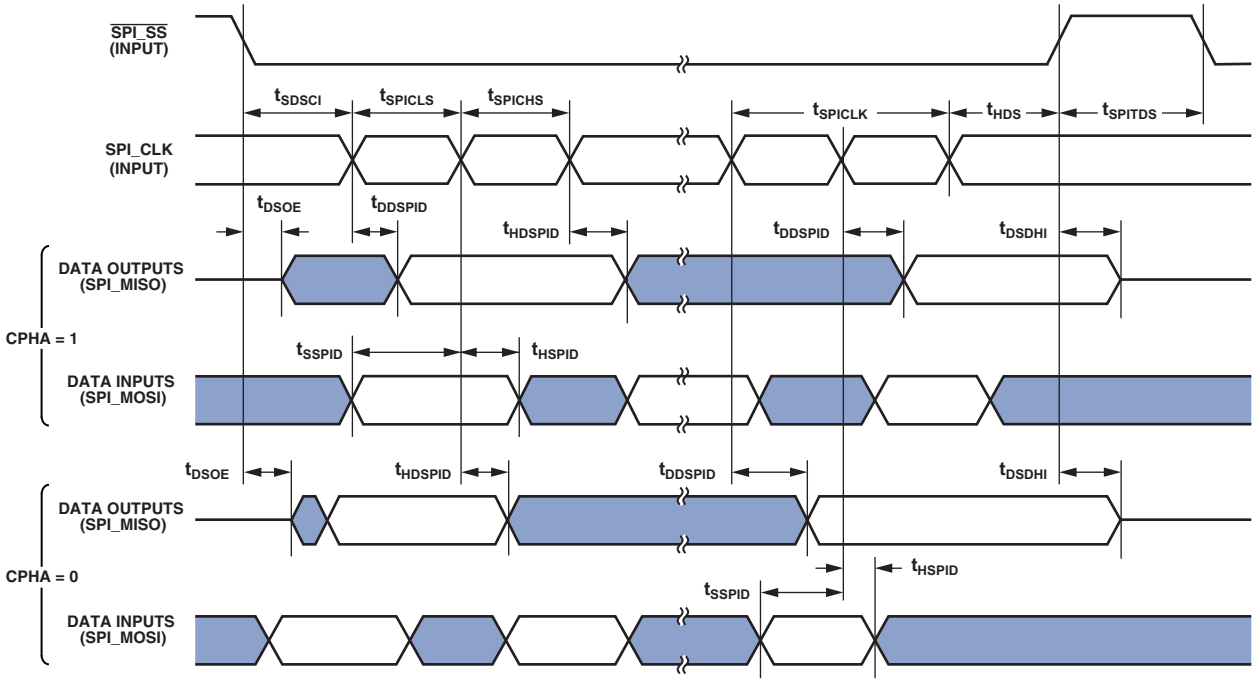


Figure 41. Serial Peripheral Interface (SPI) Port—Slave Timing

Up/Down Counter/Rotary Encoder Timing

Table 59. Up/Down Counter/Rotary Encoder Timing

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirement						
t_{WCOUNT}	Up/Down Counter/Rotary Encoder Input Pulse Width	$2 \times t_{SCLK0}$		$2 \times t_{SCLK0}$		ns

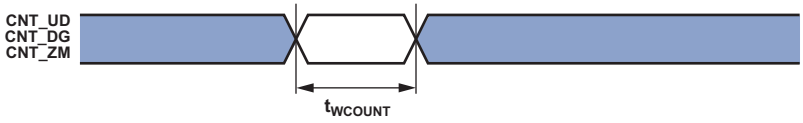


Figure 51. Up/Down Counter/Rotary Encoder Timing

Pulse Width Modulator (PWM) Timing

Table 60 and Figure 52 describe PWM operations.

Table 60. PWM Timing

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirement						
t_{ES}	External Sync Pulse Width			$2 \times t_{SCLK0}$		ns
Switching Characteristics						
t_{DODIS}	Output Inactive (OFF) After Trip Input[1]				15	ns
t_{DOE}	Output Delay After External Sync[1, 2]			$2 \times t_{SCLK0} + 5.5$	$5 \times t_{SCLK0} + 14$	ns

[1] PWM outputs are: PWMx_AH, PWMx_AL, PWMx_BH, PWMx_BL, PWMx_CH, and PWMx_CL.

[2] When the external sync signal is synchronous to the peripheral clock, it takes fewer clock cycles for the output to appear compared to when the external sync signal is asynchronous to the peripheral clock. For more information, see the *ADSP-BF60x Blackfin Processor Hardware Reference*.

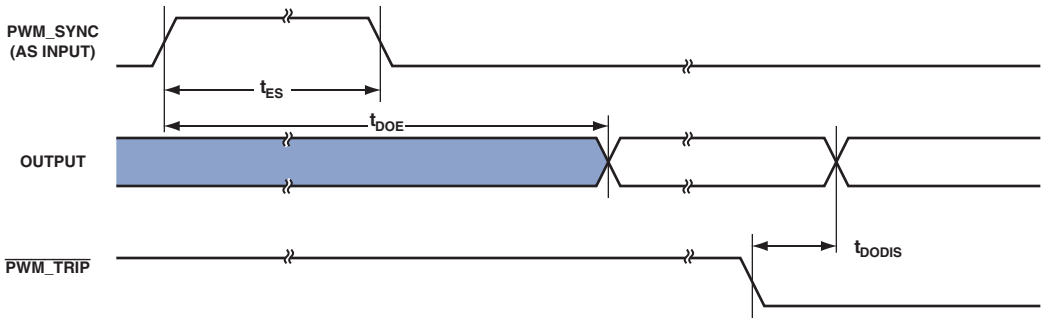


Figure 52. PWM Timing

RSI Controller Timing

Table 63 and Figure 54 describe RSI controller timing.

Table 63. RSI Controller Timing

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{ISU}	Input Setup Time	11		9.6		ns
t_{IH}	Input Hold Time	2		2		ns
Switching Characteristics						
f_{PP}	Clock Frequency Data Transfer Mode[1]		41.67		41.67	MHz
t_{WL}	Clock Low Time	8		8		ns
t_{WH}	Clock High Time	8		8		ns
t_{TLH}	Clock Rise Time		3		3	ns
t_{THL}	Clock Fall Time		3		3	ns
t_{ODLY}	Output Delay Time During Data Transfer Mode		2.5		2.5	ns
t_{OH}	Output Hold Time	–1		–1		ns

[1] $t_{PP} = 1/f_{PP}$

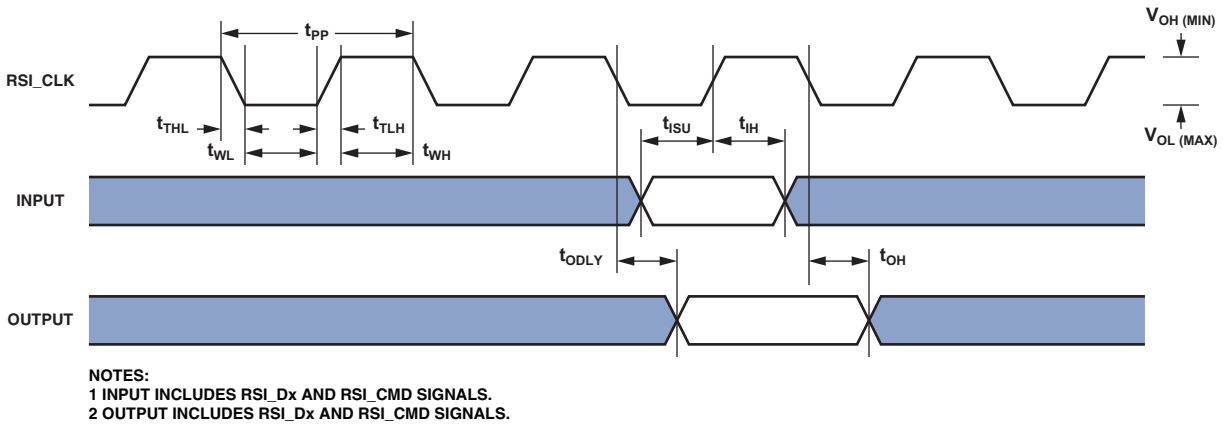


Figure 54. RSI Controller Timing

JTAG Test And Emulation Port Timing

Table 67 and Figure 58 describe JTAG port operations.

Table 67. JTAG Port Timing

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{TCK}	JTG_TCK Period	20		20		ns
t_{STAP}	JTG_TDI, JTG_TMS Setup Before JTG_TCK High	4		4		ns
t_{HTAP}	JTG_TDI, JTG_TMS Hold After JTG_TCK High	4		4		ns
t_{SSYS}	System Inputs Setup Before JTG_TCK High[1]	12		12		ns
t_{HSYS}	System Inputs Hold After JTG_TCK High[1]	5		5		ns
t_{TRSTW}	$\overline{\text{JTG\_TRST}}$ Pulse Width (measured in JTG_TCK cycles)[2]	4		4		T_{CK}
Switching Characteristics						
t_{DTDO}	JTG_TDO Delay from JTG_TCK Low		18		13.5	ns
t_{DSYS}	System Outputs Delay After JTG_TCK Low[3]		22		17	ns

[1] System Inputs = DMC0_DQ00–15, DMC0_LDQS, $\overline{\text{DMC0\_LDQS}}$, DMC0_UDQS, $\overline{\text{DMC0\_UDQS}}$, PA_15–0, PB_15–0, PC_15–0, PD_15–0, PE_15–0, PF_15–0, PG_15–0, SMC0_ARDY_NORWT, $\overline{\text{SMC0\_BR}}$, SMC0_D15–0, SYS_BMODE0–2, $\overline{\text{SYS\_HWRST}}$, SYS_FAULT, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{SYS\_NMI\_RESOUT}}$, SYS_PWRGD, TWI0_SCL, TWI0_SDA, TWI1_SCL, TWI1_SDA.

[2] 50 MHz Maximum.

[3] System Outputs = DMC0_A00–13, DMC0_BA0–2, $\overline{\text{DMC0\_CAS}}$, DMC0_CK, $\overline{\text{DMC0\_CK}}$, DMC0_CKE, $\overline{\text{DMC0\_CS0}}$, DMC0_DQ00–15, DMC0_LDM, DMC0_LDQS, $\overline{\text{DMC0\_LDQS}}$, DMC0_ODT, $\overline{\text{DMC0\_RAS}}$, DMC0_UDM, DMC0_UDQS, $\overline{\text{DMC0\_UDQS}}$, $\overline{\text{DMC0\_WE}}$, $\overline{\text{JTG\_EMU}}$, PA_15–0, PB_15–0, PC_15–0, PD_15–0, PE_15–0, PF_15–0, PG_15–0, $\overline{\text{SMC0\_AMS0}}$, $\overline{\text{SMC0\_AOE\_NORDV}}$, $\overline{\text{SMC0\_ARE}}$, $\overline{\text{SMC0\_AWE}}$, SMC0_A01, SMC0_A02, SMC0_D15–0, SYS_CLKOUT, SYS_FAULT, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{SYS\_NMI\_RESOUT}}$.

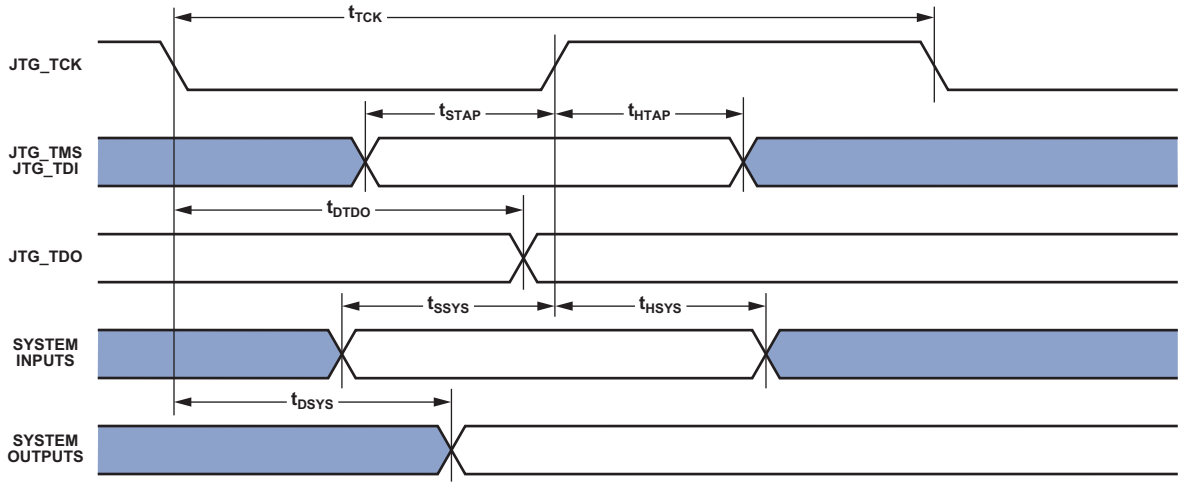


Figure 58. JTAG Port Timing