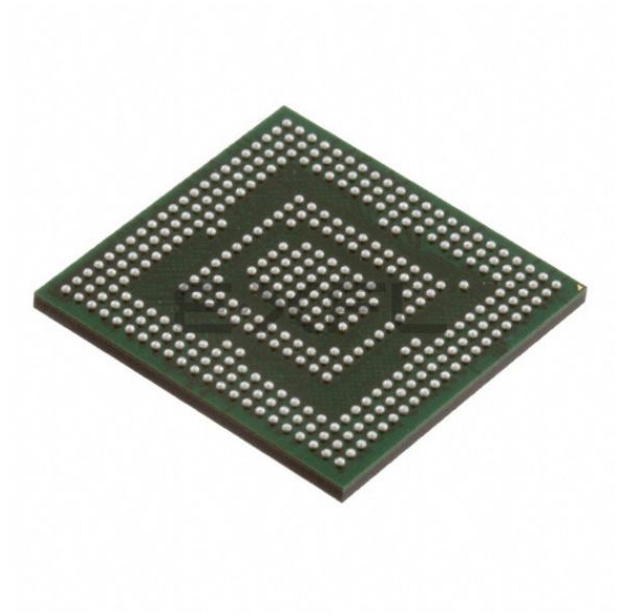

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Dual Core
Interface	CAN, EBI/EMI, Ethernet, I²C, SPI, SPORT, UART/USART, USB OTG
Clock Rate	500MHz
Non-Volatile Memory	ROM (64kB)
On-Chip RAM	808K x 8
Voltage - I/O	1.8V, 3.3V
Voltage - Core	1.25V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	349-LFBGA, CSPBGA
Supplier Device Package	349-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf609bbcz-5

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REVISION HISTORY

2/14—Rev. 0 to Rev. A

Added the system clock output specification and additional peripheral external clocks in Clock Related Operating Conditions on Page 53. These changes affect the following peripheral timing sections.

Enhanced Parallel Peripheral Interface Timing 74
Link Ports 78
Serial Ports—External Clock 80
Serial Peripheral Interface (SPI) Port—Master Timing 86
Serial Peripheral Interface (SPI) Port—Slave Timing 88
ADC Controller Module (ACM) Timing 96

Additional revisions include the following.

Corrected S0SEL and S1SEL in Figure 8 Clock Relationships and Divider Values 54

Revised the dynamic and static current tables CCLK Dynamic Current per core (mA, with ASF = 1) 57
Static Current—IDD_DEEPSLEEP (mA) 58

Corrected the t_{WARE} parameter in Asynchronous Page Mode Read 64

Corrected the timing diagram in Bus Request/Bus Grant . 69

Corrected the signal names in the following figures:
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Added Figure 29 and updated Table 42 in Enhanced Parallel Peripheral Interface Timing 74

Corrected the t_{HSPIDM}, t_{SDSCIM}, t_{SPICLK}, t_{HDSM}, and t_{SPITDM} specifications in Serial Peripheral Interface (SPI) Port—Master Timing 86

Corrected the t_{HDSPID} specification in Serial Peripheral Interface (SPI) Port—Slave Timing 88

Corrected $t_{SRDYSCKM1}$ in Serial Peripheral Interface (SPI) Port—SPI_RDY Timing 92

Revised all parameters in Timer Cycle Timing 94

Corrected the timing diagram in ADC Controller Module (ACM) Timing 96

Removed TWI signals in footnote 3 in JTAG Test And Emulation Port Timing 101

Added models to Automotive Products 112

Memory Protection

The Blackfin cores feature a memory protection concept, which grants data and/or instruction accesses from enabled memory regions only. A supervisor mode vs. user mode programming model supports dynamically varying access rights. Increased flexibility in memory page size options supports a simple method of static memory partitioning.

System Protection

All system resources and L2 memory banks can be controlled by either the processor cores, memory-to-memory DMA, or the system debug unit (SDU). A system protection unit (SPU) enables write accesses to specific resources that are locked to any of four masters: Core 0, Core 1, Memory DMA, and the System Debug Unit. System protection is enabled in greater granularity for some modules (L2, SEC and GPIO controllers) through a *global lock* concept.

Watchpoint Protection

The primary purpose of watchpoints and hardware breakpoints is to serve emulator needs. When enabled, they signal an emulator event whenever user-defined system resources are accessed or a core executes from user-defined addresses. Watchpoint events can be configured such that they signal the events to the other Blackfin core or to the fault management unit.

Dual Watchdog

The two on-chip watchdog timers each may supervise one Blackfin core.

Bandwidth Monitor

All DMA channels that operate in memory-to-memory mode (Memory DMA, PVP Memory Pipe DMA, PIXC DMA) are equipped with a bandwidth monitor mechanism. They can signal a system event or fault when transactions tend to starve because system buses are fully loaded with higher-priority traffic.

Signal Watchdogs

The eight general-purpose timers feature two new modes to monitor off-chip signals. The Watchdog Period mode monitors whether external signals toggle with a period within an expected range. The Watchdog Width mode monitors whether the pulse widths of external signals are in an expected range. Both modes help to detect incorrect undesired toggling (or lack thereof) of system-level signals.

Up/Down Count Mismatch Detection

The up/down counter can monitor external signal pairs, such as request/grant strobes. If the edge count mismatch exceeds the expected range, the up/down counter can flag this to the processor or to the fault management unit.

Fault Management

The fault management unit is part of the system event controller (SEC). Any system event, whether a dual-bit uncorrectable ECC error, or any peripheral status interrupt, can be defined as being a "fault". Additionally, the system events can be defined as an interrupt to the cores. If defined as such, the SEC forwards the event to the fault management unit which may automatically reset the entire device for reboot, or simply toggle the SYS_FAULT output pins to signal off-chip hardware. Optionally, the fault management unit can delay the action taken via a keyed sequence, to provide a final chance for the Blackfin cores to resolve the crisis and to prevent the fault action from being taken.

ADDITIONAL PROCESSOR PERIPHERALS

The processor contains a rich set of peripherals connected to the core via several high-bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the block diagram on Page 1). The processors contain high-speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

The following sections describe additional peripherals that were not described in the previous sections.

Timers

The processor includes several timers which are described in the following sections.

General-Purpose Timers

There is one GP timer unit and it provides eight general-purpose programmable timers. Each timer has an external pin that can be configured either as a pulse width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input on the TMRx pins, an external clock TMRCLK input pin, or to the internal SCLK0.

The timer units can be used in conjunction with the UARTs and the CAN controller to measure the width of the pulses in the data stream to provide a software auto-baud detect function for the respective serial channels.

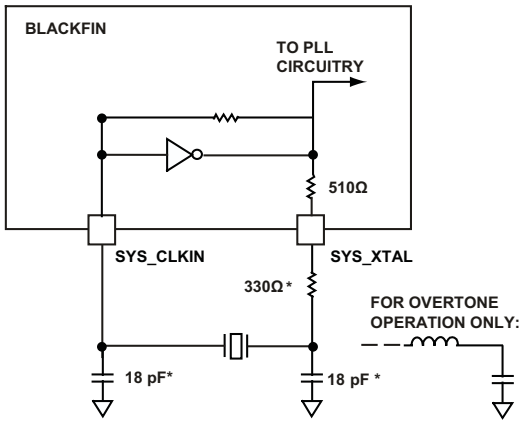
The timers can generate interrupts to the processor core, providing periodic events for synchronization to either the system clock or to external signals. Timer events can also trigger other peripherals via the TRU (for instance, to signal a fault).

Core Timers

Each processor core also has its own dedicated timer. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generating periodic operating system interrupts.

Watchdog Timers

Each core includes a 32-bit timer, which may be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state, via generation of a hardware reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before



NOTE: VALUES MARKED WITH * MUST BE CUSTOMIZED, DEPENDING ON THE CRYSTAL AND LAYOUT. PLEASE ANALYZE CAREFULLY. FOR FREQUENCIES ABOVE 33 MHz, THE SUGGESTED CAPACITOR VALUE OF 18pF SHOULD BE TREATED AS A MAXIMUM, AND THE SUGGESTED RESISTOR VALUE SHOULD BE REDUCED TO 0 Ω.

Figure 6. External Crystal Connection

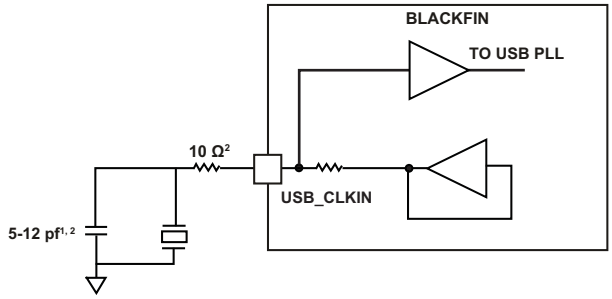
The two capacitors and the series resistor shown in Figure 6 fine tune phase and amplitude of the sine frequency. The capacitor and resistor values shown in Figure 6 are typical values only. The capacitor values are dependent upon the crystal manufacturers' load capacitance recommendations and the PCB physical layout. The resistor value depends on the drive level specified by the crystal manufacturer. The user should verify the customized values based on careful investigations on multiple devices over temperature range.

A third-overtone crystal can be used for frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone by adding a tuned inductor circuit as shown in Figure 6. A design procedure for third-overtone operation is discussed in detail in application note (EE-168) Using Third Overtone Crystals with the ADSP-218x DSP on the Analog Devices website (www.analog.com)—use site search on "EE-168."

USB Crystal Oscillator

The USB can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator. If an external clock is used, it should be a TTL compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor's USB_CLKIN pin. Alternatively, because the processor includes an on-chip oscillator circuit, an external crystal may be used.

For fundamental frequency operation, use the circuit shown in Figure 7. A parallel-resonant, fundamental frequency, microprocessor grade crystal is connected between the USB_CLKIN pin and ground. A load capacitor is placed in parallel with the crystal. The combined capacitive value of the board trace parasitic, the case capacitance of the crystal (from crystal manufacturer) and the parallel capacitor in the diagram should be in the range of 8 pF to 15 pF.



NOTES:
1. CAPACITANCE VALUE SHOWN INCLUDES BOARD PARASITICS
2. VALUES ARE A PRELIMINARY ESTIMATE.

Figure 7. External USB Crystal Connection

The crystal should be chosen so that its rated load capacitance matches the nominal total capacitance on this node. A series resistor may be added between the USB_CLKIN pin and the parallel crystal and capacitor combination, in order to further reduce the drive level of the crystal.

The parallel capacitor and the series resistor shown in Figure 7 fine tune phase and amplitude of the sine frequency. The capacitor and resistor values shown in Figure 7 are typical values only. The capacitor values are dependent upon the crystal manufacturers' load capacitance recommendations and the PCB physical layout. The resistor value depends on the drive level specified by the crystal manufacturer. The user should verify the customized values based on careful investigations on multiple devices over temperature range.

Clock Generation

The clock generation unit (CGU) generates all on-chip clocks and synchronization signals. Multiplication factors are programmed to the PLL to define the PLLCLK frequency. Programmable values divide the PLLCLK frequency to generate the core clock (CCLK), the system clocks (SYSCLK, SCLK0 and SCLK1), the LPDDR or DDR2 clock (DCLK) and the output clock (OCLK). This is illustrated in Figure 8 on Page 54.

Writing to the CGU control registers does not affect the behavior of the PLL immediately. Registers are first programmed with a new value, and the PLL logic executes the changes so that it transitions smoothly from the current conditions to the new ones.

SYS_CLKIN oscillations start when power is applied to the V_{DD_EXT} pins. The rising edge of $\overline{\text{SYS\_HWRST}}$ can be applied after all voltage supplies are within specifications (see Operating Conditions on Page 52), and SYS_CLKIN oscillations are stable.

Clock Out/External Clock

The SYS_CLKOUT output pin has programmable options to output divided-down versions of the on-chip clocks. By default, the SYS_CLKOUT pin drives a buffered version of the SYS_CLKIN input. Clock generation faults (for example PLL unlock) may trigger a reset by hardware. The clocks shown in Table 3 can be outputs from SYS_CLKOUT.

349-BALL CSP_BGA SIGNAL DESCRIPTIONS

The processors' pin definitions are shown in the table. The columns in this table provide the following information:

- Signal Name: The Signal Name column in the table includes the Signal Name for every pin.
- Description: The Description column in the table provides a verbose (descriptive) name for the signal.
- Port: The General-Purpose I/O Port column in the table shows whether or not the signal is multiplexed with other signals on a general-purpose I/O port pin.
- Pin Name: The Pin Name column in the table identifies the name of the package pin (at power-on reset) on which the signal is located (if a single function pin) or is multiplexed (if a general-purpose I/O pin).

Table 7. ADSP-BF60x 349-Ball CSP_BGA Signal Descriptions

Signal Name	Description	Port	Pin Name
ACM0_A0	ACM0 Address 0	F	PF_14
ACM0_A1	ACM0 Address 1	F	PF_15
ACM0_A2	ACM0 Address 2	F	PF_12
ACM0_A3	ACM0 Address 3	F	PF_13
ACM0_A4	ACM0 Address 4	F	PF_10
ACM0_CLK	ACM0 Clock	E	PE_04
ACM0_FS	ACM0 Frame Sync	E	PE_03
ACM0_T0	ACM0 External Trigger 0	E	PE_08
ACM0_T1	ACM0 External Trigger 1	G	PG_05
CAN0_RX	CAN0 Receive	G	PG_04
CAN0_TX	CAN0 Transmit	G	PG_01
CNT0_DG	CNT0 Count Down and Gate	G	PG_12
CNT0_UD	CNT0 Count Up and Direction	G	PG_11
CNT0_ZM	CNT0 Count Zero Marker	G	PG_07
DMC0_A00	DMC Address 0	Not Muxed	DMC0_A00
DMC0_A01	DMC Address 1	Not Muxed	DMC0_A01
DMC0_A02	DMC Address 2	Not Muxed	DMC0_A02
DMC0_A03	DMC Address 3	Not Muxed	DMC0_A03
DMC0_A04	DMC Address 4	Not Muxed	DMC0_A04
DMC0_A05	DMC Address 5	Not Muxed	DMC0_A05
DMC0_A06	DMC Address 6	Not Muxed	DMC0_A06
DMC0_A07	DMC Address 7	Not Muxed	DMC0_A07
DMC0_A08	DMC Address 8	Not Muxed	DMC0_A08
DMC0_A09	DMC Address 9	Not Muxed	DMC0_A09
DMC0_A10	DMC Address 10	Not Muxed	DMC0_A10
DMC0_A11	DMC Address 11	Not Muxed	DMC0_A11
DMC0_A12	DMC Address 12	Not Muxed	DMC0_A12
DMC0_A13	DMC Address 13	Not Muxed	DMC0_A13
DMC0_BA0	DMC Bank Address Input 0	Not Muxed	DMC0_BA0
DMC0_BA1	DMC Bank Address Input 1	Not Muxed	DMC0_BA1
DMC0_BA2	DMC Bank Address Input 2	Not Muxed	DMC0_BA2
$\overline{\text{DMC0\_CAS}}$	DMC Column Address Strobe	Not Muxed	$\overline{\text{DMC0\_CAS}}$
DMC0_CK	DMC Clock	Not Muxed	DMC0_CK
DMC0_CKE	DMC Clock Enable	Not Muxed	DMC0_CKE
$\overline{\text{DMC0\_CK}}$	DMC Clock (complement)	Not Muxed	$\overline{\text{DMC0\_CK}}$
$\overline{\text{DMC0\_CS0}}$	DMC Chip Select 0	Not Muxed	$\overline{\text{DMC0\_CS0}}$

Table 7. ADSP-BF60x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
PWM1_AH	PWM1 Channel A High Side	G	PG_03
PWM1_AL	PWM1 Channel A Low Side	G	PG_02
PWM1_BH	PWM1 Channel B High Side	G	PG_00
PWM1_BL	PWM1 Channel B Low Side	E	PE_15
PWM1_CH	PWM1 Channel C High Side	E	PE_13
PWM1_CL	PWM1 Channel C Low Side	E	PE_12
PWM1_DH	PWM1 Channel D High Side	E	PE_11
PWM1_DL	PWM1 Channel D Low Side	E	PE_10
PWM1_SYNC	PWM1 Sync	G	PG_05
$\overline{\text{PWM1\_TRIP0}}$	PWM1 Shutdown Input 0	G	PG_06
$\overline{\text{PWM1\_TRIP1}}$	PWM1 Shutdown Input 1	G	PG_08
RSI0_CLK	RSI0 Clock	G	PG_06
RSI0_CMD	RSI0 Command	G	PG_05
RSI0_D0	RSI0 Data 0	G	PG_03
RSI0_D1	RSI0 Data 1	G	PG_02
RSI0_D2	RSI0 Data 2	G	PG_00
RSI0_D3	RSI0 Data 3	E	PE_15
RSI0_D4	RSI0 Data 4	E	PE_13
RSI0_D5	RSI0 Data 5	E	PE_12
RSI0_D6	RSI0 Data 6	E	PE_10
RSI0_D7	RSI0 Data 7	E	PE_11
SMC0_A01	SMC0 Address 1	Not Muxed	SMC0_A01
SMC0_A02	SMC0 Address 2	Not Muxed	SMC0_A02
SMC0_A03	SMC0 Address 3	A	PA_00
SMC0_A04	SMC0 Address 4	A	PA_01
SMC0_A05	SMC0 Address 5	A	PA_02
SMC0_A06	SMC0 Address 6	A	PA_03
SMC0_A07	SMC0 Address 7	A	PA_04
SMC0_A08	SMC0 Address 8	A	PA_05
SMC0_A09	SMC0 Address 9	A	PA_06
SMC0_A10	SMC0 Address 10	A	PA_07
SMC0_A11	SMC0 Address 11	A	PA_08
SMC0_A12	SMC0 Address 12	A	PA_09
SMC0_A13	SMC0 Address 13	B	PB_02
SMC0_A14	SMC0 Address 14	A	PA_10
SMC0_A15	SMC0 Address 15	A	PA_11
SMC0_A16	SMC0 Address 16	B	PB_03
SMC0_A17	SMC0 Address 17	A	PA_12
SMC0_A18	SMC0 Address 18	A	PA_13
SMC0_A19	SMC0 Address 19	A	PA_14
SMC0_A20	SMC0 Address 20	A	PA_15
SMC0_A21	SMC0 Address 21	B	PB_06
SMC0_A22	SMC0 Address 22	B	PB_07
SMC0_A23	SMC0 Address 23	B	PB_08
SMC0_A24	SMC0 Address 24	B	PB_10
SMC0_A25	SMC0 Address 25	B	PB_11

Table 7. ADSP-BF60x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SMC0_ABE0	SMC0 Byte Enable 0	B	PB_04
SMC0_ABE1	SMC0 Byte Enable 1	B	PB_05
SMC0_AMS0	SMC0 Memory Select 0	Not Muxed	SMC0_AMS0
SMC0_AMS1	SMC0 Memory Select 1	B	PB_01
SMC0_AMS2	SMC0 Memory Select 2	B	PB_04
SMC0_AMS3	SMC0 Memory Select 3	B	PB_05
SMC0_AOE	SMC0 Output Enable	Not Muxed	SMC0_AOE_NORDV
SMC0_ARDY	SMC0 Asynchronous Ready	Not Muxed	SMC0_ARDY_NORWT
SMC0_ARE	SMC0 Read Enable	Not Muxed	SMC0_ARE
SMC0_AWE	SMC0 Write Enable	Not Muxed	SMC0_AWE
SMC0_BGH	SMC0 Bus Grant Hang	B	PB_09
SMC0_BG	SMC0 Bus Grant	B	PB_12
SMC0_BR	SMC0 Bus Request	Not Muxed	SMC0_BR
SMC0_D00	SMC0 Data 0	Not Muxed	SMC0_D00
SMC0_D01	SMC0 Data 1	Not Muxed	SMC0_D01
SMC0_D02	SMC0 Data 2	Not Muxed	SMC0_D02
SMC0_D03	SMC0 Data 3	Not Muxed	SMC0_D03
SMC0_D04	SMC0 Data 4	Not Muxed	SMC0_D04
SMC0_D05	SMC0 Data 5	Not Muxed	SMC0_D05
SMC0_D06	SMC0 Data 6	Not Muxed	SMC0_D06
SMC0_D07	SMC0 Data 7	Not Muxed	SMC0_D07
SMC0_D08	SMC0 Data 8	Not Muxed	SMC0_D08
SMC0_D09	SMC0 Data 9	Not Muxed	SMC0_D09
SMC0_D10	SMC0 Data 10	Not Muxed	SMC0_D10
SMC0_D11	SMC0 Data 11	Not Muxed	SMC0_D11
SMC0_D12	SMC0 Data 12	Not Muxed	SMC0_D12
SMC0_D13	SMC0 Data 13	Not Muxed	SMC0_D13
SMC0_D14	SMC0 Data 14	Not Muxed	SMC0_D14
SMC0_D15	SMC0 Data 15	Not Muxed	SMC0_D15
SMC0_NORCLK	SMC0 NOR Clock	B	PB_00
SMC0_NORDV	SMC0 NOR Data Valid	Not Muxed	SMC0_AOE_NORDV
SMC0_NORWT	SMC0 NOR Wait	Not Muxed	SMC0_ARDY_NORWT
SPI0_CLK	SPI0 Clock	D	PD_04
SPI0_D2	SPI0 Data 2	D	PD_00
SPI0_D3	SPI0 Data 3	D	PD_01
SPI0_MISO	SPI0 Master In, Slave Out	D	PD_02
SPI0_MOSI	SPI0 Master Out, Slave In	D	PD_03
SPI0_RDY	SPI0 Ready	D	PD_10
SPI0_SEL1	SPI0 Slave Select Output 1	D	PD_11
SPI0_SEL2	SPI0 Slave Select Output 2	D	PD_01
SPI0_SEL3	SPI0 Slave Select Output 3	D	PD_00
SPI0_SEL4	SPI0 Slave Select Output 4	C	PC_15
SPI0_SEL5	SPI0 Slave Select Output 5	D	PD_09
SPI0_SEL6	SPI0 Slave Select Output 6	C	PC_13
SPI0_SEL7	SPI0 Slave Select Output 7	C	PC_12
SPI0_SS	SPI0 Slave Select Input	D	PD_11

Table 7. ADSP-BF60x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
UART0_RX	UART0 Receive	D	PD_08
UART0_TX	UART0 Transmit	D	PD_07
UART1_CTS	UART1 Clear to Send	G	PG_13
UART1_RTS	UART1 Request to Send	G	PG_10
UART1_RX	UART1 Receive	G	PG_14
UART1_TX	UART1 Transmit	G	PG_15
USB0_CLKIN	USB0 Clock/Crystal Input	Not Muxed	USB0_CLKIN
USB0_DM	USB0 Data –	Not Muxed	USB0_DM
USB0_DP	USB0 Data +	Not Muxed	USB0_DP
USB0_ID	USB0 OTG ID	Not Muxed	USB0_ID
USB0_VBC	USB0 VBUS Control	Not Muxed	USB0_VBC
USB0_VBUS	USB0 Bus Voltage	Not Muxed	USB0_VBUS
VDD_DMC	VDD for DMC	Not Muxed	VDD_DMC
VDD_EXT	External VDD	Not Muxed	VDD_EXT
VDD_INT	Internal VDD	Not Muxed	VDD_INT
VDD_TD	VDD for Thermal Diode	Not Muxed	VDD_TD
VDD_USB	VDD for USB	Not Muxed	VDD_USB
VREF_DMC	VREF for DMC	Not Muxed	VREF_DMC

GP I/O MULTIPLEXING FOR 349-BALL CSP_BGA

Table 8 through Table 14 identifies the pin functions that are multiplexed on the general-purpose I/O pins of the 349-ball CSP_BGA package.

Table 8. Signal Multiplexing for Port A

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function Input Tap
PA_00	SMC0_A03	PPI2_D00	LP0_D0	
PA_01	SMC0_A04	PPI2_D01	LP0_D1	
PA_02	SMC0_A05	PPI2_D02	LP0_D2	
PA_03	SMC0_A06	PPI2_D03	LP0_D3	
PA_04	SMC0_A07	PPI2_D04	LP0_D4	
PA_05	SMC0_A08	PPI2_D05	LP0_D5	
PA_06	SMC0_A09	PPI2_D06	LP0_D6	
PA_07	SMC0_A10	PPI2_D07	LP0_D7	
PA_08	SMC0_A11	PPI2_D08	LP1_D0	
PA_09	SMC0_A12	PPI2_D09	LP1_D1	
PA_10	SMC0_A14	PPI2_D10	LP1_D2	
PA_11	SMC0_A15	PPI2_D11	LP1_D3	
PA_12	SMC0_A17	PPI2_D12	LP1_D4	
PA_13	SMC0_A18	PPI2_D13	LP1_D5	
PA_14	SMC0_A19	PPI2_D14	LP1_D6	
PA_15	SMC0_A20	PPI2_D15	LP1_D7	

Table 9. Signal Multiplexing for Port B

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function Input Tap
PB_00	SMC0_NORCLK	PPI2_CLK	LP0_CLK	
PB_01	$\overline{\text{SMC0\_AMS1}}$	PPI2_FS1	LP0_ACK	
PB_02	SMC0_A13	PPI2_FS2	LP1_ACK	
PB_03	SMC0_A16	PPI2_FS3	LP1_CLK	
PB_04	$\overline{\text{SMC0\_AMS2}}$	$\overline{\text{SMC0\_ABE0}}$	SPT0_AFS	
PB_05	$\overline{\text{SMC0\_AMS3}}$	$\overline{\text{SMC0\_ABE1}}$	SPT0_ACLK	
PB_06	SMC0_A21	SPT0_ATDV		TM0_ACLK4
PB_07	SMC0_A22	PPI2_D16	SPT0_BFS	
PB_08	SMC0_A23	PPI2_D17	SPT0_BCLK	
PB_09	$\overline{\text{SMC0\_BGH}}$		SPT0_AD0	TM0_ACLK2
PB_10	SMC0_A24		SPT0_BD1	TM0_ACLK0
PB_11	SMC0_A25		SPT0_BD0	TM0_ACLK3
PB_12	$\overline{\text{SMC0\_BG}}$	SPT0_BTDV	SPT0_AD1	TM0_ACLK1
PB_13	ETH0_TXEN	PPI1_FS1		TM0_ACI6
PB_14	ETH0_REFCLK	PPI1_CLK		
PB_15	ETH0_PTPPPS	PPI1_FS3		

ADSP-BF60x DESIGNER QUICK REFERENCE

The table provides a quick reference summary of pin related information for circuit board design. The columns in this table provide the following information:

- Signal Name: The Signal Name column in the table includes the Signal Name for every pin.
- Type: The Pin Type column in the table identifies the I/O type or supply type of the pin. The abbreviations used in this column are na (None), I/O (Digital input and/or output), a (Analog), s (Supply), and g (Ground).
- Driver Type: The Driver Type column in the table identifies the driver type used by the pin. The driver types are defined in Output Drive Currents on Page 102.
- Int Term: The Internal Termination column in the table specifies the termination present when the processor is not in the reset or hibernate state. The abbreviations used in this column are wk (Weak Keeper, weakly retains previous value driven on the pin), pu (Pull-up resistor), or pd (Pull-down resistor).
- Reset Term: The Reset Termination column in the table specifies the termination present when the processor is in the reset state. The abbreviations used in this column are wk (Weak Keeper, weakly retains previous value driven on the pin), pu (Pull-up resistor), or pd (Pull-down resistor).
- Reset Drive: The Reset Drive column in the table specifies the active drive on the signal when the processor is in the reset state.
- Hiber Term: The Hibernate Termination column in the table specifies the termination present when the processor is in the hibernate state. The abbreviations used in this column are wk (Weak Keeper, weakly retains previous value driven on the pin), pu (Pull-up resistor), or pd (Pull-down resistor).
- Hiber Drive: The Hibernate Drive column in the table specifies the active drive on the signal when the processor is in the hibernate state.
- Power Domain: The Power Domain column in the table specifies the power supply domain in which the signal resides.
- Description and Notes: The Description and Notes column in the table identifies any special requirements or characteristics for the signal. If no special requirements are listed the signal may be left unconnected if it is not used. Also, for multiplexed general-purpose I/O pins, this column identifies the functions available on the pin.

Table 15. ADSP-BF60x Designer Quick Reference

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
DMC0_A00	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 0. Notes: No notes.
DMC0_A01	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 1. Notes: No notes.
DMC0_A02	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 2. Notes: No notes.
DMC0_A03	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 3. Notes: No notes.
DMC0_A04	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 4. Notes: No notes.
DMC0_A05	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 5. Notes: No notes.
DMC0_A06	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 6. Notes: No notes.
DMC0_A07	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 7. Notes: No notes.
DMC0_A08	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 8. Notes: No notes.
DMC0_A09	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 9. Notes: No notes.
DMC0_A10	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 10. Notes: No notes.

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PA_00	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 0 | SMC0 Address 3 | EPPI2 Data 0 | LP0 Data 0. Notes: No notes.
PA_01	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 1 | SMC0 Address 4 | EPPI2 Data 1 | LP0 Data 1. Notes: No notes.
PA_02	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 2 | SMC0 Address 5 | EPPI2 Data 2 | LP0 Data 2. Notes: No notes.
PA_03	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 3 | SMC0 Address 6 | EPPI2 Data 3 | LP0 Data 3. Notes: No notes.
PA_04	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 4 | SMC0 Address 7 | EPPI2 Data 4 | LP0 Data 4. Notes: No notes.
PA_05	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 5 | SMC0 Address 8 | EPPI2 Data 5 | LP0 Data 5. Notes: No notes.
PA_06	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 6 | SMC0 Address 9 | EPPI2 Data 6 | LP0 Data 6. Notes: No notes.
PA_07	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 7 | SMC0 Address 10 | EPPI2 Data 7 | LP0 Data 7. Notes: No notes.
PA_08	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 8 | SMC0 Address 11 | EPPI2 Data 8 | LP1 Data 0. Notes: No notes.
PA_09	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 9 | SMC0 Address 12 | EPPI2 Data 9 | LP1 Data 1. Notes: No notes.
PA_10	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 10 | SMC0 Address 14 | EPPI2 Data 10 | LP1 Data 2. Notes: No notes.
PA_11	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 11 | SMC0 Address 15 | EPPI2 Data 11 | LP1 Data 3. Notes: No notes.
PA_12	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 12 | SMC0 Address 17 | EPPI2 Data 12 | LP1 Data 4. Notes: No notes.
PA_13	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 13 | SMC0 Address 18 | EPPI2 Data 13 | LP1 Data 5. Notes: No notes.
PA_14	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 14 | SMC0 Address 19 | EPPI2 Data 14 | LP1 Data 6. Notes: No notes.
PA_15	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PA Position 15 | SMC0 Address 20 | EPPI2 Data 15 | LP1 Data 7. Notes: May be used to wake the processor from hibernate or deep sleep mode.

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
USB0_DP	I/O	F	none	none	none	none	none	VDD_USB	Desc: USB0 Data +. Notes: Pull low if not using USB. For complete documentation of hibernate behavior when USB is used, see the USB chapter in the processor hardware reference.
USB0_ID	I/O	na	none	none	none	pu	none	VDD_USB	Desc: USB0 OTG ID. Notes: If USB is not used, connect to ground. When USB is being used, the internal pull-up resistor that is present during hibernate is programmable. See the USB chapter in the processor hardware reference. Active during reset.
USB0_VBC	I/O	E	none	none	none	wk	none	VDD_USB	Desc: USB0 VBUS Control. Notes: If USB is not used, pull low.
USB0_VBUS	I/O	G	none	none	none	none	none	VDD_USB	Desc: USB0 Bus Voltage. Notes: If USB is not used, connect to ground.
VDD_DMC	s	na	none	none	none	none	none	na	Desc: VDD for DMC. Notes: If the DMC is not used, connect to VDD_INT.
VDD_EXT	s	na	none	none	none	none	none	na	Desc: External VDD. Notes: Must be powered.
VDD_INT	s	na	none	none	none	none	none	na	Desc: Internal VDD. Notes: Must be powered.
VDD_TD	s	na	none	none	none	none	none	na	Desc: VDD for Thermal Diode. Notes: If the thermal diode is not used, connect to ground.
VDD_USB	s	na	none	none	none	none	none	na	Desc: VDD for USB. Notes: If USB is not used, connect to VDD_EXT.
VREF_DMC	s	na	none	none	none	none	none	na	Desc: VREF for DMC. Notes: If the DMC is not used, connect to VDD_INT.

PROCESSOR — ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 23 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 23. Absolute Maximum Ratings

Parameter	Rating
Internal Supply Voltage (V_{DD_INT})	–0.33 V to 1.32 V
External (I/O) Supply Voltage (V_{DD_EXT})	–0.33 V to 3.63 V
Thermal Diode Supply Voltage (V_{DD_TD})	–0.33 V to 3.63 V
DDR2 Controller Supply Voltage (V_{DD_DMC})	–0.33 V to 1.90 V
USB PHY Supply Voltage (V_{DD_USB})	–0.33 V to 3.63 V
Input Voltage[1, 2, 3]	–0.33 V to 3.63 V
TWI Input Voltage[2, 4]	–0.33 V to 5.50 V
USB0_Dx Input Voltage[5]	–0.33 V to 5.25 V
USB0_VBUS Input Voltage[5]	–0.33 V to 6.00 V
DDR2 Input Voltage[6]	–0.33 V to 1.90 V
Output Voltage Swing	–0.33 V to V_{DD_EXT} + 0.5 V
I_{OH}/I_{OL} Current per Signal[1]	12.5 mA (max)
Storage Temperature Range	–65°C to +150°C
Junction Temperature Under Bias	+125°C

[1] Applies to 100% transient duty cycle.
[2] Applies only when V_{DD_EXT} is within specifications. When V_{DD_EXT} is outside specifications, the range is V_{DD_EXT} ± 0.2 V.
[3] For other duty cycles see Table 24.
[4] Applies to balls TWI_SCL and TWI_SDA.
[5] If the USB is not used, connect USB0_Dx and USB0_VBUS according to Table 15 on Page 37.
[6] Applies only when V_{DD_DMC} is within specifications. When V_{DD_DMC} is outside specifications, the range is V_{DD_DMC} ± 0.2 V.

Table 24. Maximum Duty Cycle for Input Transient Voltage[1, 2]

Maximum Duty Cycle (%)[2]	V_{IN} Min (V)[3]	V_{IN} Max (V)[3]
100	–0.33	3.63
50	–0.50	3.80
40	–0.56	3.86
25	–0.67	3.97
20	–0.73	4.03
15	–0.80	4.10
10	–0.90	4.20

[1] Applies to all signal balls with the exception of SYS_CLKIN, SYS_XTAL, SYS_EXT_WAKE, USB0_DP, USB0_DM, USB0_VBUS, TWI signals, and DMC0 signals.
[2] Applies only when V_{DD_EXT} is within specifications. When V_{DD_EXT} is outside specifications, the range is V_{DD_EXT} ± 0.2 V.
[3] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the specified voltages, and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PROCESSOR — PACKAGE INFORMATION

The information presented in Figure 9 and Table 25 provides details about package branding. For a complete listing of product availability, see Automotive Products on Page 112.

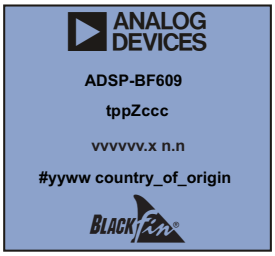


Figure 9. Product Information on Package

Table 25. Package Brand Information

Brand Key	Field Description
ADSP-BF609	Product Model
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Designation
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

Enhanced Parallel Peripheral Interface Timing

The following tables and figures describe enhanced parallel peripheral interface timing operations. The POLC bits in the EPPI_CTL register may be used to set the sampling/driving edges of the EPPI clock.

When internally generated, the programmed PPI clock ($f_{PCLKPROG}$) frequency in MHz is set by the following equation where VALUE is a field in the EPPI_CLKDIV register that can be set from 0 to 65535:

$$f_{PCLKPROG} = \frac{f_{SCLK0}}{(VALUE + 1)}$$

$$t_{PCLKPROG} = \frac{1}{f_{PCLKPROG}}$$

When externally generated the EPPI_CLK is called $f_{PCLKEXT}$:

$$t_{PCLKEXT} = \frac{1}{f_{PCLKEXT}}$$

Table 42. Enhanced Parallel Peripheral Interface—Internal Clock

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{SFSPI}	External FS Setup Before EPPI_CLK	7.9		6.5		ns
t_{HFSPI}	External FS Hold After EPPI_CLK	0		0		ns
t_{SDRPI}	Receive Data Setup Before EPPI_CLK	7.9		6.5		ns
t_{HDRPI}	Receive Data Hold After EPPI_CLK	0		0		ns
t_{SFS3GI}	External FS3 Input Setup Before EPPI_CLK Fall Edge in Clock Gating Mode	15.4		14		ns
t_{HFS3GI}	External FS3 Input Hold Before EPPI_CLK Fall Edge in Clock Gating Mode	0		0		ns
Switching Characteristics						
t_{PCLKW}	EPPI_CLK Width[1]	0.5 × $t_{PCLKPROG}$ – 1		0.5 × $t_{PCLKPROG}$ – 1		ns
t_{PCLK}	EPPI_CLK Period[1]	$t_{PCLKPROG}$ – 1		$t_{PCLKPROG}$ – 1		ns
t_{DFSPI}	Internal FS Delay After EPPI_CLK		3.5		3.5	ns
t_{HOFSPI}	Internal FS Hold After EPPI_CLK	–0.5		–0.5		ns
t_{DDTPI}	Transmit Data Delay After EPPI_CLK		3.5		3.5	ns
t_{HDTPI}	Transmit Data Hold After EPPI_CLK	–0.5		–0.5		ns

[1] See Table 17 on Page 53 in Clock Related Operating Conditions for details on the minimum period that may be programmed for $t_{PCLKPROG}$.

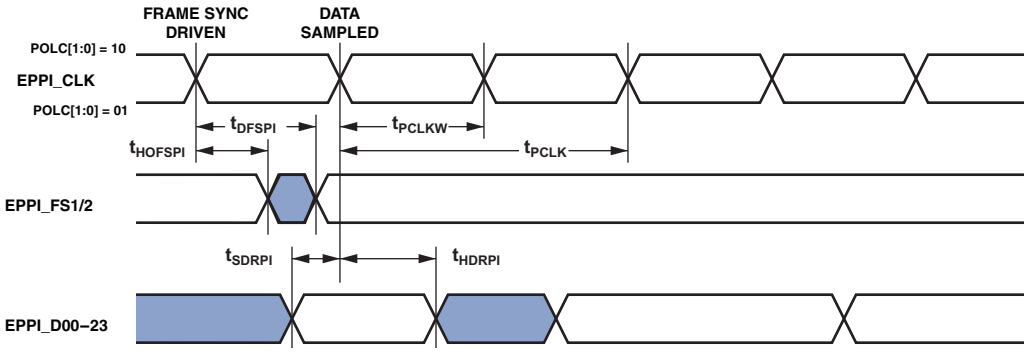
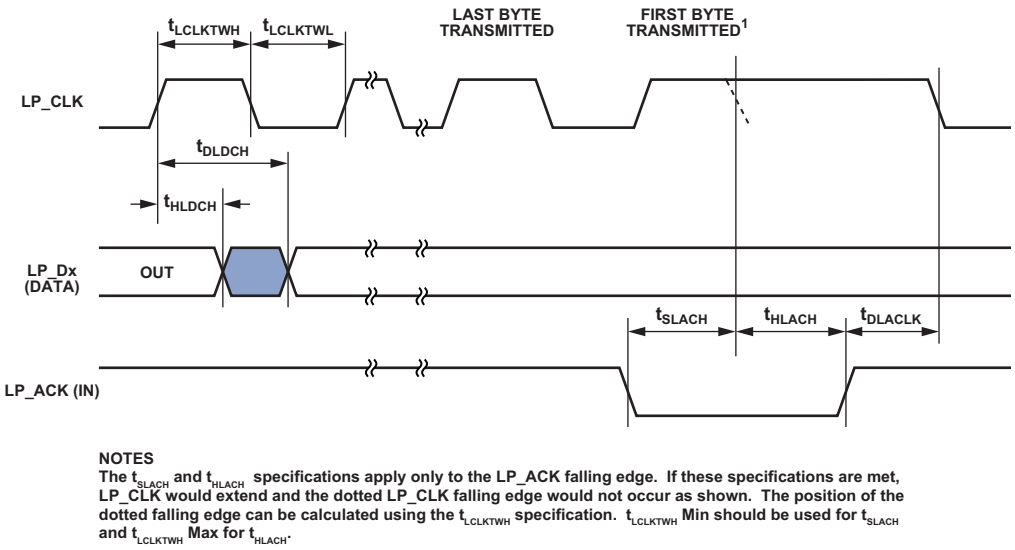


Figure 25. PPI Internal Clock GP Receive Mode with Internal Frame Sync Timing

Table 45. Link Ports—Transmit

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{SLACH}	LP_ACK Setup Before LP_CLK Low	$2 \times t_{SCLK0} + 17.5$		$2 \times t_{SCLK0} + 13.5$		ns
t_{HLACH}	LP_ACK Hold After LP_CLK Low	0		0		ns
Switching Characteristics						
t_{DLDCH}	Data Delay After LP_CLK High		2.5		2.5	ns
t_{HLDCH}	Data Hold After LP_CLK High	–1.5		–1.5		ns
$t_{LCLKTWL}$[1]	LP_CLK Width Low	$0.4 \times t_{LCLKTPROG}$	$0.6 \times t_{LCLKTPROG}$	$0.4 \times t_{LCLKTPROG}$	$0.6 \times t_{LCLKTPROG}$	ns
$t_{LCLKTWH}$[1]	LP_CLK Width High	$0.4 \times t_{LCLKTPROG}$	$0.6 \times t_{LCLKTPROG}$	$0.4 \times t_{LCLKTPROG}$	$0.6 \times t_{LCLKTPROG}$	ns
t_{LCLKTW}[1]	LP_CLK Period	$t_{LCLKTPROG} - 1.2$		$t_{LCLKTPROG} - 1.2$		ns
t_{DLACLK}	LP_CLK Low Delay After LP_ACK High	$t_{SCLK0} + 4$	$(2 \times t_{SCLK0}) + t_{LCLK} + 10$	$t_{SCLK0} + 4$	$(2 \times t_{SCLK0}) + t_{LCLK} + 10$	ns

[1] See Table 17 on Page 53 in Clock Related Operating Conditions for details on the minimum period that may be programmed for $t_{LCLKTPROG}$.



NOTES
The t_{SLACH} and t_{HLACH} specifications apply only to the LP_ACK falling edge. If these specifications are met, LP_CLK would extend and the dotted LP_CLK falling edge would not occur as shown. The position of the dotted falling edge can be calculated using the $t_{LCLKTWH}$ specification. $t_{LCLKTWH}$ Min should be used for t_{SLACH} and $t_{LCLKTWH}$ Max for t_{HLACH}.

Figure 35. Link Ports—Transmit

Table 48. Serial Ports—Enable and Three-State

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Switching Characteristics						
t_{DDTEN}	Data Enable from External Transmit SPT_CLK[1]	1		1		ns
t_{DDTTE}	Data Disable from External Transmit SPT_CLK[1]		18.8		14	ns
t_{DDTIN}	Data Enable from Internal Transmit SPT_CLK[1]	–1		–1		ns
t_{DDTTI}	Data Disable from Internal Transmit SPT_CLK[1]		2.8		2.8	ns

[1] Referenced to drive edge.

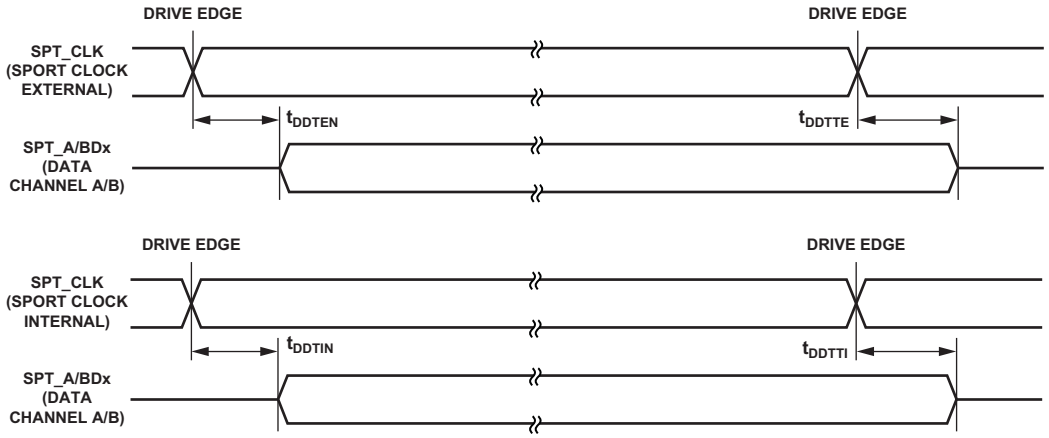


Figure 37. Serial Ports—Enable and Three-State

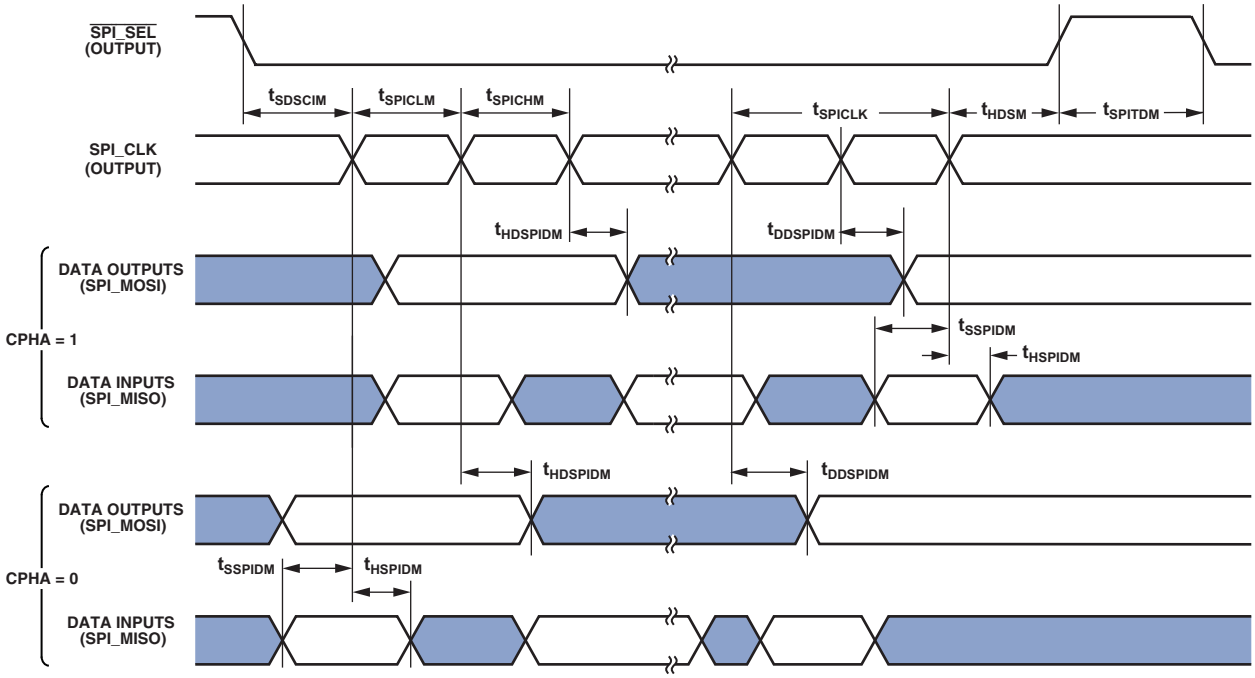


Figure 40. Serial Peripheral Interface (SPI) Port—Master Timing

Serial Peripheral Interface (SPI) Port—Slave Timing

Table 52 and Figure 41 describe SPI port slave operations. Note that:

- In dual mode data transmit the SPI_MOSI signal is also an output.
- In quad mode data transmit the SPI_MOSI, SPI_D2, and SPI_D3 signals are also outputs.
- In dual mode data receive the SPI_MISO signal is also an input.
- In quad mode data receive the SPI_MISO, SPI_D2, and SPI_D3 signals are also inputs.
- In SPI slave mode the SPI clock is supplied externally and is called $f_{SPICLKEXT}$:

$$t_{SPICLKEXT} = \frac{1}{f_{SPICLKEXT}}$$

Table 52. Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{SPICHS}	SPI_CLK High Period[1]	$(0.5 \times t_{SPICLKEXT}) - 1.5$		$(0.5 \times t_{SPICLKEXT}) - 1.5$		ns
t_{SPICLS}	SPI_CLK Low Period[1]	$(0.5 \times t_{SPICLKEXT}) - 1.5$		$(0.5 \times t_{SPICLKEXT}) - 1.5$		ns
t_{SPICLK}	SPI_CLK Period[1]	$t_{SPICLKEXT} - 1.5$		$t_{SPICLKEXT} - 1.5$		ns
t_{HDS}	Last SPI_CLK Edge to $\overline{\text{SPI\_SS}}$ Not Asserted	5		5		ns
t_{SPITDS}	Sequential Transfer Delay	$0.5 \times t_{SPICLK} - 1.5$		$0.5 \times t_{SPICLK} - 1.5$		ns
t_{SDSCI}	$\overline{\text{SPI\_SS}}$ Assertion to First SPI_CLK Edge	11.9		10.5		ns
t_{SSPID}	Data Input Valid to SPI_CLK Edge (Data Input Setup)	2.0		2.0		ns
t_{HSPID}	SPI_CLK Sampling Edge to Data Input Invalid	1.6		1.6		ns
Switching Characteristics						
t_{DSOE}	$\overline{\text{SPI\_SS}}$ Assertion to Data Out Active	0	18.8	0	14	ns
t_{DSDHI}	$\overline{\text{SPI\_SS}}$ Deassertion to Data High Impedance	0	16.3	0	12.5	ns
t_{DDSPID}	SPI_CLK Edge to Data Out Valid (Data Out Delay)		18.8		14	ns
t_{HDSPID}	SPI_CLK Edge to Data Out Invalid (Data Out Hold)	1.5		1.5		ns

[1] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPI_CLK. For the external SPI_CLK ideal maximum frequency see the $f_{SPICLKTEXT}$ specification in the Clock Related Operating Conditions table on Page 53.

10/100 Ethernet MAC Controller Timing

Table 64 through Table 66 and Figure 55 through Figure 57 describe the 10/100 Ethernet MAC Controller operations.

Table 64. 10/100 Ethernet MAC Controller Timing: RMII Receive Signal

Parameter[1]		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Timing Requirements				
$t_{REFCLKF}$	ETHx_REFCLK Frequency (f_{SCLK0} = SCLK0 Frequency)	None	50 + 1%	MHz
$t_{REFCLKW}$	ETHx_REFCLK Width (t_{REFCLK} = ETHx_REFCLK Period)	$t_{REFCLK} \times 35\%$	$t_{REFCLK} \times 65\%$	ns
$t_{REFCLKIS}$	Rx Input Valid to RMII ETHx_REFCLK Rising Edge (Data In Setup)	4		ns
$t_{REFCLKIH}$	RMII ETHx_REFCLK Rising Edge to Rx Input Invalid (Data In Hold)	2.2		ns

[1] RMII inputs synchronous to RMII REF_CLK are ERxD1–0, RMII CRS_DV, and ERxER.

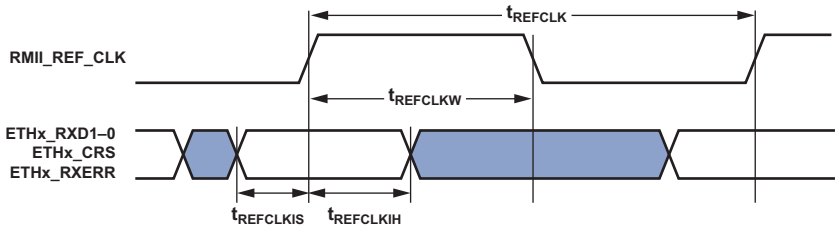


Figure 55. 10/100 Ethernet MAC Controller Timing: RMII Receive Signal

Table 65. 10/100 Ethernet MAC Controller Timing: RMII Transmit Signal

Parameter[1]		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Switching Characteristics				
$t_{REFCLKOV}$	RMII ETHx_REFCLK Rising Edge to Transmit Output Valid (Data Out Valid)		14	ns
$t_{REFCLKOH}$	RMII ETHx_REFCLK Rising Edge to Transmit Output Invalid (Data Out Hold)	2		ns

[1] RMII outputs synchronous to RMII REF_CLK are ETxD1–0.

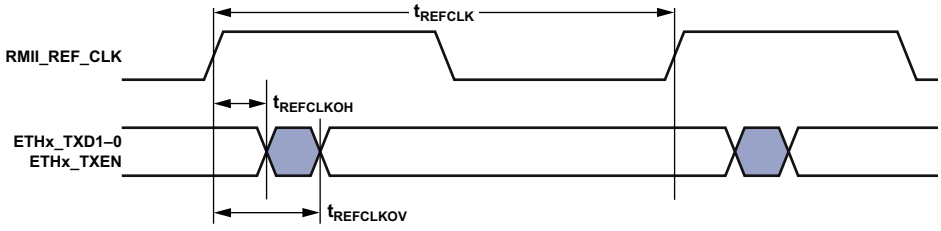


Figure 56. 10/100 Ethernet MAC Controller Timing: RMII Transmit Signal

JTAG Test And Emulation Port Timing

Table 67 and Figure 58 describe JTAG port operations.

Table 67. JTAG Port Timing

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{TCK}	JTG_TCK Period	20		20		ns
t_{STAP}	JTG_TDI, JTG_TMS Setup Before JTG_TCK High	4		4		ns
t_{HTAP}	JTG_TDI, JTG_TMS Hold After JTG_TCK High	4		4		ns
t_{SSYS}	System Inputs Setup Before JTG_TCK High[1]	12		12		ns
t_{HSYS}	System Inputs Hold After JTG_TCK High[1]	5		5		ns
t_{TRSTW}	$\overline{\text{JTG\_TRST}}$ Pulse Width (measured in JTG_TCK cycles)[2]	4		4		T_{CK}
Switching Characteristics						
t_{DTDO}	JTG_TDO Delay from JTG_TCK Low		18		13.5	ns
t_{DSYS}	System Outputs Delay After JTG_TCK Low[3]		22		17	ns

[1] System Inputs = DMC0_DQ00–15, DMC0_LDQS, $\overline{\text{DMC0\_LDQS}}$, DMC0_UDQS, $\overline{\text{DMC0\_UDQS}}$, PA_15–0, PB_15–0, PC_15–0, PD_15–0, PE_15–0, PF_15–0, PG_15–0, SMC0_ARDY_NORWT, $\overline{\text{SMC0\_BR}}$, SMC0_D15–0, SYS_BMODE0–2, $\overline{\text{SYS\_HWRST}}$, SYS_FAULT, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{SYS\_NMI\_RESOUT}}$, SYS_PWRGD, TWI0_SCL, TWI0_SDA, TWI1_SCL, TWI1_SDA.

[2] 50 MHz Maximum.

[3] System Outputs = DMC0_A00–13, DMC0_BA0–2, $\overline{\text{DMC0\_CAS}}$, DMC0_CK, $\overline{\text{DMC0\_CK}}$, DMC0_CKE, $\overline{\text{DMC0\_CS0}}$, DMC0_DQ00–15, DMC0_LDM, DMC0_LDQS, $\overline{\text{DMC0\_LDQS}}$, DMC0_ODT, $\overline{\text{DMC0\_RAS}}$, DMC0_UDM, DMC0_UDQS, $\overline{\text{DMC0\_UDQS}}$, $\overline{\text{DMC0\_WE}}$, $\overline{\text{JTG\_EMU}}$, PA_15–0, PB_15–0, PC_15–0, PD_15–0, PE_15–0, PF_15–0, PG_15–0, $\overline{\text{SMC0\_AMS0}}$, $\overline{\text{SMC0\_AOE\_NORDV}}$, $\overline{\text{SMC0\_ARE}}$, $\overline{\text{SMC0\_AWE}}$, SMC0_A01, SMC0_A02, SMC0_D15–0, SYS_CLKOUT, SYS_FAULT, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{SYS\_NMI\_RESOUT}}$.

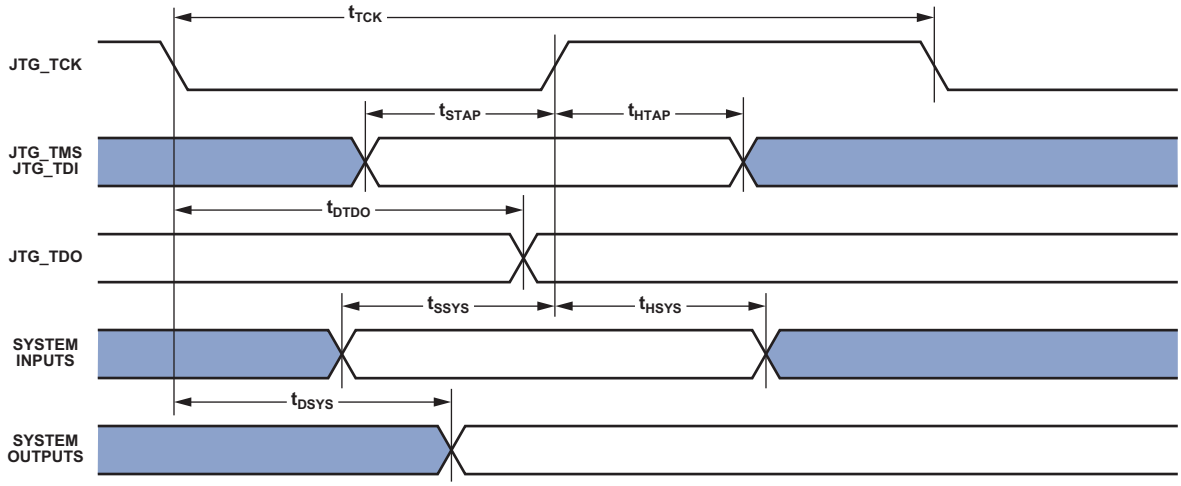


Figure 58. JTAG Port Timing

ADSP-BF60x 349-BALL CSP_BGA BALL ASSIGNMENTS

The 349-Ball CSP_BGA Ball Assignment (Numerical by Ball Number) table lists the CSP_BGA package by ball number for the ADSP-BF609.

The 349-Ball CSP_BGA Ball Assignment (Alphabetical by Pin Name) table lists the CSP_BGA package by signal.

349-BALL CSP_BGA BALL ASSIGNMENT (NUMERICAL BY BALL NUMBER)

Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name
A01	GND	B21	GND	F06	V_{DD_EXT}	H22	DMC0_DQ14
A02	USB0_DM	B22	$\overline{\text{SMC0_AOE}}$_NORDV	F07	V_{DD_INT}	J01	GND
A03	USB0_DP	C01	USB0_CLKIN	F08	V_{DD_INT}	J02	SYS_PWRGD
A04	PB_10	C02	USB0_VBC	F09	V_{DD_INT}	J03	SYS_BMODE0
A05	PB_07	C03	GND	F10	V_{DD_INT}	J06	V_{DD_EXT}
A06	PA_14	C04	PB_12	F11	V_{DD_EXT}	J09	GND
A07	PA_12	C05	PB_09	F12	V_{DD_EXT}	J10	GND
A08	PA_10	C06	PB_06	F13	V_{DD_INT}	J11	GND
A09	PA_08	C07	PB_05	F14	V_{DD_INT}	J12	GND
A10	PA_06	C08	PB_04	F15	V_{DD_INT}	J13	GND
A11	PA_04	C09	PB_03	F16	V_{DD_INT}	J14	GND
A12	PA_02	C10	PB_02	F17	V_{DD_DMC}	J17	V_{DD_DMC}
A13	PA_00	C11	PB_01	F20	$\overline{\text{DMC0\_CS0}}$	J20	DMC0_ODT
A14	SMC0_A01	C12	PB_00	F21	DMC0_DQ15	J21	DMC0_DQ12
A15	SMC0_D00	C13	$\overline{\text{SMC0\_BR}}$	F22	DMC0_DQ08	J22	DMC0_DQ11
A16	$\overline{\text{SMC0\_AMS0}}$	C14	SMC0_D06	G01	GND	K01	PC_00
A17	SMC0_D03	C15	SMC0_D12	G02	$\overline{\text{SYS\_HWRST}}$	K02	SYS_EXTWAKE
A18	SMC0_D04	C16	$\overline{\text{SMC0\_ARE}}$	G03	SYS_BMODE2	K03	PB_13
A19	SMC0_D07	C17	SMC0_D08	G06	V_{DD_EXT}	K06	V_{DD_EXT}
A20	SMC0_D10	C18	SMC0_D11	G07	V_{DD_EXT}	K08	GND
A21	$\overline{\text{SMC0\_AWE}}$	C19	SMC0_D14	G08	V_{DD_INT}	K09	GND
A22	GND	C20	GND	G09	V_{DD_INT}	K10	GND
B01	USB0_VBUS	C21	TWI1_SCL	G10	V_{DD_EXT}	K11	GND
B02	GND	C22	TWI0_SCL	G11	V_{DD_EXT}	K12	GND
B03	USB0_ID	D01	JTG_TDI	G12	V_{DD_EXT}	K13	GND
B04	PB_11	D02	JTG_TDO	G13	V_{DD_EXT}	K14	GND
B05	PB_08	D03	JTG_TCK	G14	V_{DD_INT}	K15	GND
B06	PA_15	D11	V_{DD_EXT}	G15	V_{DD_INT}	K17	V_{DD_DMC}
B07	PA_13	D12	GND	G16	V_{DD_DMC}	K20	DMC0_LDM
B08	PA_11	D20	SMC0_ARDY_NORWT	G17	V_{DD_DMC}	K21	$\overline{\text{DMC0\_LDQS}}$
B09	PA_09	D21	TWI1_SDA	G20	DMC0_UDM	K22	DMC0_LDQS
B10	PA_07	D22	TWI0_SDA	G21	DMC0_UDQS	L01	PC_02
B11	PA_05	E01	$\overline{\text{JTG\_TRST}}$	G22	$\overline{\text{DMC0\_UDQS}}$	L02	PC_01
B12	PA_03	E02	$\overline{\text{JTG\_EMU}}$	H01	SYS_CLKIN	L03	PB_14
B13	PA_01	E03	JTG_TMS	H02	SYS_XTAL	L04	V_{DD_EXT}
B14	SMC0_A02	E05	V_{DD_USB}	H03	SYS_BMODE1	L06	V_{DD_EXT}
B15	SMC0_D01	E20	$\overline{\text{DMC0\_CAS}}$	H06	V_{DD_EXT}	L08	GND
B16	SMC0_D15	E21	DMC0_DQ10	H07	V_{DD_EXT}	L09	GND
B17	SMC0_D09	E22	DMC0_DQ13	H16	V_{DD_DMC}	L10	GND
B18	SMC0_D02	F01	$\overline{\text{SYS\_FAULT}}$	H17	V_{DD_DMC}	L11	GND
B19	SMC0_D13	F02	SYS_FAULT	H20	$\overline{\text{DMC0\_RAS}}$	L12	GND
B20	SMC0_D05	F03	$\overline{\text{SYS\_NMI\_RESOUT}}$	H21	DMC0_DQ09	L13	GND