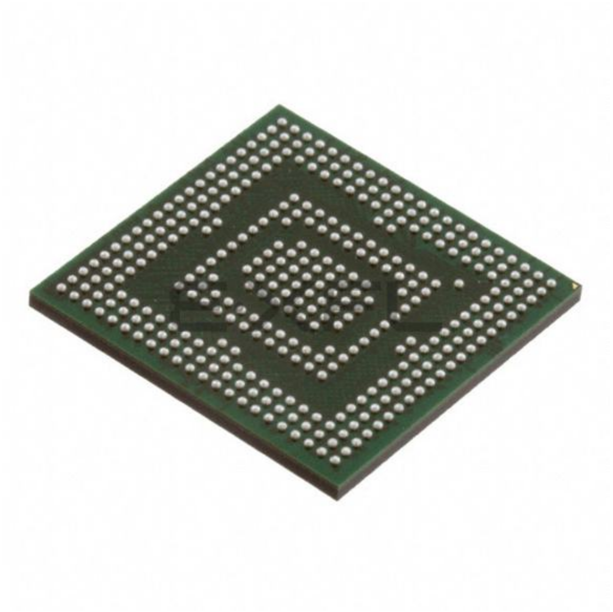
Analog Devices Inc. - ADSP-BF609KBCZ-5 Datasheet



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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Dual Core
Interface	CAN, EBI/EMI, Ethernet, I²C, SPI, SPORT, UART/USART, USB OTG
Clock Rate	500MHz
Non-Volatile Memory	ROM (64kB)
On-Chip RAM	808K x 8
Voltage - I/O	1.8V, 3.3V
Voltage - Core	1.25V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	349-LFBGA, CSPBGA
Supplier Device Package	349-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf609kbcz-5

Internal (Core-Accessible) Memory

The L1 memory system is the highest-performance memory available to the Blackfin processor cores.

Each core has its own private L1 memory. The modified Harvard architecture supports two concurrent 32-bit data accesses along with an instruction fetch at full processor speed which provides high bandwidth processor performance. In each core a 64K-byte block of data memory partners with an 80K-byte memory block for instruction storage. Each data block is multibanked for efficient data exchange through DMA and can be configured as SRAM. Alternatively, 16K bytes of each block can be configured in L1 cache mode. The four-way set-associative instruction cache and the 2 two-way set-associative data caches greatly accelerate memory access performance, especially when accessing external memories.

The L1 memory domain also features a 4K-byte scratchpad SRAM block which is ideal for storing local variables and the software stack. All L1 memory is protected by a multi-parity bit concept, regardless of whether the memory is operating in SRAM or cache mode.

Outside of the L1 domain, L2 and L3 memories are arranged using a Von Neumann topology. The L2 memory domain is a unified instruction and data memory and can hold any mixture of code and data required by the system design. The L2 memory domain is accessible by both Blackfin cores through a dedicated 64-bit interface. It operates at SYSCLK frequency.

The processor features up to 256K bytes of L2 SRAM which is ECC-protected and organized in eight banks. Individual banks can be made private to any of the cores or the DMA subsystem. There is also a 32K-byte single-bank ROM in the L2 domain. It contains boot code and safety functions.

Static Memory Controller (SMC)

The SMC can be programmed to control up to four banks of external memories or memory-mapped devices, with very flexible timing parameters. Each bank occupies a 64M byte segment regardless of the size of the device used, so that these banks are only contiguous if each is fully populated with 64M bytes of memory.

Dynamic Memory Controller (DMC)

The DMC includes a controller that supports JESD79-2E compatible double data rate (DDR2) SDRAM and JESD209A low power DDR (LPDDR) SDRAM devices.

I/O Memory Space

The processor does not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory-mapped registers (MMRs) at addresses near the top of the 4G byte address space. These are separated into two smaller blocks, one which contains the control MMRs for all core functions, and the other which contains the registers needed for setup and control of the on-chip peripherals outside of the core. The MMRs are accessible only in supervisor mode and appear as reserved space to on-chip peripherals.

Booting

The processor has several mechanisms for automatically loading internal and external memory after a reset. The boot mode is defined by the SYS_BMODE input pins dedicated for this purpose. There are two categories of boot modes. In master boot modes, the processor actively loads data from parallel or serial memories. In slave boot modes, the processor receives data from external host devices.

The boot modes are shown in Table 2. These modes are implemented by the SYS_BMODE bits of the reset configuration register and are sampled during power-on resets and software-initiated resets.

Table 2. Boot Modes

SYS_BMODE Setting	Boot Mode
000	No boot/Idle
001	Memory
010	RSI0 Master
011	SPI0 Master
100	SPI0 Slave
101	Reserved
110	LP0 Slave
111	UART0 Slave

VIDEO SUBSYSTEM

The following sections describe the components of the processor's video subsystem. These blocks are shown with blue shading in Figure 1 on Page 1.

Video Interconnect (VID)

The Video Interconnect provides a connectivity matrix that interconnects the Video Subsystem: three PPIs, the PIXC, and the PVP. The interconnect uses a protocol to manage data transfer among these video peripherals.

Pipelined Vision Processor (PVP)

The PVP engine provides hardware implementation of signal and image processing algorithms that are required for co-processing and pre-processing of monochrome video frames in ADAS applications, robotic systems, and other machine applications.

The PVP works in conjunction with the Blackfin cores. It is optimized for convolution and wavelet based object detection and classification, and tracking and verification algorithms. The PVP has the following processing blocks.

- Four 5 × 5 16-bit convolution blocks optionally followed by down scaling
- A 16-bit cartesian-to-polar coordinate conversion block
- A pixel edge classifier that supports 1st and 2nd derivative modes
- An arithmetic unit with 32-bit addition, multiply and divide

A third counter input can provide flexible zero marker support and can alternatively be used to input the push-button signal of thumb wheels. All three pins have a programmable debouncing circuit.

Internal signals forwarded to each general-purpose timer enable these timers to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmable count values are exceeded.

Serial Peripheral Interface (SPI) Ports

The processors have two SPI-compatible ports that allow the processor to communicate with multiple SPI-compatible devices.

In its simplest mode, the SPI interface uses three pins for transferring data: two data pins (Master Output-Slave Input, MOSI, and Master Input-Slave Output, MISO) and a clock pin (serial clock, SPI_CLK). A SPI chip select input pin ($\overline{\text{SPI\_SS}}$) lets other SPI devices select the processor, and seven SPI chip select output pins ($\overline{\text{SPI\_SEL7–1}}$) let the processor select other SPI devices. The SPI select pins are reconfigured general-purpose I/O pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

In a multi-master or multi-slave SPI system, the MOSI and MISO data output pins can be configured to behave as open drain outputs (using the ODM bit) to prevent contention and possible damage to pin drivers. An external pull-up resistor is required on both the MOSI and MISO pins when this option is selected.

When ODM is set and the SPI is configured as a master, the MOSI pin is three-stated when the data driven out on MOSI is a logic-high. The MOSI pin is not three-stated when the driven data is a logic-low. Similarly, when ODM is set and the SPI is configured as a slave, the MISO pin is three-stated if the data driven out on MISO is a logic-high.

The SPI port's baud rate and clock phase/polarities are programmable, and it has integrated DMA channels for both transmit and receive data streams.

UART Ports

The processors provide two full-duplex universal asynchronous receiver/transmitter (UART) ports, which are fully compatible with PC-standard UARTs. Each UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits, and none, even, or odd parity. Optionally, an additional address bit can be transferred to interrupt only addressed nodes in multi-drop bus (MDB) systems. A frame is terminates by one, one and a half, two or two and a half stop bits.

The UART ports support automatic hardware flow control through the Clear To Send (CTS) input and Request To Send (RTS) output with programmable assertion FIFO levels.

To help support the Local Interconnect Network (LIN) protocols, a special command causes the transmitter to queue a break command of programmable bit length into the transmit buffer. Similarly, the number of stop bits can be extended by a programmable inter-frame space.

The capabilities of the UARTs are further extended with support for the Infrared Data Association (IrDA®) serial infrared physical layer link specification (SIR) protocol.

TWI Controller Interface

The processors include a 2-wire interface (TWI) module for providing a simple exchange method of control data between multiple devices. The TWI module is compatible with the widely used I^{2}C bus standard. The TWI module offers the capabilities of simultaneous master and slave operation and support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two pins for transferring clock (TWI_SCL) and data (TWI_SDA) and supports the protocol at speeds up to 400k bits/sec. The TWI interface pins are compatible with 5 V logic levels.

Additionally, the TWI module is fully compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

Removable Storage Interface (RSI)

The removable storage interface (RSI) controller acts as the host interface for multimedia cards (MMC), secure digital memory cards (SD), secure digital input/output cards (SDIO). The following list describes the main features of the RSI controller.

- Support for a single MMC, SD memory, SDIO card
- Support for 1-bit and 4-bit SD modes
- Support for 1-bit, 4-bit, and 8-bit MMC modes
- Support for eMMC 4.3 embedded NAND flash devices
- A ten-signal external interface with clock, command, and up to eight data lines
- Card interface clock generation from SCLK0
- SDIO interrupt and read wait features

Controller Area Network (CAN)

A CAN controller implements the CAN 2.0B (active) protocol. This protocol is an asynchronous communications protocol used in both industrial and automotive control systems. The CAN protocol is well suited for control applications due to its capability to communicate reliably over a network. This is because the protocol incorporates CRC checking, message error tracking, and fault node confinement.

The CAN controller offers the following features:

- 32 mailboxes (8 receive only, 8 transmit only, 16 configurable for receive or transmit).
- Dedicated acceptance masks for each mailbox.
- Additional data filtering on first two bytes.
- Support for both the standard (11-bit) and extended (29-bit) identifier (ID) message formats.

Table 7. ADSP-BF60x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
PPI1_D08	EPPI1 Data 8	C	PC_08
PPI1_D09	EPPI1 Data 9	C	PC_09
PPI1_D10	EPPI1 Data 10	C	PC_10
PPI1_D11	EPPI1 Data 11	C	PC_11
PPI1_D12	EPPI1 Data 12	C	PC_12
PPI1_D13	EPPI1 Data 13	C	PC_13
PPI1_D14	EPPI1 Data 14	C	PC_14
PPI1_D15	EPPI1 Data 15	C	PC_15
PPI1_D16	EPPI1 Data 16	D	PD_00
PPI1_D17	EPPI1 Data 17	D	PD_01
PPI1_FS1	EPPI1 Frame Sync 1 (HSYNC)	B	PB_13
PPI1_FS2	EPPI1 Frame Sync 2 (VSYNC)	D	PD_06
PPI1_FS3	EPPI1 Frame Sync 3 (FIELD)	B	PB_15
PPI2_CLK	EPPI2 Clock	B	PB_00
PPI2_D00	EPPI2 Data 0	A	PA_00
PPI2_D01	EPPI2 Data 1	A	PA_01
PPI2_D02	EPPI2 Data 2	A	PA_02
PPI2_D03	EPPI2 Data 3	A	PA_03
PPI2_D04	EPPI2 Data 4	A	PA_04
PPI2_D05	EPPI2 Data 5	A	PA_05
PPI2_D06	EPPI2 Data 6	A	PA_06
PPI2_D07	EPPI2 Data 7	A	PA_07
PPI2_D08	EPPI2 Data 8	A	PA_08
PPI2_D09	EPPI2 Data 9	A	PA_09
PPI2_D10	EPPI2 Data 10	A	PA_10
PPI2_D11	EPPI2 Data 11	A	PA_11
PPI2_D12	EPPI2 Data 12	A	PA_12
PPI2_D13	EPPI2 Data 13	A	PA_13
PPI2_D14	EPPI2 Data 14	A	PA_14
PPI2_D15	EPPI2 Data 15	A	PA_15
PPI2_D16	EPPI2 Data 16	B	PB_07
PPI2_D17	EPPI2 Data 17	B	PB_08
PPI2_FS1	EPPI2 Frame Sync 1 (HSYNC)	B	PB_01
PPI2_FS2	EPPI2 Frame Sync 2 (VSYNC)	B	PB_02
PPI2_FS3	EPPI2 Frame Sync 3 (FIELD)	B	PB_03
PWM0_AH	PWM0 Channel A High Side	F	PF_01
PWM0_AL	PWM0 Channel A Low Side	F	PF_00
PWM0_BH	PWM0 Channel B High Side	F	PF_03
PWM0_BL	PWM0 Channel B Low Side	F	PF_02
PWM0_CH	PWM0 Channel C High Side	F	PF_05
PWM0_CL	PWM0 Channel C Low Side	F	PF_04
PWM0_DH	PWM0 Channel D High Side	F	PF_07
PWM0_DL	PWM0 Channel D Low Side	F	PF_06
PWM0_SYNC	PWM0 Sync	E	PE_08
$\overline{\text{PWM0\_TRIP0}}$	PWM0 Shutdown Input 0	E	PE_09
$\overline{\text{PWM0\_TRIP1}}$	PWM0 Shutdown Input 1	F	PF_11

Table 7. ADSP-BF60x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SMC0_ABE0	SMC0 Byte Enable 0	B	PB_04
SMC0_ABE1	SMC0 Byte Enable 1	B	PB_05
SMC0_AMS0	SMC0 Memory Select 0	Not Muxed	SMC0_AMS0
SMC0_AMS1	SMC0 Memory Select 1	B	PB_01
SMC0_AMS2	SMC0 Memory Select 2	B	PB_04
SMC0_AMS3	SMC0 Memory Select 3	B	PB_05
SMC0_AOE	SMC0 Output Enable	Not Muxed	SMC0_AOE_NORDV
SMC0_ARDY	SMC0 Asynchronous Ready	Not Muxed	SMC0_ARDY_NORWT
SMC0_ARE	SMC0 Read Enable	Not Muxed	SMC0_ARE
SMC0_AWE	SMC0 Write Enable	Not Muxed	SMC0_AWE
SMC0_BGH	SMC0 Bus Grant Hang	B	PB_09
SMC0_BG	SMC0 Bus Grant	B	PB_12
SMC0_BR	SMC0 Bus Request	Not Muxed	SMC0_BR
SMC0_D00	SMC0 Data 0	Not Muxed	SMC0_D00
SMC0_D01	SMC0 Data 1	Not Muxed	SMC0_D01
SMC0_D02	SMC0 Data 2	Not Muxed	SMC0_D02
SMC0_D03	SMC0 Data 3	Not Muxed	SMC0_D03
SMC0_D04	SMC0 Data 4	Not Muxed	SMC0_D04
SMC0_D05	SMC0 Data 5	Not Muxed	SMC0_D05
SMC0_D06	SMC0 Data 6	Not Muxed	SMC0_D06
SMC0_D07	SMC0 Data 7	Not Muxed	SMC0_D07
SMC0_D08	SMC0 Data 8	Not Muxed	SMC0_D08
SMC0_D09	SMC0 Data 9	Not Muxed	SMC0_D09
SMC0_D10	SMC0 Data 10	Not Muxed	SMC0_D10
SMC0_D11	SMC0 Data 11	Not Muxed	SMC0_D11
SMC0_D12	SMC0 Data 12	Not Muxed	SMC0_D12
SMC0_D13	SMC0 Data 13	Not Muxed	SMC0_D13
SMC0_D14	SMC0 Data 14	Not Muxed	SMC0_D14
SMC0_D15	SMC0 Data 15	Not Muxed	SMC0_D15
SMC0_NORCLK	SMC0 NOR Clock	B	PB_00
SMC0_NORDV	SMC0 NOR Data Valid	Not Muxed	SMC0_AOE_NORDV
SMC0_NORWT	SMC0 NOR Wait	Not Muxed	SMC0_ARDY_NORWT
SPI0_CLK	SPI0 Clock	D	PD_04
SPI0_D2	SPI0 Data 2	D	PD_00
SPI0_D3	SPI0 Data 3	D	PD_01
SPI0_MISO	SPI0 Master In, Slave Out	D	PD_02
SPI0_MOSI	SPI0 Master Out, Slave In	D	PD_03
SPI0_RDY	SPI0 Ready	D	PD_10
SPI0_SEL1	SPI0 Slave Select Output 1	D	PD_11
SPI0_SEL2	SPI0 Slave Select Output 2	D	PD_01
SPI0_SEL3	SPI0 Slave Select Output 3	D	PD_00
SPI0_SEL4	SPI0 Slave Select Output 4	C	PC_15
SPI0_SEL5	SPI0 Slave Select Output 5	D	PD_09
SPI0_SEL6	SPI0 Slave Select Output 6	C	PC_13
SPI0_SEL7	SPI0 Slave Select Output 7	C	PC_12
SPI0_SS	SPI0 Slave Select Input	D	PD_11

Table 7. ADSP-BF60x 349-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
UART0_RX	UART0 Receive	D	PD_08
UART0_TX	UART0 Transmit	D	PD_07
UART1_CTS	UART1 Clear to Send	G	PG_13
UART1_RTS	UART1 Request to Send	G	PG_10
UART1_RX	UART1 Receive	G	PG_14
UART1_TX	UART1 Transmit	G	PG_15
USB0_CLKIN	USB0 Clock/Crystal Input	Not Muxed	USB0_CLKIN
USB0_DM	USB0 Data –	Not Muxed	USB0_DM
USB0_DP	USB0 Data +	Not Muxed	USB0_DP
USB0_ID	USB0 OTG ID	Not Muxed	USB0_ID
USB0_VBC	USB0 VBUS Control	Not Muxed	USB0_VBC
USB0_VBUS	USB0 Bus Voltage	Not Muxed	USB0_VBUS
VDD_DMC	VDD for DMC	Not Muxed	VDD_DMC
VDD_EXT	External VDD	Not Muxed	VDD_EXT
VDD_INT	Internal VDD	Not Muxed	VDD_INT
VDD_TD	VDD for Thermal Diode	Not Muxed	VDD_TD
VDD_USB	VDD for USB	Not Muxed	VDD_USB
VREF_DMC	VREF for DMC	Not Muxed	VREF_DMC

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PB_00	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 0 | SMC0 NOR Clock | EPPI2 Clock | LP0 Clock. Notes: No notes.
PB_01	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 1 | SMC0 Memory Select 1 | EPPI2 Frame Sync 1 (HSYNC) | LP0 Acknowledge. Notes: No notes.
PB_02	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 2 | SMC0 Address 13 | EPPI2 Frame Sync 2 (VSYNC) | LP1 Acknowledge. Notes: No notes.
PB_03	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 3 | SMC0 Address 16 | EPPI2 Frame Sync 3 (FIELD) | LP1 Clock. Notes: No notes.
PB_04	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 4 | SMC0 Memory Select 2 | SMC0 Byte Enable 0 | SPORT0 Channel A Frame Sync. Notes: No notes.
PB_05	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 5 | SMC0 Memory Select 3 | SMC0 Byte Enable 1 | SPORT0 Channel A Clock. Notes: No notes.
PB_06	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 6 | SMC0 Address 21 | SPORT0 Channel A Transmit Data Valid | TIMER0 Alternate Clock 4. Notes: No notes.
PB_07	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 7 | SMC0 Address 22 | EPPI2 Data 16 | SPORT0 Channel B Frame Sync. Notes: No notes.
PB_08	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 8 | SMC0 Address 23 | EPPI2 Data 17 | SPORT0 Channel B Clock. Notes: No notes.
PB_09	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 9 | SMC0 Bus Grant Hang | SPORT0 Channel A Data 0 | TIMER0 Alternate Clock 2. Notes: No notes.
PB_10	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 10 | SMC0 Address 24 | SPORT0 Channel B Data 1 | TIMER0 Alternate Clock 0. Notes: No notes.
PB_11	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 11 | SMC0 Address 25 | SPORT0 Channel B Data 0 | TIMER0 Alternate Clock 3. Notes: No notes.
PB_12	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PB Position 12 | SMC0 Bus Grant | SPORT0 Channel B Transmit Data Valid | SPORT0 Channel A Data 1 | TIMER0 Alternate Clock 1. Notes: No notes.

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PC_13	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PC Position 13 | SPI0 Slave Select Output b | EPPI1 Data 13 | ETH PTP Clock Input. Notes: No notes.
PC_14	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PC Position 14 | SPI1 Slave Select Output b | EPPI1 Data 14. Notes: No notes.
PC_15	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PC Position 15 | SPI0 Slave Select Output b | EPPI1 Data 15. Notes: May be used to wake the processor from hibernate or deep sleep mode.
PD_00	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 0 | SPI0 Data 2 | EPPI1 Data 16 | SPI0 Slave Select Output b. Notes: No notes.
PD_01	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 1 | SPI0 Data 3 | EPPI1 Data 17 | SPI0 Slave Select Output b. Notes: No notes.
PD_02	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 2 | SPI0 Master In, Slave Out. Notes: No notes.
PD_03	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 3 | SPI0 Master Out, Slave In. Notes: No notes.
PD_04	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 4 | SPI0 Clock. Notes: No notes.
PD_05	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 5 | SPI1 Clock | TIMER0 Alternate Clock 7. Notes: No notes.
PD_06	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 6 | EPPI1 Frame Sync 2 (VSYNC) | ETH0 RMII Management Data Interrupt | TIMER0 Alternate Capture Input 5. Notes: May be used to wake the processor from hibernate or deep sleep mode.
PD_07	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 7 | UART0 Transmit | TIMER0 Alternate Capture Input 3. Notes: No notes.
PD_08	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 8 | UART0 Receive | TIMER0 Alternate Capture Input 0. Notes: No notes.
PD_09	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 9 | SPI1 Slave Select Output b | UART0 Request to Send | SPI0 Slave Select Output b. Notes: No notes.
PD_10	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 10 | SPI0 Ready | UART0 Clear to Send | SPI1 Slave Select Output b. Notes: No notes.
PD_11	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PD Position 11 | SPI0 Slave Select Output b | SPI0 Slave Select Input. Notes: No notes.

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PE_10	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 10 | PWM1 Channel D Low Side | RSI0 Data 6 | ETH1 Management Channel Clock. Notes: Has an optional internal pull-up resistor for use with RSI. See the RSI chapter in the processor hardware reference for more details.
PE_11	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 11 | PWM1 Channel D High Side | ETH1 Management Channel Serial Data | RSI0 Data 7. Notes: Has an optional internal pull-up resistor for use with RSI. See the RSI chapter in the processor hardware reference for more details.
PE_12	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 12 | PWM1 Channel C Low Side | RSI0 Data 5 | ETH1 RMII Management Data Interrupt. Notes: Has an optional internal pull-up resistor for use with RSI. See the RSI chapter in the processor hardware reference for more details. May be used to wake the processor from hibernate or deep sleep mode.
PE_13	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 13 | PWM1 Channel C High Side | RSI0 Data 4 | ETH1 Carrier Sense/RMII Receive Data Valid. Notes: Has an optional internal pull-up resistor for use with RSI. See the RSI chapter in the processor hardware reference for more details.
PE_14	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 14 | SPORT2 Channel A Transmit Data Valid | TIMER0 Timer 0 | ETH1 Receive Error. Notes: No notes.
PE_15	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PE Position 15 | PWM1 Channel B Low Side | RSI0 Data 3 | ETH1 Receive Data 1. Notes: Has an optional internal pull-up resistor for use with RSI. See the RSI chapter in the processor hardware reference for more details.
PF_00	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 0 | PWM0 Channel A Low Side | EPPI0 Data 0 | LP2 Data 0. Notes: No notes.
PF_01	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 1 | PWM0 Channel A High Side | EPPI0 Data 1 | LP2 Data 1. Notes: No notes.
PF_02	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: PF Position 2 | PWM0 Channel B Low Side | EPPI0 Data 2 | LP2 Data 2. Notes: No notes.

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
SMC0_D06	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Data 6. Notes: No notes.
SMC0_D07	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Data 7. Notes: No notes.
SMC0_D08	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Data 8. Notes: No notes.
SMC0_D09	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Data 9. Notes: No notes.
SMC0_D10	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Data 10. Notes: No notes.
SMC0_D11	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Data 11. Notes: No notes.
SMC0_D12	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Data 12. Notes: No notes.
SMC0_D13	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Data 13. Notes: No notes.
SMC0_D14	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Data 14. Notes: No notes.
SMC0_D15	I/O	A	wk	wk	none	wk	none	VDD_EXT	Desc: SMC0 Data 15. Notes: No notes.
SYS_BMODE0	I/O	na	none	none	none	none	none	VDD_EXT	Desc: SYS Boot Mode Control 0. Notes: No notes.
SYS_BMODE1	I/O	na	none	none	none	none	none	VDD_EXT	Desc: SYS Boot Mode Control 1. Notes: No notes.
SYS_BMODE2	I/O	na	none	none	none	none	none	VDD_EXT	Desc: SYS Boot Mode Control 2. Notes: No notes.
SYS_CLKIN	a	na	none	none	none	none	none	VDD_EXT	Desc: SYS Clock Input/Crystal Input. Notes: Active during reset.
SYS_CLKOUT	I/O	A	none	none	L	none	none	VDD_EXT	Desc: SYS Processor Clock Output. Notes: No notes.
SYS_EXTWAKE	I/O	A	none	none	H	none	L	VDD_EXT	Desc: SYS External Wake Control. Notes: Drives low during hibernate and high all other times.
SYS_FAULT	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SYS Fault. Notes: Open source, requires an external pull-down resistor.
$\overline{\text{SYS\_FAULT}}$	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SYS Complementary Fault. Notes: Open drain, requires an external pull-up resistor.
$\overline{\text{SYS\_HWRST}}$	I/O	na	none	none	none	none	none	VDD_EXT	Desc: SYS Processor Hardware Reset Control. Notes: Active during reset.
$\overline{\text{SYS\_NMI\_}}$ RESOUT	I/O	A	none	none	L	none	none	VDD_EXT	Desc: SYS Reset Output | SYS Non-maskable Interrupt. Notes: Requires an external pull-up resistor.

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
SYS_PWRGD	I/O	na	none	none	none	none	none	VDD_EXT	Desc: SYS Power Good Indicator. Notes: If hibernate is not used or the internal Power Good Counter is used, connect to VDD_EXT.
SYS_TDA	a	na	none	none	none	none	none	VDD_TD	Desc: SYS Thermal Diode Anode. Notes: Active during reset and hibernate. If the thermal diode is not used, connect to ground.
SYS_TDK	a	na	none	none	none	none	none	VDD_TD	Desc: SYS Thermal Diode Cathode. Notes: Active during reset and hibernate. If the thermal diode is not used, connect to ground.
SYS_XTAL	a	na	none	none	none	none	none	VDD_EXT	Desc: SYS Crystal Output. Notes: Leave unconnected if an oscillator is used to provide SYS_CLKIN. Active during reset. State during hibernate is controlled by DPM_HIB_DIS.
TWI0_SCL	I/O	D	none	none	none	none	none	VDD_EXT	Desc: TWI0 Serial Clock. Notes: Open drain, requires external pull-up resistor. Consult Version 2.1 of the I2C specification for the proper resistor value. If TWI is not used, connect to ground.
TWI0_SDA	I/O	D	none	none	none	none	none	VDD_EXT	Desc: TWI0 Serial Data. Notes: Open drain, requires external pull-up resistor. Consult Version 2.1 of the I2C specification for the proper resistor value. If TWI is not used, connect to ground.
TWI1_SCL	I/O	D	none	none	none	none	none	VDD_EXT	Desc: TWI1 Serial Clock. Notes: Open drain, requires external pull-up resistor. Consult Version 2.1 of the I2C specification for the proper resistor value. If TWI is not used, connect to ground.
TWI1_SDA	I/O	D	none	none	none	none	none	VDD_EXT	Desc: TWI1 Serial Data. Notes: Open drain, requires external pull-up resistor. See the I2C-Bus Specification, Version 2.1,January 2000 for the proper resistor value. If TWI is not used, connect to ground.
USB0_CLKIN	a	na	none	none	none	none	none	VDD_USB	Desc: USB0 Clock/Crystal Input. Notes: If USB is not used, connect to ground. Active during reset.
USB0_DM	I/O	F	none	none	none	none	none	VDD_USB	Desc: USB0 Data –. Notes: Pull low if not using USB. For complete documentation of hibernate behavior when USB is used, see the USB chapter in the processor hardware reference.

Table 15. ADSP-BF60x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
USB0_DP	I/O	F	none	none	none	none	none	VDD_USB	Desc: USB0 Data +. Notes: Pull low if not using USB. For complete documentation of hibernate behavior when USB is used, see the USB chapter in the processor hardware reference.
USB0_ID	I/O	na	none	none	none	pu	none	VDD_USB	Desc: USB0 OTG ID. Notes: If USB is not used, connect to ground. When USB is being used, the internal pull-up resistor that is present during hibernate is programmable. See the USB chapter in the processor hardware reference. Active during reset.
USB0_VBC	I/O	E	none	none	none	wk	none	VDD_USB	Desc: USB0 VBUS Control. Notes: If USB is not used, pull low.
USB0_VBUS	I/O	G	none	none	none	none	none	VDD_USB	Desc: USB0 Bus Voltage. Notes: If USB is not used, connect to ground.
VDD_DMC	s	na	none	none	none	none	none	na	Desc: VDD for DMC. Notes: If the DMC is not used, connect to VDD_INT.
VDD_EXT	s	na	none	none	none	none	none	na	Desc: External VDD. Notes: Must be powered.
VDD_INT	s	na	none	none	none	none	none	na	Desc: Internal VDD. Notes: Must be powered.
VDD_TD	s	na	none	none	none	none	none	na	Desc: VDD for Thermal Diode. Notes: If the thermal diode is not used, connect to ground.
VDD_USB	s	na	none	none	none	none	none	na	Desc: VDD for USB. Notes: If USB is not used, connect to VDD_EXT.
VREF_DMC	s	na	none	none	none	none	none	na	Desc: VREF for DMC. Notes: If the DMC is not used, connect to VDD_INT.

SPECIFICATIONS

For information about product specifications please contact your ADI representative.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DD_INT}	Internal Supply Voltage	CCLK 500 MHz	1.19	1.25	1.32	V
V_{DD_EXT}[1]	External Supply Voltage	1.8 V I/O	1.7	1.8	1.9	V
V_{DD_EXT}[1]	External Supply Voltage	3.3 V I/O	3.13	3.3	3.47	V
V_{DD_DMC}	DDR2/LPDDR Supply Voltage		1.7	1.8	1.9	V
V_{DD_USB}[2]	USB Supply Voltage		3.13	3.3	3.47	V
V_{DD_TD}	Thermal Diode Supply Voltage		3.13	3.3	3.47	V
V_{IH}[3]	High Level Input Voltage	V_{DD_EXT} = 3.47 V	2.1			V
V_{IH}[3]	High Level Input Voltage	V_{DD_EXT} = 1.9 V	0.7 × V_{DD_EXT}			V
V_{IHTWI}[4, 5]	High Level Input Voltage	V_{DD_EXT} = Maximum	0.7 × $V_{VBUSTWI}$		$V_{VBUSTWI}$	V
V_{IH_DDR2}[6, 7]		V_{DD_DMC} = 1.9 V	V_{DDR_REF} + 0.25			V
V_{IH_LPDDR}[8]		V_{DD_DMC} = 1.9 V	0.8 × V_{DD_DMC}			V
V_{ID_DDR2}[9]	Differential Input Voltage	V_{IX} = 1.075 V	0.50			V
V_{ID_DDR2}[9]	Differential Input Voltage	V_{IX} = 0.725 V	0.55			V
V_{IL}[3]	Low Level Input Voltage	V_{DD_EXT} = 3.13 V			0.8	V
V_{IL}[3]	Low Level Input Voltage	V_{DD_EXT} = 1.7 V			0.3 × V_{DD_EXT}	V
V_{ILTWI}[4, 5]	Low Level Input Voltage	V_{DD_EXT} = Minimum			0.3 × $V_{VBUSTWI}$	V
V_{IL_DDR2}[6, 7]		V_{DD_DMC} = 1.7 V			V_{DDR_REF} 0.25	V
V_{IL_LPDDR}[8]		V_{DD_DMC} = 1.7 V			0.2 × V_{DD_DMC}	V
T_J	Junction Temperature	$T_{AMBIENT}$ = 0℃ to +70℃	0		+105	℃
T_J	Junction Temperature	$T_{AMBIENT}$ = 40℃ to +85℃	40		+105	℃
T_J	Junction Temperature	$T_{AMBIENT}$ = 40℃ to +105℃	40		+125	℃

[1] Must remain powered (even if the associated function is not used).

[2] If not used, connect to 1.8 V or 3.3 V.

[3] Parameter value applies to all input and bidirectional signals except TWI signals, DMC0 signals and USB0 signals.

[4] Parameter applies to TWI signals.

[5] TWI signals are pulled up to V_{BUSTWI}. See Table 16

[6] Parameter applies to DMC0 signals in DDR2 mode.

[7] V_{DDR_REF} is the voltage applied to pin V_{REF_DMG} nominally $V_{DD\_DMC}/2$.

[8] Parameter applies to DMC0 signals in LPDDR mode.

[9] Parameter applies to signals DMC0_CK, $\overline{\text{DMC0\_CK}}$, DMC0_LDQS, $\overline{\text{DMC0\_LDQS}}$, DMC0_UDQS, $\overline{\text{DMC0\_UDQS}}$ when used in DDR2 differential input mode.

Table 16. TWI_VSEL Selections and V_{DD_EXT}/V_{BUSTWI}

	V_{DD_EXT} Nominal	V_{BUSTWI} Min	V_{BUSTWI} Nom	V_{BUSTWI} Max	Unit
TWI000[1]	3.30	3.13	3.30	3.47	V
TWI001	1.80	1.70	1.80	1.90	V
TWI011	1.80	3.13	3.30	3.47	V
TWI100	3.30	4.75	5.00	5.25	V

[1] Designs must comply with the V_{DD_EXT} and V_{BUSTWI} voltages specified for the default TWI_DT setting for correct JTAG boundary scan operation during reset.

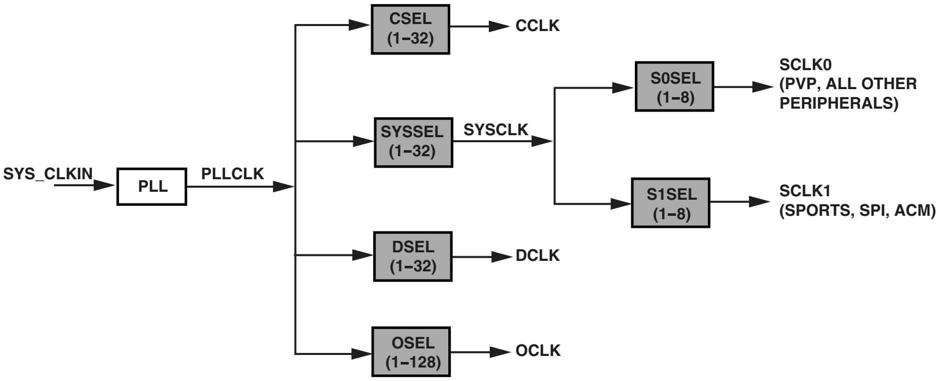

SYS_CLKIN
PLL
PLLCLK
CSEL
(1–32)
CCLK
SYSSEL
(1–32)
SYSCLK
S0SEL
(1–8)
SCLK0
(PVP, ALL OTHER PERIPHERALS)
S1SEL
(1–8)
SCLK1
(SPORTS, SPI, ACM)
DSEL
(1–32)
DCLK
OSEL
(1–128)
OCLK

Figure 8. Clock Relationships and Divider Values

Total Internal Power Dissipation

Total power dissipation has two components:

1. Static, including leakage current (deep sleep)
2. Dynamic, due to transistor switching characteristics for each clock domain

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. The following equation describes the internal current consumption.

$$I_{DDINT\_TOT} = I_{DDINT\_CCLK\_DYN} + I_{DDINT\_SYSCLK\_DYN} + I_{DDINT\_SCLK0\_DYN} + I_{DDINT\_SCLK1\_DYN} + I_{DDINT\_DCLK\_DYN} + I_{DDINT\_USBCLK\_DYN} + I_{DDINT\_DMA\_DR\_DYN} + I_{DDINT\_DEEPSLEEP} + I_{DDINT\_PVP\_DYN}$$

$I_{DDINT\_DEEPSLEEP}$ is the only item present that is part of the static power dissipation component. $I_{DDINT\_DEEPSLEEP}$ is specified as a function of voltage (V_{DD_INT}) and temperature (see Table 21).

There are eight different items that contribute to the dynamic power dissipation. These components fall into three broad categories: application-dependent currents, clock currents and data transmission currents.

Application-Dependent Current

The application-dependent currents include the dynamic current in the core clock domain and the dynamic current of the PVP.

Core clock (CCLK) use is subject to an activity scaling factor (ASF) that represents application code running on the processor cores and L1/L2 memories (Table 20). The ASF is combined with the CCLK frequency and V_{DD_INT} dependent data in Table 19 to calculate this portion.

$I_{DDINT\_CCLK\_DYN}$ (mA) = Table 19 × (ASFC0 + ASFC1)

The dynamic current of the PVP is determined by selecting the appropriate use case from Table 22.

$I_{DDINT\_PVP\_DYN}$ (mA) = Table 22

Clock Current

The dynamic clock currents provide the total power dissipated by all transistors switching in the clock paths. The power dissipated by each clock domain is dependent on voltage (V_{DD_INT}), operating frequency and a unique scaling factor.

$I_{DDINT\_SYSCLK\_DYN}(\text{mA}) = 0.187 \times f_{SYSCLK}(\text{MHz}) \times V_{DD\_INT}(\text{V})$

$I_{DDINT\_SCLK0\_DYN}(\text{mA}) = 0.217 \times f_{SCLK0}(\text{MHz}) \times V_{DD\_INT}(\text{V})$

$I_{DDINT\_SCLK1\_DYN}(\text{mA}) = 0.042 \times f_{SCLK1}(\text{MHz}) \times V_{DD\_INT}(\text{V})$

$I_{DDINT\_DCLK\_DYN}(\text{mA}) = 0.024 \times f_{DCLK}(\text{MHz}) \times V_{DD\_INT}(\text{V})$

The dynamic component of the USB clock is a unique case. The USB clock contributes a near constant current value when used.

$I_{DDINT\_USBCLK\_DYN}$(mA) = 5 mA (if USB enabled)

Data Transmission Current

The data transmission current represents the power dissipated when transmitting data. This current is expressed in terms of data rate. The calculation is performed by adding the data rate (MB/s) of each DMA and core driven access to peripherals and L2/external memory. This number is then multiplied by a coefficient and V_{DD_INT}. The following equation provides an estimate of all data transmission current.

$I_{DDINT\_DMA\_DR\_DYN}(\text{mA}) = 0.0578 \times \text{data rate (MB/s)} \times V_{DD\_INT}(\text{V})$

For details on using this equation see the related Engineer Zone material.

Table 19. CCLK Dynamic Current per core (mA, with ASF = 1)

	Voltage (V_{DD_INT})						
f_{CCLK}(MHz)	1.190	1.200	1.225	1.250	1.275	1.300	1.320
500	97.9	98.8	101.5	103.9	106.7	109.3	110.8
450	88.6	89.5	91.9	94.1	96.7	98.9	100.6
400	79.3	80.1	82.2	84.3	86.5	88.6	90.1
350	70.0	70.7	72.5	74.4	76.3	78.3	79.4
300	60.6	61.2	63.0	64.6	66.3	68.0	69.1
250	51.3	51.8	53.2	54.7	56.3	57.6	58.5
200	42.0	42.4	43.6	44.8	46.0	47.2	48.2
150	32.5	32.9	34.0	34.8	35.9	37.0	37.4
100	23.2	23.5	24.2	25.0	25.7	26.5	26.9

Asynchronous Flash Read

Table 29. Asynchronous Flash Read

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Switching Characteristics				
t_{AMSADV}	SMC0_Ax (Address)/$\overline{\text{SMC0\_AMSx}}$ Assertion Before SMC0_NORDV Low[1]	PREST × t_{SCLK0} 2		ns
t_{WADV}	SMC0_NORDV Active Low Width[2]	RST × t_{SCLK0} 2		ns
$t_{DADVARE}$	$\overline{\text{SMC0\_ARE}}$ Low Delay From SMC0_NORDV High[3]	PREAT × t_{SCLK0} 2		ns
t_{HARE}	Output[4] Hold After $\overline{\text{SMC0\_ARE}}$ High[5]	RHT × t_{SCLK0} 2		ns
t_{WARE}[6]	$\overline{\text{SMC0\_ARE}}$ Active Low Width[7]	RAT × t_{SCLK0} 2		ns

[1] PREST value set using the SMC_BxETIM.PREST bits.
[2] RST value set using the SMC_BxTIM.RST bits.
[3] PREAT value set using the SMC_BxETIM.PREAT bits.
[4] Output signals are SMC0_Ax, $\overline{\text{SMC0\_AMS}}$, $\overline{\text{SMC0\_AOE}}$.
[5] RHT value set using the SMC_BxTIM.RHT bits.
[6] SMC0_BxCTL.ARDYEN bit = 0.
[7] RAT value set using the SMC_BxTIM.RAT bits.

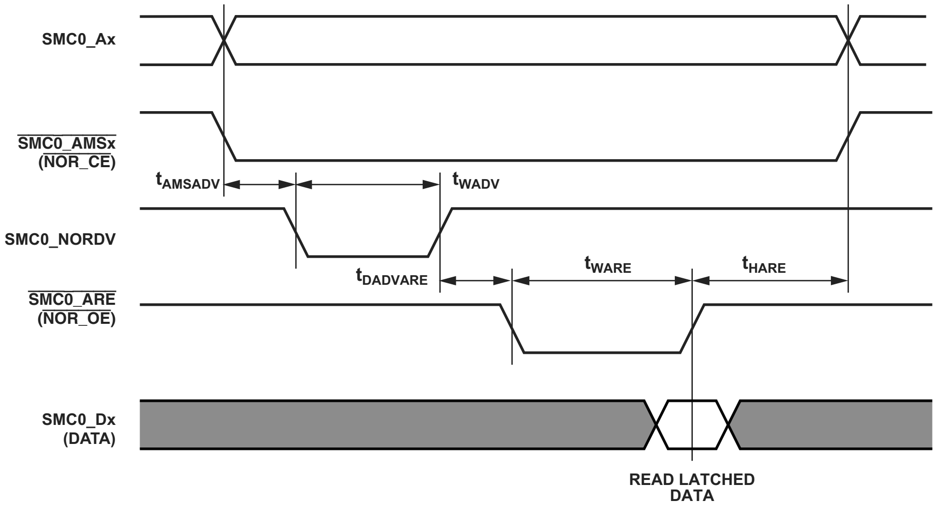

SMC0_Ax
SMC0_AMSx
(NOR_CE)
tAMSADV
tWADV
SMC0_NORDV
tDADVARE
tWARE
tHARE
SMC0_ARE
(NOR_OE)
SMC0_Dx
(DATA)
READ LATCHED
DATA

Figure 13. Asynchronous Flash Read

Bus Request/Bus Grant

Table 35. Bus Request/Bus Grant

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Switching Characteristics				
t_{DBGBR}	$\overline{\text{SMC0\_BG}}$ Delay After $\overline{\text{SMC0\_BR}}$	$2.5 \times t_{SCLK0}$	$3.5 \times t_{SCLK0} + 17.5$	ns
t_{ENGDAT}	DATA Enable After $\overline{\text{SMC0\_BG}}$ Deassertion	3		ns
t_{DBGDAT}	DATA Disable After $\overline{\text{SMC0\_BG}}$ Assertion		3	ns

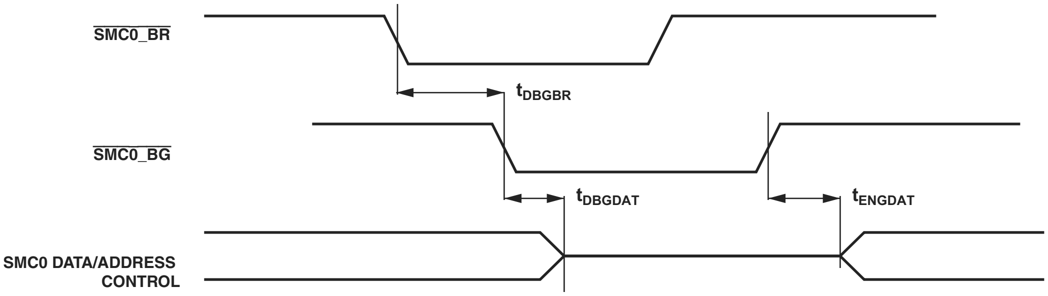
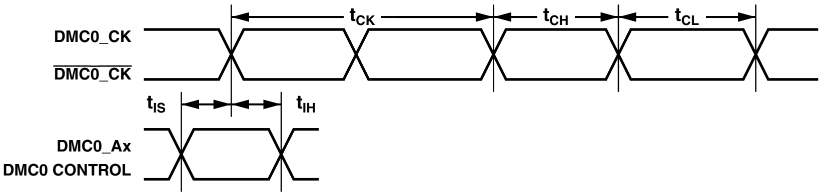

$\overline{\text{SMC0\_BR}}$
t_{DBGBR}
$\overline{\text{SMC0\_BG}}$
t_{DBGDAT}
t_{ENGDAT}
SMC0 DATA/ADDRESS
CONTROL

Figure 18. Bus Request/Bus Grant

DDR2 SDRAM Clock and Control Cycle Timing

Table 36. DDR2 SDRAM Read Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		250 MHz Min	Max	Unit
Switching Characteristics				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	4		ns
t_{CH}	Minimum Clock Pulse Width	0.45	0.55	t_{CK}
t_{CL}	Maximum Clock Pulse Width	0.45	0.55	t_{CK}
t_{IS}	Control/Address Setup Relative to DMC0_CK Rise	350		ps
t_{IH}	Control/Address Hold Relative to DMC0_CK Rise	475		ps


t_{CK}
t_{CH}
t_{CL}
DMC0_CK
$\overline{\text{DMC0\_CK}}$
t_{IS}
t_{IH}
DMC0_Ax
DMC0 CONTROL

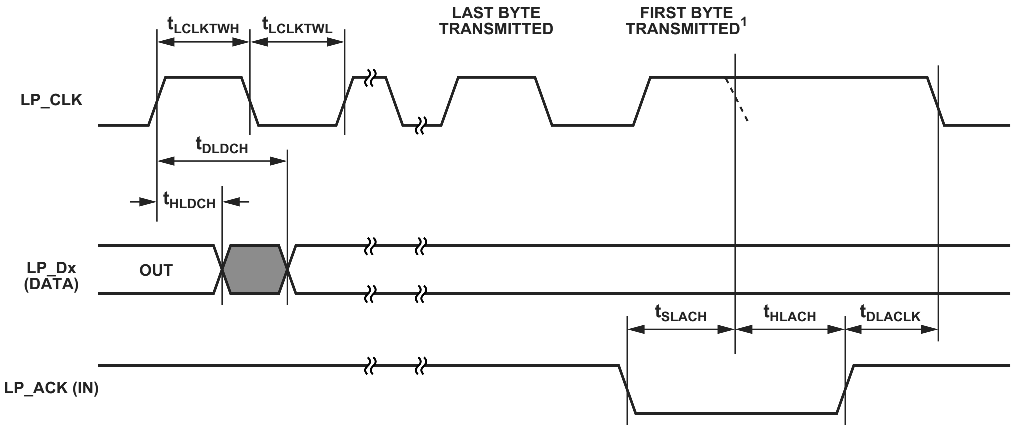
NOTE: CONTROL = $\overline{\text{DMC0\_CS0}}$, DMC0_CKE, $\overline{\text{DMC0\_RAS}}$, $\overline{\text{DMC0\_CAS}}$, AND $\overline{\text{DMC0\_WE}}$.
ADDRESS = DMC0_A00–13, AND DMC0_BA0–1.

Figure 19. DDR2 SDRAM Clock and Control Cycle Timing

Table 45. Link Ports Transmit

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{SLACH}	LP_ACK Setup Before LP_CLK Low	$2 \times t_{SCLK0} + 17.5$		$2 \times t_{SCLK0} + 13.5$		ns
t_{HLACH}	LP_ACK Hold After LP_CLK Low	0		0		ns
Switching Characteristics						
t_{DLDCH}	Data Delay After LP_CLK High		2.5		2.5	ns
t_{HLDCH}	Data Hold After LP_CLK High	1.5		1.5		ns
$t_{LCLKTWL}$[1]	LP_CLK Width Low	$0.4 \times t_{LCLKTPROG}$	$0.6 \times t_{LCLKTPROG}$	$0.4 \times t_{LCLKTPROG}$	$0.6 \times t_{LCLKTPROG}$	ns
$t_{LCLKTWH}$[1]	LP_CLK Width High	$0.4 \times t_{LCLKTPROG}$	$0.6 \times t_{LCLKTPROG}$	$0.4 \times t_{LCLKTPROG}$	$0.6 \times t_{LCLKTPROG}$	ns
t_{LCLKTW}[1]	LP_CLK Period	$t_{LCLKTPROG}$ 1.2		$t_{LCLKTPROG}$ 1.2		ns
t_{DLACLK}	LP_CLK Low Delay After LP_ACK High	$t_{SCLK0} + 4$	$(2 \times t_{SCLK0}) + t_{LCLK} + 10$	$t_{SCLK0} + 4$	$(2 \times t_{SCLK0}) + t_{LCLK} + 10$	ns

[1] See Table 17 on Page 53 in Clock Related Operating Conditions for details on the minimum period that may be programmed for $t_{LCLKTPROG}$.



NOTES
The t_{SLACH} and t_{HLACH} specifications apply only to the LP_ACK falling edge. If these specifications are met, LP_CLK would extend and the dotted LP_CLK falling edge would not occur as shown. The position of the dotted falling edge can be calculated using the $t_{LCLKTWH}$ specification. $t_{LCLKTWH}$ Min should be used for t_{SLACH} and $t_{LCLKTWH}$ Max for t_{HLACH}.

Figure 35. Link Ports—Transmit

Serial Peripheral Interface (SPI) Port—Master Timing

Table 51 and Figure 40 describe SPI port master operations.

When internally generated, the programmed SPI clock ($f_{SPICLKPROG}$) frequency in MHz is set by the following equation where BAUD is a field in the SPI_CLK register that can be set from 0 to 65535:

$$f_{SPICLKPROG} = \frac{f_{SCLK1}}{(BAUD + 1)}$$

$$t_{SPICLKPROG} = \frac{1}{f_{SPICLKPROG}}$$

Note that:

- In dual mode data transmit the SPI_MISO signal is also an output.
- In quad mode data transmit the SPI_MISO, SPI_D2, and SPI_D3 signals are also outputs.
- In dual mode data receive the SPI_MOSI signal is also an input.
- In quad mode data receive the SPI_MOSI, SPI_D2, and SPI_D3 signals are also inputs.
- To add additional frame delays see the documentation for the SPI_DLY register in the hardware reference manual.

Table 51. Serial Peripheral Interface (SPI) Port Master Timing

		V_{DD_EXT} 1.8 V Nominal		V_{DD_EXT} 3.3 V Nominal		
Parameter		Min	Max	Min	Max	Unit
Timing Requirements						
t_{SSPIDM}	Data Input Valid to SPI_CLK Edge (Data Input Setup)	4.6		3.2		ns
t_{HSPIDM}	SPI_CLK Sampling Edge to Data Input Invalid	1.3		1.3		ns
Switching Characteristics						
t_{SDSCIM}	$\overline{\text{SPI\_SEL}}$ Low to First SPI_CLK Edge	$0.5 \times t_{SCLK1}$ 2		$0.5 \times t_{SCLK1}$ 2		ns
t_{SPICHM}	SPI_CLK High Period[1]	$0.5 \times t_{SPICLKPROG}$ 1.5		$0.5 \times t_{SPICLKPROG}$ 1.5		ns
t_{SPICLM}	SPI_CLK Low Period[1]	$0.5 \times t_{SPICLKPROG}$ 1.5		$0.5 \times t_{SPICLKPROG}$ 1.5		ns
t_{SPICLK}	SPI_CLK Period[1]	$t_{SPICLKPROG}$ 1.5		$t_{SPICLKPROG}$ 1.5		ns
t_{HDSM}	Last SPI_CLK Edge to $\overline{\text{SPI\_SEL}}$ High	$(0.5 \times t_{SCLK1})$ 1.5		$(0.5 \times t_{SCLK1})$ 1.5		ns
t_{SPITDM}	Sequential Transfer Delay	t_{SCLK1} 1.5		t_{SCLK1} 1.5		ns
$t_{DDSPIDM}$	SPI_CLK Edge to Data Out Valid (Data Out Delay)		2.6		2.6	ns
$t_{HDSPIDM}$	SPI_CLK Edge to Data Out Invalid (Data Out Hold)	1		1		ns

[1] See Table 17 on Page 53 in Clock Related Operating Conditions for details on the minimum period that may be programmed for $t_{SPICLKPROG}$.

Serial Peripheral Interface (SPI) Port—Open Drain Mode Timing

In Figure 44 and Figure 45, the outputs can be SPI_MOSI SPI_MISO, SPI_D2, and/or SPI_D3 depending on the mode of operation.

Table 54. SPI Port ODM Master Mode Timing

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Switching Characteristics				
$t_{HDSPIODMM}$	SPI_CLK Edge to High Impedance from Data Out Valid	1		ns
$t_{DDSPIODMM}$	SPI_CLK Edge to Data Out Valid from High Impedance	0	6	ns

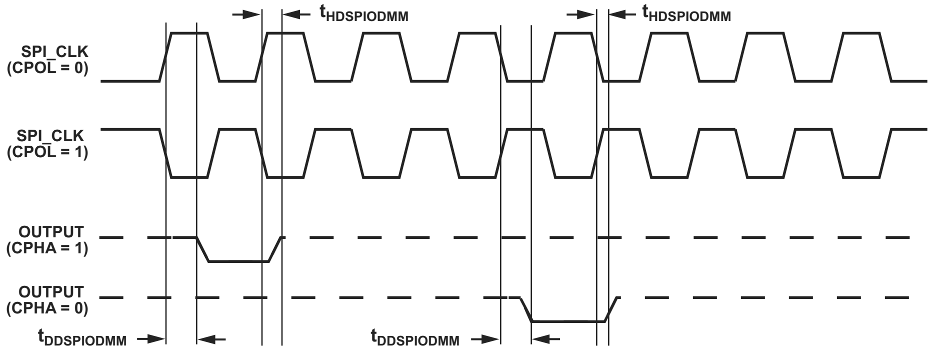

tHDSPIODMM
tHDSPIODMM
SPI_CLK (CPOL = 0)
SPI_CLK (CPOL = 1)
OUTPUT (CPHA = 1)
OUTPUT (CPHA = 0)
tDDSPIODMM
tDDSPIODMM

Figure 44. ODM Master

Table 55. SPI Port ODM Slave Mode

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Timing Requirements				
$t_{HDSPIODMS}$	SPI_CLK Edge to High Impedance from Data Out Valid	0		ns
$t_{DDSPIODMS}$	SPI_CLK Edge to Data Out Valid from High Impedance		11.5	ns

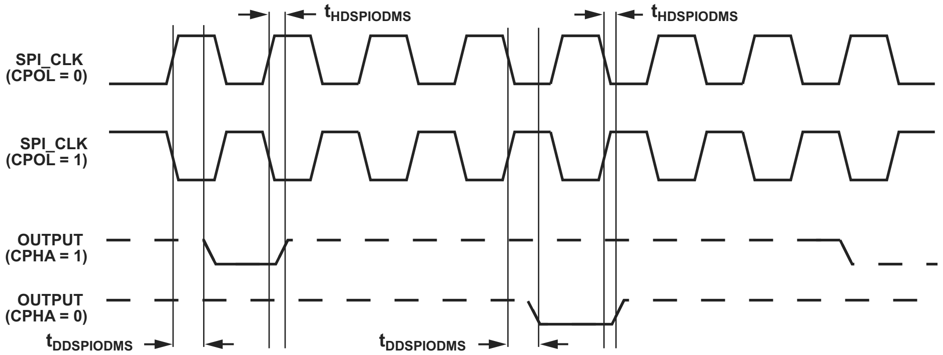

tHDSPIODMS
tHDSPIODMS
SPI_CLK (CPOL = 0)
SPI_CLK (CPOL = 1)
OUTPUT (CPHA = 1)
OUTPUT (CPHA = 0)
tDDSPIODMS
tDDSPIODMS

Figure 45. ODM Slave

OUTPUT DRIVE CURRENTS

Figure 59 through Figure 64 show typical current-voltage characteristics for the output drivers of the ADSP-BF60x Blackfin processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

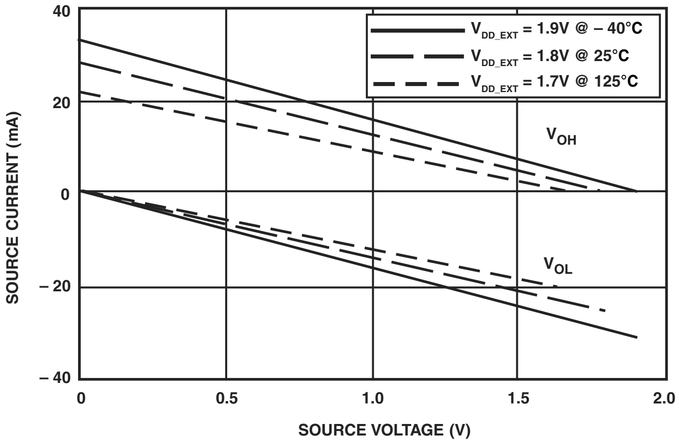


Figure 59. Driver Type A Current (1.8 V V_{DD_EXT})

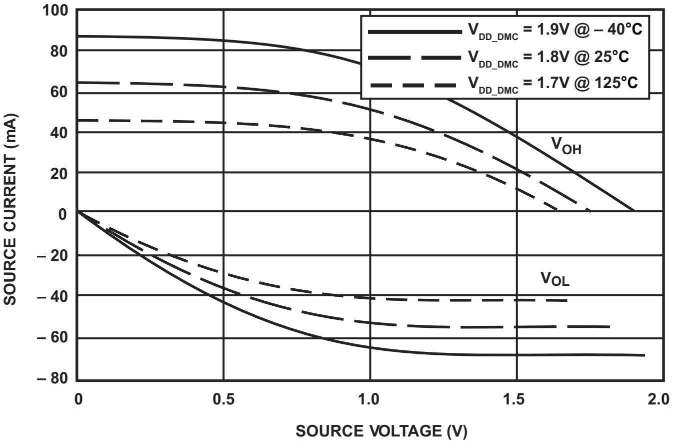


Figure 61. Driver Type B Current (1.8 V V_{DD_DMC})

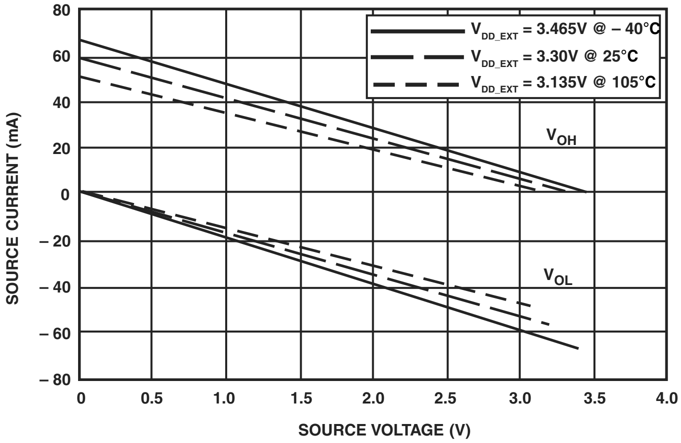


Figure 60. Driver Type A Current (3.3 V V_{DD_EXT})

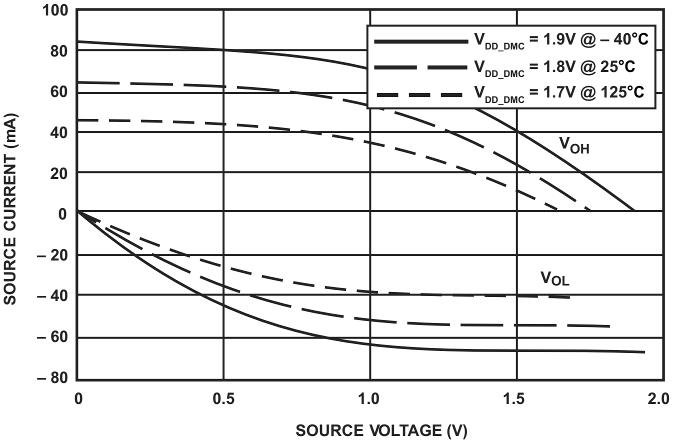


Figure 62. Driver Type C Current (1.8 V V_{DD_DMC})

AUTOMOTIVE PRODUCTS

The models in the following table are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the product specifications section of this data sheet carefully. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Model[1]	Max. Core Clock	Temperature Range[2]	Package Description	Package Option
ADBF606WCBCZ4xx	400 MHz	40℃ to +105℃	349-Ball CSP_BGA	BC-349-1
ADBF607WCBCZ5xx	500 MHz	40℃ to +105℃	349-Ball CSP_BGA	BC-349-1
ADBF608WCBCZ5xx	500 MHz	40℃ to +105℃	349-Ball CSP_BGA	BC-349-1
ADBF609WCBCZ5xx	500 MHz	40℃ to +105℃	349-Ball CSP_BGA	BC-349-1

[1] Z =RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 52 for the junction temperature (T_J) specification which is the only temperature specification.

ORDERING GUIDE

Model[1]	Max. Core Clock	Temperature Range[2]	Package Description	Package Option
ADSP-BF606KBCZ-4	400 MHz	0℃ to +70℃	349-Ball CSP_BGA	BC-349-1
ADSP-BF606BBCZ-4	400 MHz	40℃ to +85℃	349-Ball CSP_BGA	BC-349-1
ADSP-BF607KBCZ-5	500 MHz	0℃ to +70℃	349-Ball CSP_BGA	BC-349-1
ADSP-BF607BBCZ-5	500 MHz	40℃ to +85℃	349-Ball CSP_BGA	BC-349-1
ADSP-BF608KBCZ-5	500 MHz	0℃ to +70℃	349-Ball CSP_BGA	BC-349-1
ADSP-BF608BBCZ-5	500 MHz	40℃ to +85℃	349-Ball CSP_BGA	BC-349-1
ADSP-BF609KBCZ-5	500 MHz	0℃ to +70℃	349-Ball CSP_BGA	BC-349-1
ADSP-BF609BBCZ-5	500 MHz	40℃ to +85℃	349-Ball CSP_BGA	BC-349-1

[1] Z =RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 52 for the junction temperature (T_J) specification which is the only temperature specification.

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