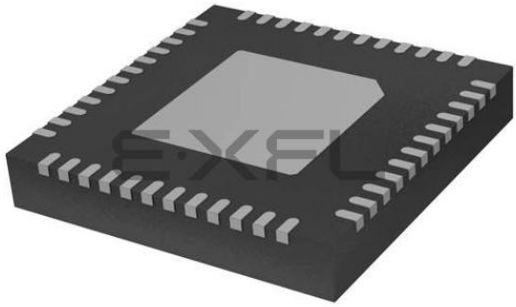

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Details	
Product Status	Active
Applications	BLDC Controller
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (32kB)
Controller Series	STM32F031x6x7
RAM Size	4K x 8
Interface	I²C, SPI, UART/USART
Number of I/O	16
Voltage - Supply	6.7V ~ 45V
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-VFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stspin32f0a

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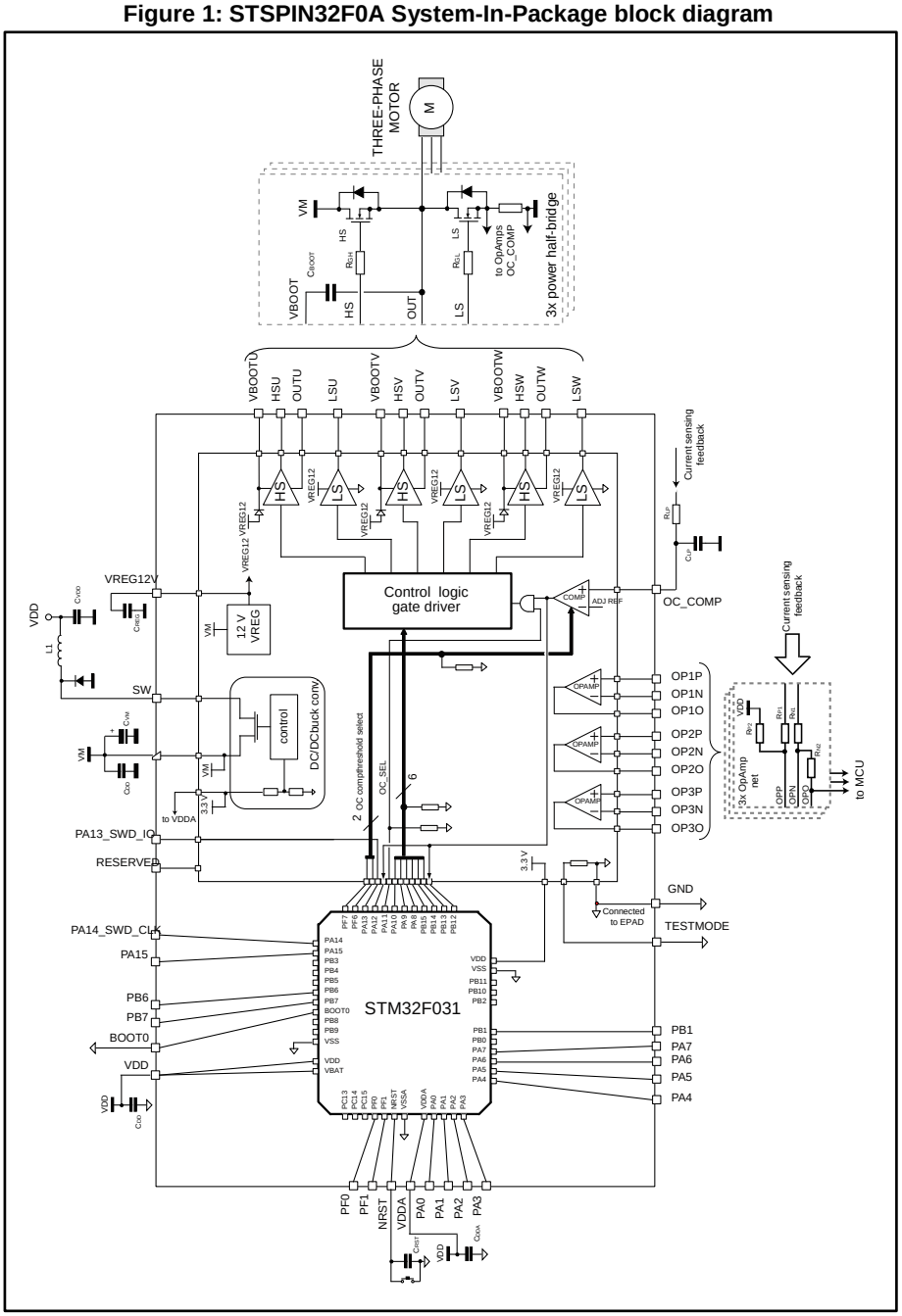
2 Block diagrams

Figure 1: STSPIN32F0A System-In-Package block diagram



3.2 ESD protections

Table 2: ESD protection ratings

Symbol	Parameter	Test condition	Class	Value	Unit
HBM	Human body model	Conforming to ANSI/ESDA/JEDEC JS-001-2014	H2	2	kV
CDM	Charge device model	Conforming to ANSI/ESDA/JEDEC JS-002-2014	C2	750	V

3.3 Recommended operating conditions

Table 3: Recommended operating conditions

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_M	Power supply voltage	-	6.7 (1)	-	45	V
dV_M/dt	Power supply voltage slope	V_M = 45 V	-	-	0.75	V/µs
V_{DDA}	DC/DC regulator output voltage	-	-	3.3	-	V
L_{SW}	Output inductance	-	-	22	-	µH
C_{DDA}	Output capacitance	-	47	-	-	µF
ESR_{DDA}	Output capacitor ESR	-	-	-	200	mΩ
V_{REG12}	Linear regulator output and gate driver supply voltage	13 < V_M < 45 V	-	12	-	V
		Shorted to VM	6.7(1)	-	15	
C_{REG}	Load capacitance	-	1	10	-	µF
ESR_{REG}	ESR load capacitance	-	-	-	1.2	Ω
V_{BO}	Floating supply voltage (2)	-	-	V_{REG12} - 1	15	V
V_{CP}	Comparator input voltage	-	0	-	1	V
T_j	Operating junction temperature	Analog IC	-40	-	125	°C
		MCU (3)	-40	-	125	°C

Notes:

(1) UVLO threshold V_{MOn_max}.

(2) $V_{BO} = V_{BOOT} - V_{OUT}$.

(3) See the STM32F031C6 datasheet (suffix 7 version).

3.4 Thermal data

Thermal values are calculated by simulation with the following boundary conditions: 2s2p board as per the std. JEDEC (JESD51-7) in natural convection, board dimensions: 114.3 x 76.2 x 1.6 mm, ambient temperature: 25 °C.

Table 4: Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ (JA)}$	Thermal resistance junction to ambient	45.6	°C/W

4 Electrical characteristics

Testing conditions: V_M = 15 V; V_{DD} = 3.3 V, unless otherwise specified.

Typical values are tested at T_j = 25 °C, minimum and maximum values are guaranteed by thermal characterization in the temperature range of -40 to 125 °C, unless otherwise specified.

Table 5: Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Power supply and standby mode						
I_M	V_M current consumption	V_M = 45 V; V_{DD} = 3.5 V externally supplied	-	2	2.6	mA
		Standby PF7 = '0' PF6 = '0 V_M = 45 V; V_{DD} = 3.5 V externally supplied	-	880	1100	µA
V_{MOn}	V_M UVLO turn-on threshold	V_M rising from 0 V	6.0	6.3	6.6	V
V_{MOff}	V_M UVLO turn-off threshold	V_M falling from 8 V	5.8	7.1	6.4	V
V_{MHys}	V_M UVLO threshold hysteresis	-	-	0.2	-	V
I_{DD}	V_{DD} current consumption	V_{DD} = 3.5 V externally supplied (1)	-	2.5	5	mA
		Standby PF7 = '0' PF6 = '0' V_{DD} = 3.5 V externally supplied(1)	-	2.5	5	
I_{DDA}	V_{DDA} current consumption	V_{DD} = 3.5 V externally supplied(1)	-	400	550	µA
		Standby PF7 = '0' PF6 = '0' V_{DD} = 3.5 V externally supplied(1)	-	80	125	
V_{DDOn}	V_{DD} UVLO turn-on threshold	V_{DD} rising from 0 V	2.5	2.65	2.8	V
V_{DDOff}	V_{DD} UVLO turn-off threshold	V_{DD} falling from 3.3 V	2.2	2.35	2.5	V
V_{DDHys}	V_{DD} UVLO threshold hysteresis	-	-	0.3	-	V
I_{REG12}	V_{REG} current consumption	V_{REG} = 13 V externally supplied, V_M = 45 V; no commutation	-	800	1200	µA
		Standby PF7 = '0' PF6 = '0' V_{REG} = 13 V externally supplied	-	800	1200	
$V_{REG12On}$	V_{REG12} UVLO turn-on threshold	V_{REG12} rising from 0 V	6.0	6.3	6.6	V
$V_{REG12Off}$	V_{REG12} UVLO turn-off threshold	V_{REG12} falling from 8 V	5.8	6.1	6.4	V
$V_{REG12Hys}$	V_{REG12} UVLO threshold hysteresis	-	-	0.25	-	V
I_{BOOT}	V_{BO} current consumption	HS on V_{BO} = 13 V	-	200	290	µA
V_{BOOn}	V_{BO} UVLO turn-on threshold	V_{BO} rising from 0 V	5.5	5.8	6.1	V
V_{BOOff}	V_{BO}UVLO turn-off threshold	V_{BO} falling from 8 V	5.3	5.6	5.9	V

5 Pin description

Figure 4: STSPIN32F0A SiP pin connection (top view)

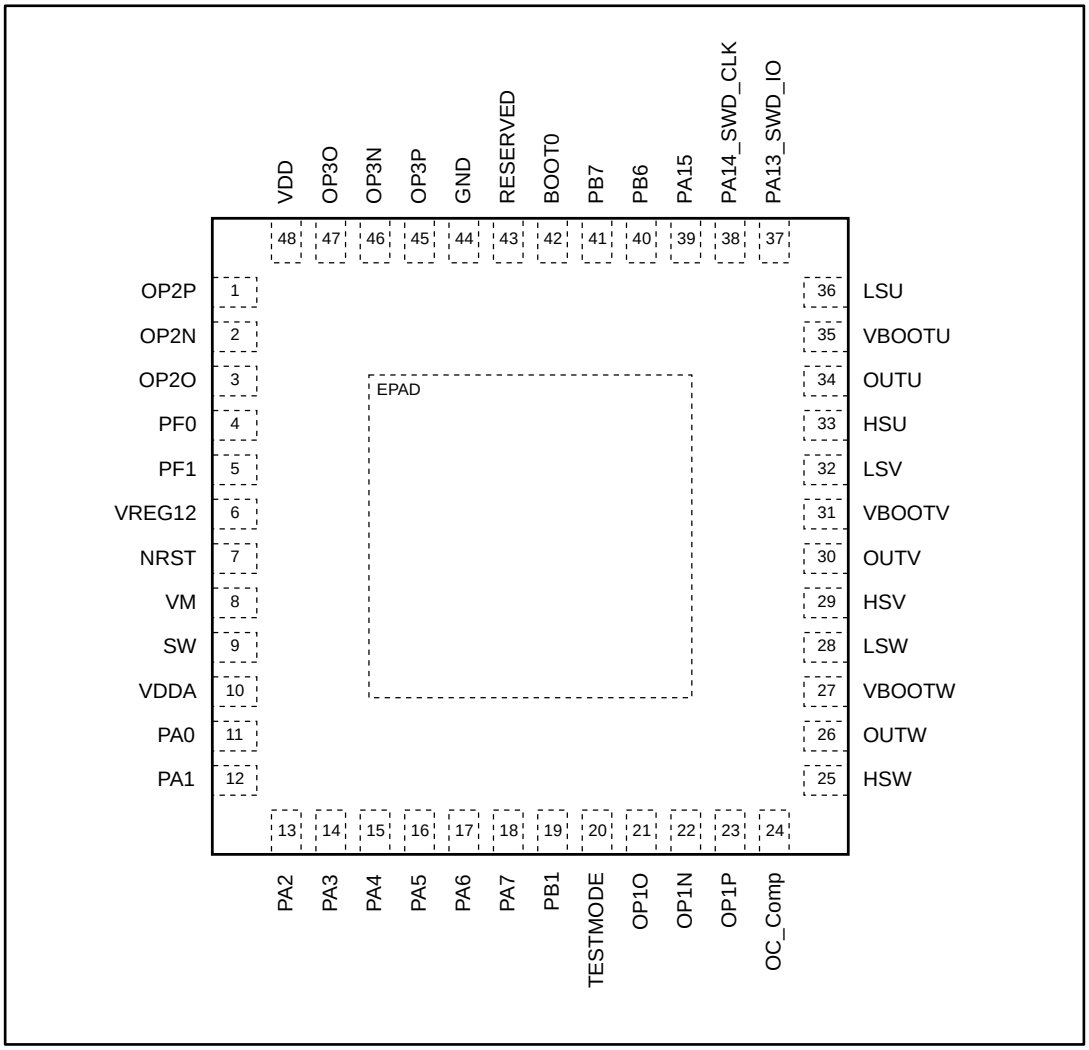


Table 6: STSPIN32F0A SiP pin description

No.	Name	Type	Function
1	OP2P	Analog in	Op amp 2 non-inverting input
2	OP2N	Analog in	Op amp 2 inverting input
3	OP2O	Analog out	Op amp 2 output
4	PF0	GPIO	MCU PF0
5	PF1	GPIO	MCU PF1
6	VREG12	Power	12 V linear regulator output
7	NRST	GPIO	MCU reset pin
8	VM	Power	Power supply voltage (bus voltage)
9	SW	Analog out	3.3 V DC/DC buck regulator switching node

No.	Name	Type	Function
10	VDDA	Power	MCU analog power supply voltage
11	PA0	GPIO	MCU PA0
12	PA1	GPIO	MCU PA1
13	PA2	GPIO	MCU PA2
14	PA3	GPIO	MCU PA3
15	PA4	GPIO	MCU PA4
16	PA5	GPIO	MCU PA5
17	PA6	GPIO	MCU PA6
18	PA7	GPIO	MCU PA7
19	PB1	GPIO	MCU PB1
20	TESTMODE	Digital In	Test mode input
21	OP1O	Analog out	Op amp 1 output
22	OP1N	Analog in	Op amp 1 inverting input
23	OP1P	Analog in	Op amp 1 non-inverting input
24	OC_COMP	Analog in	Overcurrent comparator input
25	HSW	Analog out	W phase high-side driver output
26	OUTW	Power	W phase high-side (floating) common voltage
27	VBOOTW	Power	W phase bootstrap supply voltage
28	LSW	Analog out	W phase low-side driver output
29	HSV	Analog out	V phase high-side driver output
30	OUTV	Power	V phase high-side (floating) common voltage
31	VBOOTV	Power	V phase bootstrap supply voltage
32	LSV	Analog out	V phase low-side driver output
33	HSU	Analog out	U phase high-side driver output
34	OUTU	Power	U phase high-side (floating) common voltage
35	VBOOTU	Power	U phase bootstrap supply voltage
36	LSU	Analog out	U phase low-side driver output
37	PA13_SWD_IO	GPIO	MCU PA13/SWDIO (system debug data via analog IC)
38	PA14_SWD_CLK	GPIO	MCU PA14/SWDCLK (system debug clock)
39	PA15	GPIO	MCU PA15
40	PB6	GPIO	MCU PB6
41	PB7	GPIO	MCU PB7
42	BOOT0	Digital in	MCU BOOT0
43	RESERVED	-	Reserved for test mode (can be left floating in application)
44	GND	Power	Ground
45	OP3P	Analog in	Op amp 3 non-inverting input
46	OP3N	Analog in	Op amp 3 inverting input

MCU pad	Type	Analog IC pad	Alternate and additional functions
PA9	I/O - FTf	HS2	TIM1_CH2(1)
PA10	I/O - FTf	HS3	TIM1_CH3
PA11	I/O - FT	OC_SEL	Push-pull output(1)
PA12	I/O - FT	OC_COMP_INT2	TIM1_ETR(1)
PA13_SWD_IO	I/O - FT	SWDIO_INT	IR_OUT, SWDIO
PF6	I/O - FTf	OC_TH_STBY2	Push-pull output(1)
PF7	I/O - FTf	OC_TH_STBY1	Push-pull output(1)
PA14_SWD_CLK	I/O - FT	-	USART1_TX, SWCLK
PA15	I/O - FT	-	SPI1_NSS, I2S1_WS, TIM2_CH_ETR, EVENTOUT, USART1_RX
PB6	I/O - FTf	-	I2C1_SCL, USART1_TX, TIM16_CH1N
PB7	I/O - FTf	-	I2C1_SDA, USART1_RX, TIM17_CH1N
VBAT, VDD	S	VDD	Backup and digital power supply
VSS, VSSA	S	-	Ground
BOOT0	I	-	Boot memory selection
PC13, PC14, PC15, PB0, PB2, PB10, PB11, PA15, PB3, PB4, PB5, PB8, PB9	-	-	Not connected

Notes:

(1)The analog IC is designed to support these GPIOs configuration only. Different configuration could cause device malfunctioning. The GPIO input configuration without pull-up or pull-down is always allowed.

Each unused GPIO inside the SiP should be configured in the OUTPUT mode low level after the startup by software.

Table 8: STSPIN32F0A analog IC pad description

Pinout name	Pad name	Type	Function
PA13_SWD_IO	SYS_SWDIO	Digital I/O	System debug data (connected to the output through the analog IC)
VDDA	VDD_3V3	Power	3.3 V DC/DC buck regulator voltage output
VM	VM	Power	Power supply voltage (bus voltage)
SW	SW	Analog out	3.3 V DC/DC buck regulator switching node
VREG12	VREG12	Power	12 V linear regulator output
VBOOTU	VBOOTU	Power	U phase bootstrap supply voltage

6 Device description

The STSPIN32F0A is a System-In-Package providing an integrated solution suitable for driving the three-phase BLDC motors. The device will be developed in the BCD8s (0.18 µm) technology.

6.1 UVLO and thermal protections

Table 9: "UVLO and OT protection management" summarizes the UVLO and OT protection management.

Table 9: UVLO and OT protection management

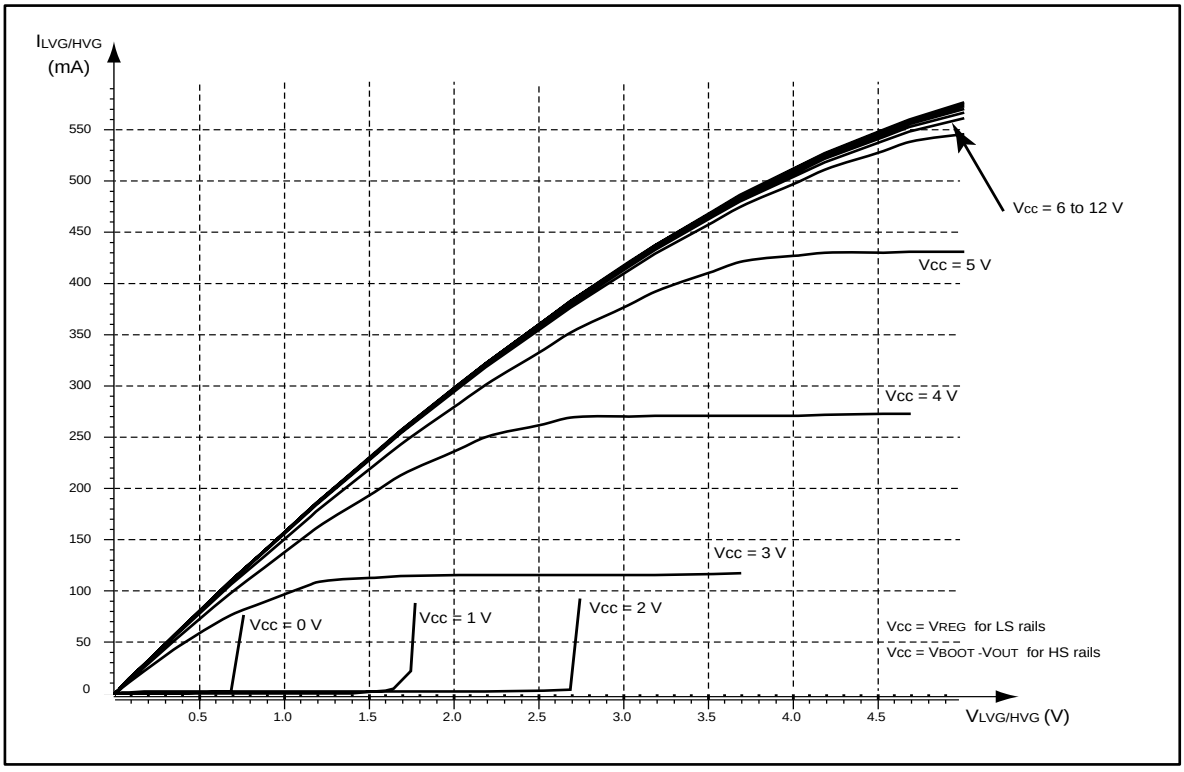
Block	V_M UVLO	V_{DD} UVLO	V_{REG12} UVLO	V_{BOOT} UVLO	Lin. Reg OT	DC/DC Reg OT
DC/DC regulator	-	-	-	-	-	OFF
Linear regulator	OFF	OFF	-	-	OFF	-
Op amps and OC comp	OFF	OFF	-	-	-	-
HSU, HSV, HSW output	LOW	LOW	LOW (1)	LOW(1), (2)	-	-
LSU, LSV, LSW output	LOW	LOW	LOW(1)	-	-	-

Notes:

(1)The N-channel of the gate driver is turned ON with all the available supply voltage, refer to *Figure 5: "Gate drivers' outputs characteristics in UVLO conditions"*.

(2)Only the high-side gate driver in which the UVLO condition is detected (e.g. UVLO on VBOOTU causes the HSU turning off).

Figure 5: Gate drivers' outputs characteristics in UVLO conditions



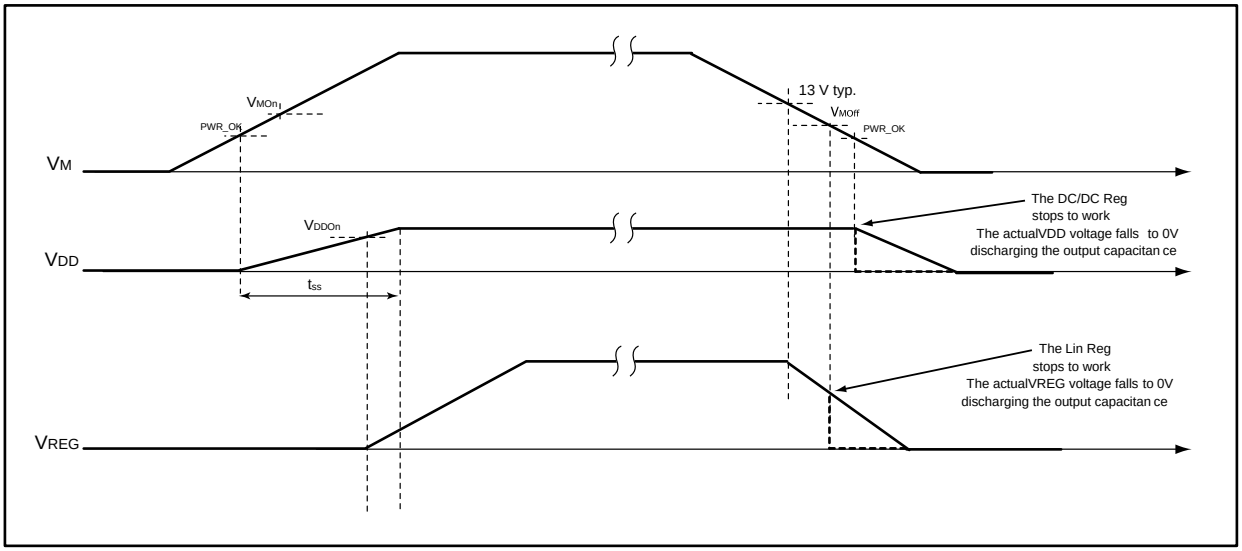
6.1.1 UVLO on supply voltages

The STSPIN32F0A device provides UVLO protections on all power supplies.

The device enters into the undervoltage condition when the power supply voltage falls below the off threshold voltage and expires when the motor supply voltage goes over the on threshold voltage.

Table 9: "UVLO and OT protection management" shows the UVLO protection management: which blocks are switched off after an UVLO event.

Figure 6: Power-up and power-down sequence



6.1.2 Thermal protection

The device embeds an overtemperature shut-down protection. The thermal sensors are placed next to the DC/DC and linear regulator blocks.

When the OT protection is triggered the correspondent block is switched off, the thermal shut-down condition only expires when the temperature goes below the "T_{SD} - T_{hys}" temperature (auto-restart).

Table 9: "UVLO and OT protection management" shows the thermal protection management which blocks are switched off after an overtemperature event.

6.2 DC/DC buck regulator

The internal DC/DC buck converter provides the 3.3 V supply voltage suitable to supply the MCU and other external devices.

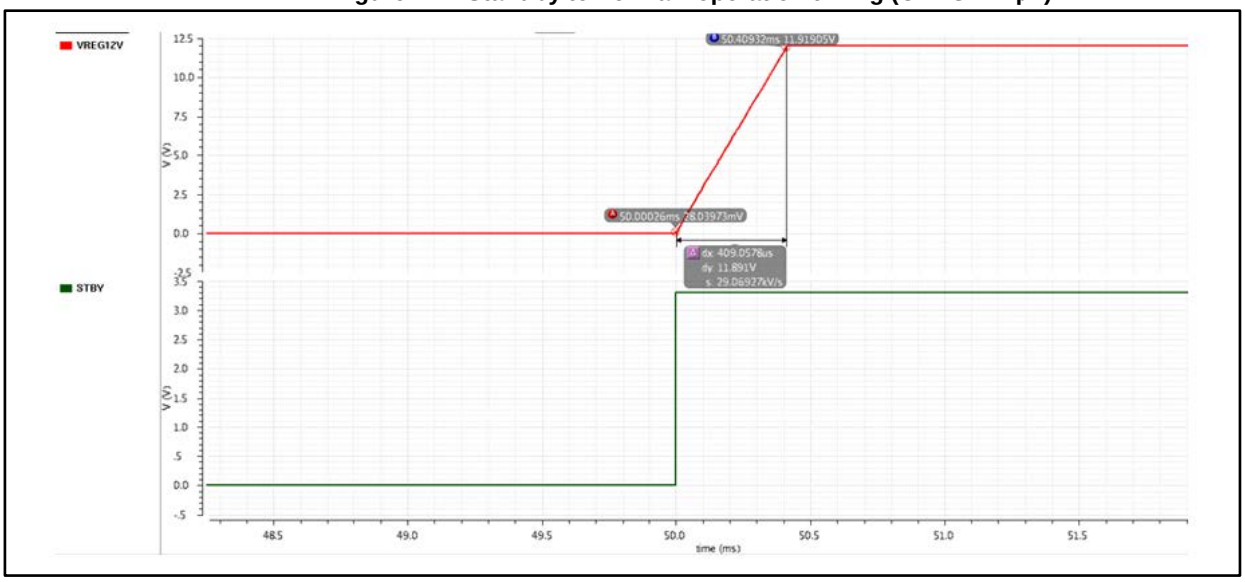
The regulator operates in the discontinuous current mode (DCM).

A soft-start function with fixed start-up time is implemented to minimize the inrush current at the start-up, refer to *Figure 8: "Soft-start timing"*.

An overcurrent and short-circuit protection is provided.

If the failure event occurs on the SW pin and the I_{OVC} threshold is reached the regulator is latched off. To restart the DC/DC regulator a power-down and power-up cycle of device supply voltage (V_M) is mandatory.

Figure 11: “Standby to normal” operation timing (CREG = 1 µF)



Equation 1

$$t_{REG} = \frac{C_{REG} \cdot V_{REG12}}{I_{REG12,lim}}$$

6.5 Gate drivers

The STSPIN32F0A device integrates a triple half-bridge gate driver able to drive N-channel power MOSFETs or IGBTs. The high-side section is supplied by a bootstrapped voltage technique with an integrated bootstrap diode.

All the input lines (refer to *Figure 2: "Analog IC block diagram"*) are connected to

a pull-down resistor (60 kΩ typical value) to guarantee the low logic level during the device start-up.

The high- and low-side outputs of same half-bridge cannot be simultaneously driven high thanks to an integrated interlocking function.

All the input lines of the analog IC have an internal pull-down to guarantee the low logic level during the device start-up and when the MCU lines are not present.

Figure 12: HSE clock source timing diagram

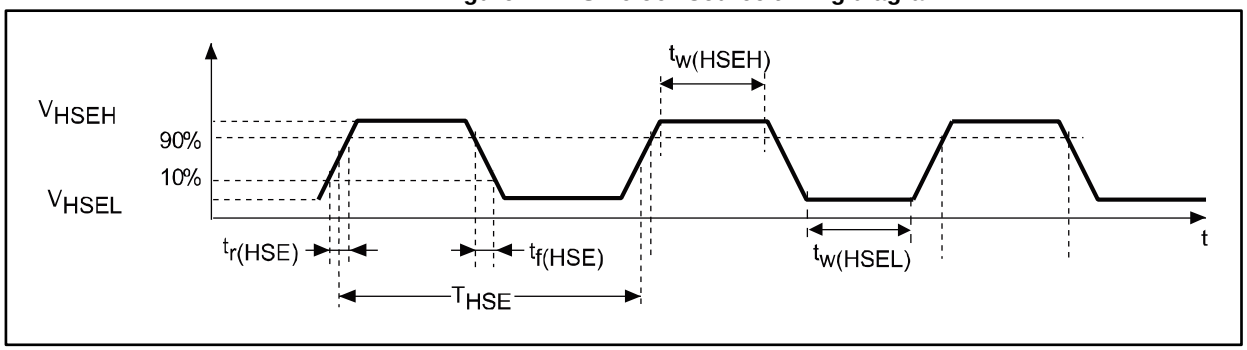
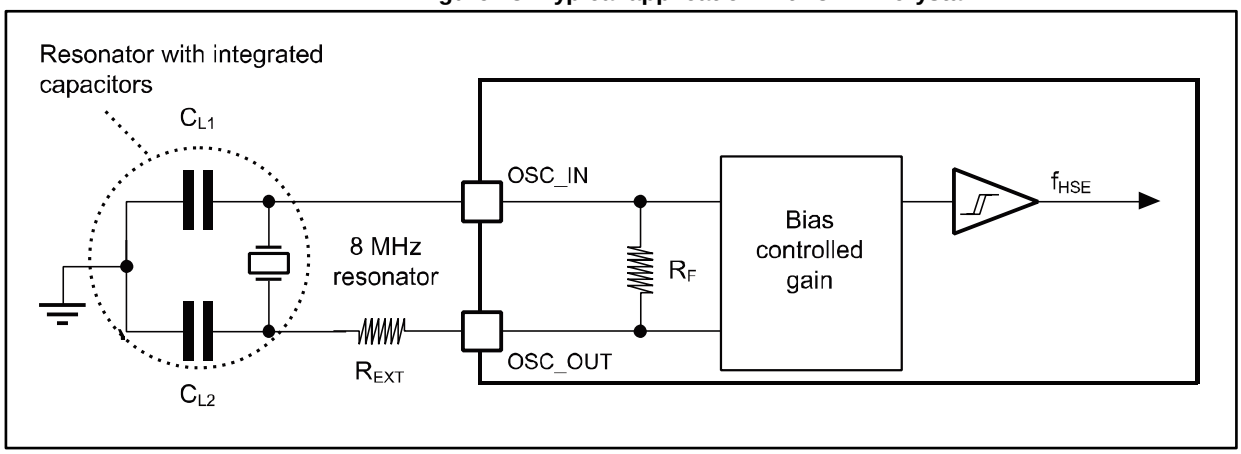


Figure 13: Typical application with 8 MHz crystal



In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The R_{EXT} value depends on the crystal characteristics (refer to the crystal resonator manufacturer for more details on them).

6.6.4 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted deadtimes.

This timer is used to generate the PWM signal for the three half-bridge gate drivers as shown in *Table 10: "TIM1 channel configuration"*.

Table 10: TIM1 channel configuration

MCU I/O	Analog IC input	TIM1 channel
PB13	LS1	TIM1_CH1N
PB14	LS2	TIM1_CH2N
PB15	LS3	TIM1_CH3N
PA8	HS1	TIM1_CH1
PA9	HS2	TIM1_CH2
PA10	HS3	TIM1_CH3

6.7 Test mode

A dedicated pin TESTMODE is available to enter into the test mode.

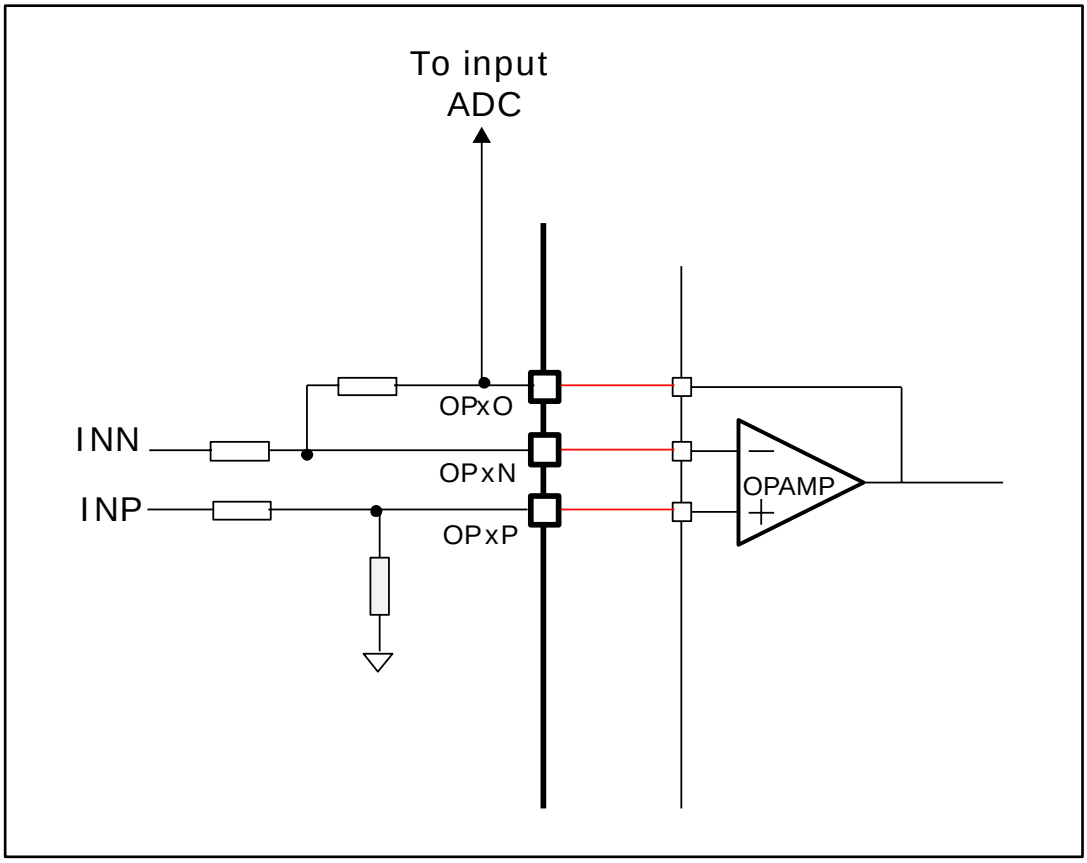
In the application, the TESTMODE pin should be shorted to GND in order not to enter the test mode inadvertently.

6.8 Operational amplifiers

The device integrates three rail-to-rail operational amplifiers suitable for signal conditioning, in particular for current sensing.

The operational amplifiers provide a rail-to-rail output stage with fast recovery in the saturation condition. The output stage saturation happens in linear applications when a high amplitude input signal occurs and causes the output of the operational amplifier to move outside its real capabilities.

Figure 14: Operational amplifiers



6.9 Comparator

A comparator is available to perform an overcurrent protection. The OC Comp pin can be connected to the shunt resistor to monitor the load current, the internal OC threshold can be set via MCU (PF6 and PF7 port, see *Table 12: "OC threshold values"*).

When an OC event is triggered, the OC comparator output signals the OC event to the PB12 and PA12 inputs of MCU (BKIN and ETR).

Depending on the status of the OC_SEL signal (see *Table 11: "OC protection selection"*) the OC event is acting directly on the control logic of the gate driver switching off all high-side gate outputs, and consequently the external high-side power switches.

Figure 15: Comparator

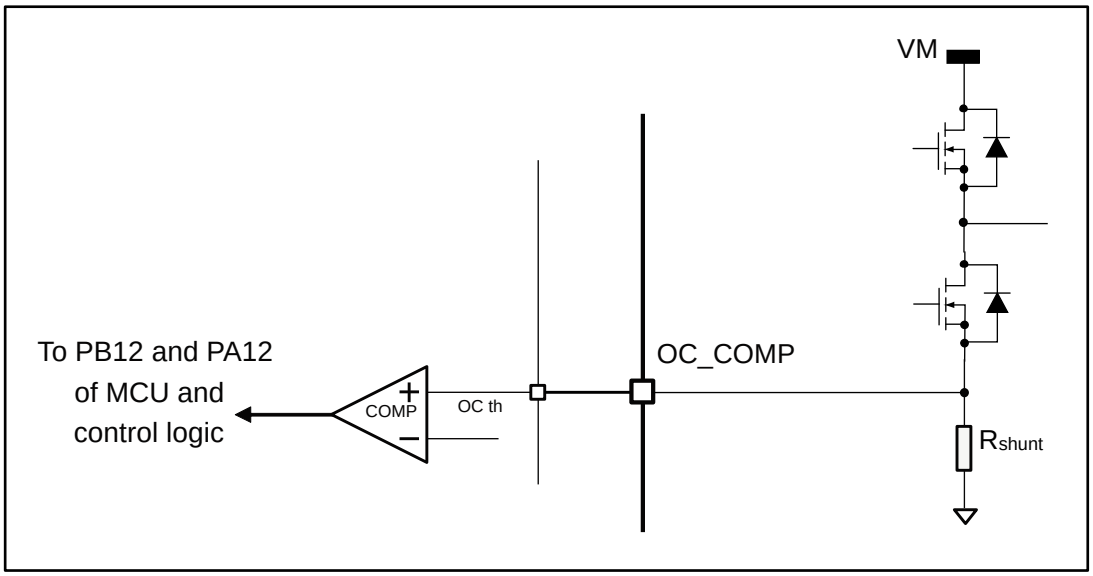


Table 11: OC protection selection

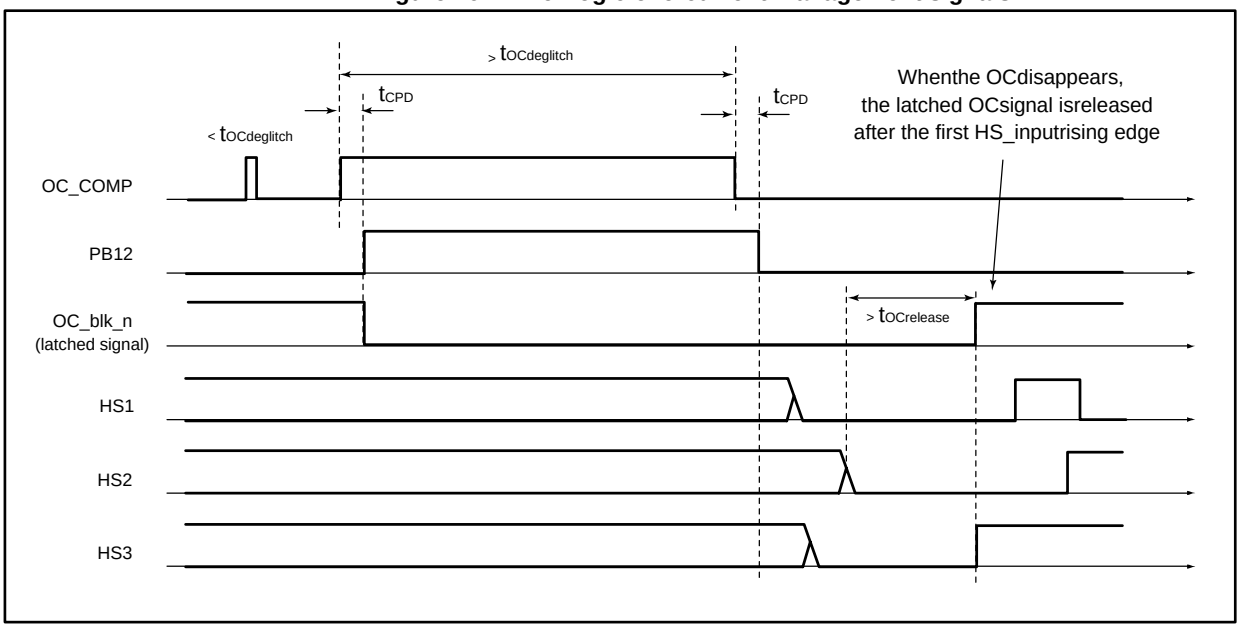
OC_SEL (PA11)	Function
0	OC comparator output signal is visible only to MCU (default)
1	OC comparator output signal is visible to MCU and also acts on gate driver control logic

Table 12: OC threshold values

OC_TH_STBY2 (PF6)	OC_TH_STBY1 (PF7)	OC threshold [mV]	Note
0	0	N.A.	Standby mode (see *Section 6.4: "Standby mode"*)
0	1	100	-
1	0	250	-
1	1	500	-

When the overcurrent condition disappears, the latched overcurrent signal is released only after all the high-side outputs are kept low for at least $t_{OCrelease}$ time. (Refer to *Figure 16: "Driver logic overcurrent management signals"*).

Figure 16: Driver logic overcurrent management signals



8 Package information

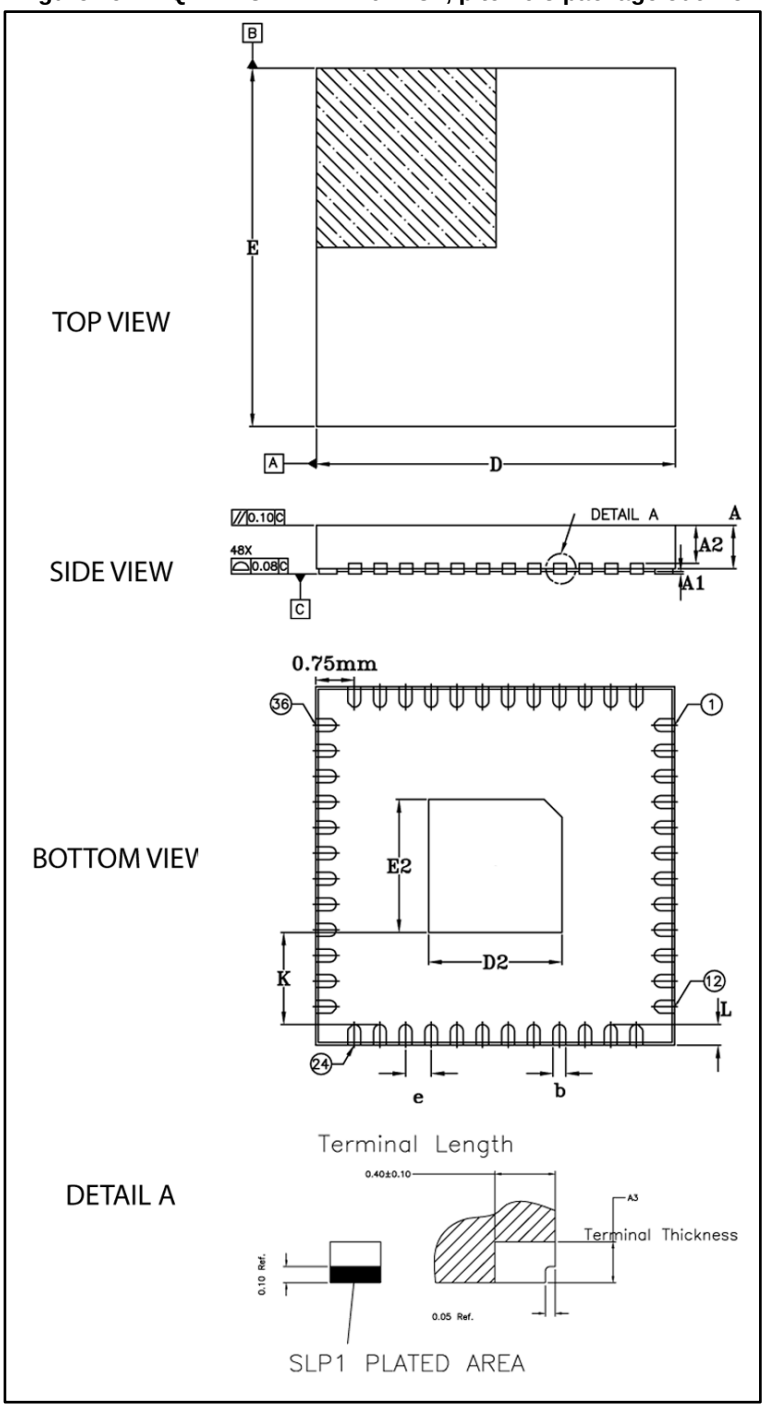
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

A customized VFQFPN48 7 x 7 package is proposed. A smaller EPAD, internally connected to the ground pin, is desired to place through holes on the bottom of the package.

Lead plating is Nickel/Palladium/Gold (Ni/Pd/Au).

8.1 VFQFPN48 7 x 7 package information

Figure 19: VFQFPN48 7 x 7 x 1.0 - 48L, pitch 0.5 package outline



10 Revision history

Table 15: Document revision history

Date	Revision	Changes
21-Jul-2017	1	Initial release.
21-Sep-2017	2	Updated document status to Production data. Added availability FW boot loader in whole document. Minor modifications throughout document.