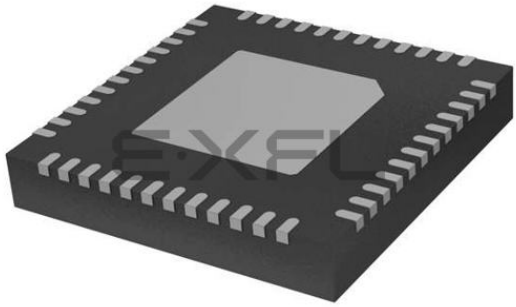

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

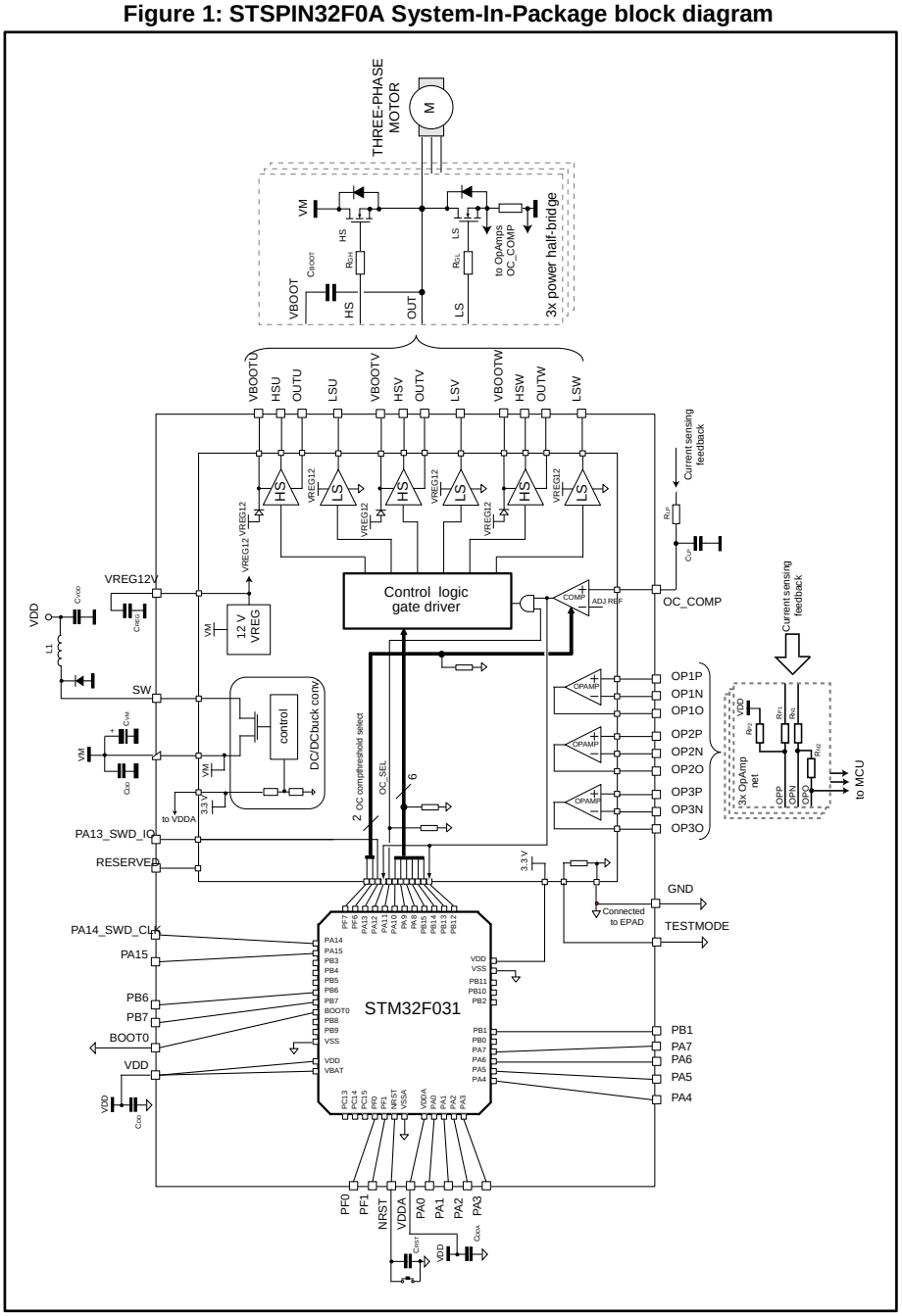
Details	
Product Status	Active
Applications	BLDC Controller
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (32kB)
Controller Series	STM32F031x6x7
RAM Size	4K x 8
Interface	I²C, SPI, UART/USART
Number of I/O	16
Voltage - Supply	6.7V ~ 45V
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-VFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stspin32f0atr

Contents

List of figures

2 Block diagrams

Figure 1: STSPIN32F0A System-In-Package block diagram



3 Electrical data

3.1 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 1: "Absolute maximum ratings"* may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 1: Absolute maximum ratings

Symbol	Parameter	Test condition	Value	Unit
V_M	Power supply voltage	-	-0.3 to 48	V
V_{REG12}	Linear regulator output and gate driver supply voltage	VREG12 shorted to VM	15	V
V_{OPP}	Op amp positive input voltage	-	-0.2 to V_{DD} + 0.2	V
V_{OPN}	Op amp negative input voltage	-	-0.2 to V_{DD} + 0.2	V
V_{CP}	Comparator input voltage	-	-2 to 2	V
V_{HS}	High-side gate output voltage	-	V_{OUT} - 0.3 to V_{BOOT} + 0.3	V
V_{LS}	Low-side gate output voltage	-	-0.3 to V_{REG12} + 0.3	V
V_{BOOT}	Bootstrap voltage	-	Max. (V_{OUT} - 0.3 or -0.3) to min. ('V_{OUT} + V_{REG12} + 0.3' or 60)	V
V_{OUT}	Output voltage (OUTU, OUTV, OUTW)	-	-2 to V_M + 2	V
dV_{OUT}/dt	Output slew rate	-	± 10	V/ns
V_{IO}	MCU logic input voltage(1)	TTa type (1)	-0.3 to 4	V
		(1) FT, FTf type	-0.3 to V_{DD} + 4 (2)	
		BOOT0	0 to 9.0	
I_{IO}	MCU I/O output current	(1)	-25 to 25	mA
ΣI_{IO}	MCU I/O total output current	(1), (3)	-80 to 80	mA
V_{DD}	MCU digital supply voltage	(1)	-0.3 to 4	V
V_{DDA}	MCU analog supply voltage	(1)	-0.3 to 4	V
T_{stg}	Storage temperature	-	-55 to 150	°C
T_j	Operating junction temperature	-	-40 to 150	°C

Notes:

(1)See Table 15 Voltage characteristics in the STM32F031C6 datasheet (suffix 7 version).

(2)Valid only if the internal pull-up/pull-down resistors are disabled. If internal the pull-up or pull-down resistor is enabled, the maximum limit is 4 V.

(3)If the MCU supply voltage is provided by an integrated DC/DC regulator, the application current consumption is limited at $I_{DDA,max}$ value (see *Table 5: "Electrical characteristics"*).

3.2 ESD protections

Table 2: ESD protection ratings

Symbol	Parameter	Test condition	Class	Value	Unit
HBM	Human body model	Conforming to ANSI/ESDA/JEDEC JS-001-2014	H2	2	kV
CDM	Charge device model	Conforming to ANSI/ESDA/JEDEC JS-002-2014	C2	750	V

3.3 Recommended operating conditions

Table 3: Recommended operating conditions

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_M	Power supply voltage	-	6.7 (1)	-	45	V
dV_M/dt	Power supply voltage slope	V_M = 45 V	-	-	0.75	V/µs
V_{DDA}	DC/DC regulator output voltage	-	-	3.3	-	V
L_{SW}	Output inductance	-	-	22	-	µH
C_{DDA}	Output capacitance	-	47	-	-	µF
ESR_{DDA}	Output capacitor ESR	-	-	-	200	mΩ
V_{REG12}	Linear regulator output and gate driver supply voltage	13 < V_M < 45 V	-	12	-	V
		Shorted to VM	6.7(1)	-	15	
C_{REG}	Load capacitance	-	1	10	-	µF
ESR_{REG}	ESR load capacitance	-	-	-	1.2	Ω
V_{BO}	Floating supply voltage (2)	-	-	V_{REG12} - 1	15	V
V_{CP}	Comparator input voltage	-	0	-	1	V
T_j	Operating junction temperature	Analog IC	-40	-	125	°C
		MCU (3)	-40	-	125	°C

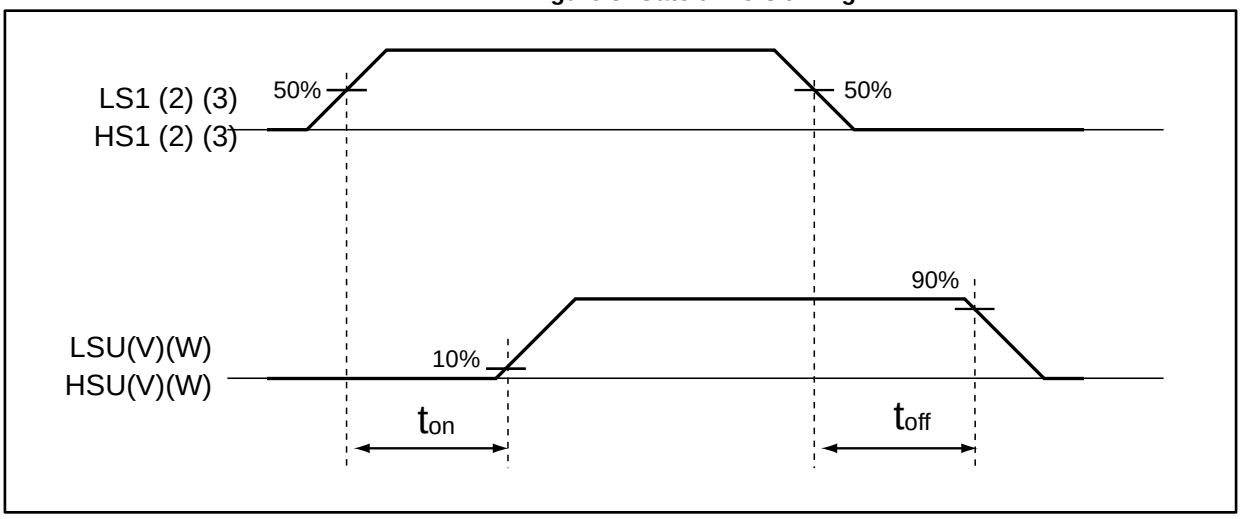
Notes:

(1) UVLO threshold V_{MOn_max}.

(2) $V_{BO} = V_{BOOT} - V_{OUT}$.

(3) See the STM32F031C6 datasheet (suffix 7 version).

Figure 3: Gate drivers timing



No.	Name	Type	Function
47	OP3O	Analog out	Op amp 3 output
48	VDD	Power	MCU digital power supply
	EPAD	Power	Internally connected to ground

Table 7: STSPIN32F0A MCU pad mapping

MCU pad	Type	Analog IC pad	Alternate and additional functions
PF0	I/O - FT	-	OSC_IN
PF1	I/O - FT	-	OSC_OUT
NRST	I/O - RST	-	Device reset input / internal reset output (active low)
VDDA	S	VDD_3V3	Analog power supply voltage
PA0	I/O - TTa	-	TIM2_CH1_ETR, USART1_CTS ADC_IN0, RTC_TAMP2, WKUP1
PA1	I/O - TTa	-	TIM2_CH2, EVENTOUT, USART1_RTS ADC_IN1
PA2	I/O - TTa	-	TIM2_CH3, USART1_TX ADC_IN2
PA3	I/O - TTa	-	TIM2_CH4, USART1_RX ADC_IN3
PA4	I/O - TTa	-	SPI1_NSS, I2S1_WS, TIM14_CH1, USART1_CK ADC_IN4
PA5	I/O - TTa	-	SPI1_SCK, I2S1_CK, TIM2_CH1_ETR ADC_IN5
PA6	I/O - TTa	-	SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, EVENTOUT ADC_IN6
PB1	I/O - TTa	-	TIM3_CH4, TIM14_CH1, TIM1_CH3N ADC_IN9
PA7	I/O - TTa	-	SPI1_MOSI, I2S1_SD, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, EVENTOUT ADC_IN7
PB12	I/O - FT	OC_COMP_INT	TIM1_BKIN (1)
PB13	I/O - FT	LS1	TIM1_CH1N(1)
PB14	I/O - FT	LS2	TIM1_CH2N(1)
PB15	I/O - FT	LS3	TIM1_CH3N(1)
PA8	I/O - FT	HS1	TIM1_CH1(1)

Pinout name	Pad name	Type	Function
-	LS3	Digital in	Low-side input driver W
-	OC_SEL	Digital in	OC protection selection
-	OC_COMP_INT2	Digital out	OC comparator output
-	SWD_IO_INT	Digital in	System debug data (connected to the output through the analog IC)
-	OC_TH_STBY1	Digital in	Overcurrent threshold selection and standby input 1
-	OC_TH_STBY2	Digital in	Overcurrent threshold selection and standby input 2

6 Device description

The STSPIN32F0A is a System-In-Package providing an integrated solution suitable for driving the three-phase BLDC motors. The device will be developed in the BCD8s (0.18 µm) technology.

6.1 UVLO and thermal protections

Table 9: "UVLO and OT protection management" summarizes the UVLO and OT protection management.

Table 9: UVLO and OT protection management

Block	V_M UVLO	V_{DD} UVLO	V_{REG12} UVLO	V_{BOOT} UVLO	Lin. Reg OT	DC/DC Reg OT
DC/DC regulator	-	-	-	-	-	OFF
Linear regulator	OFF	OFF	-	-	OFF	-
Op amps and OC comp	OFF	OFF	-	-	-	-
HSU, HSV, HSW output	LOW	LOW	LOW (1)	LOW(1), (2)	-	-
LSU, LSV, LSW output	LOW	LOW	LOW(1)	-	-	-

Notes:

(1)The N-channel of the gate driver is turned ON with all the available supply voltage, refer to *Figure 5: "Gate drivers' outputs characteristics in UVLO conditions"*.

(2)Only the high-side gate driver in which the UVLO condition is detected (e.g. UVLO on VBOOTU causes the HSU turning off).

Figure 5: Gate drivers' outputs characteristics in UVLO conditions

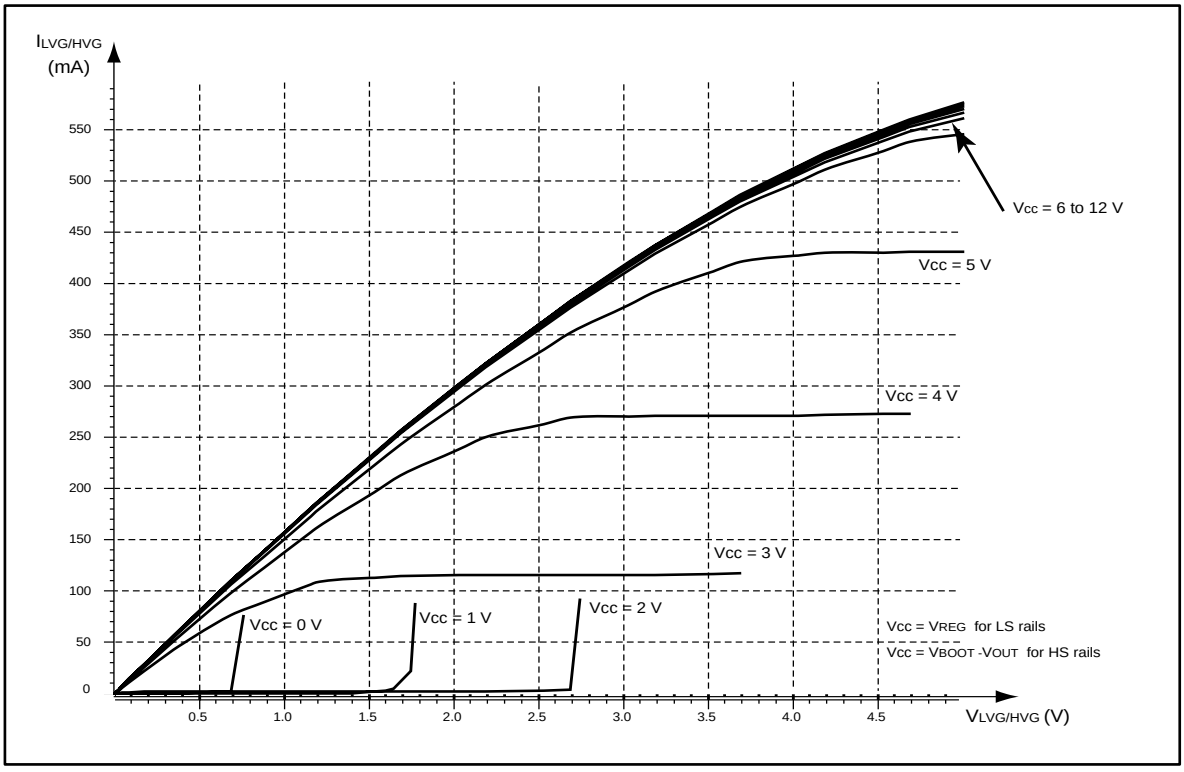
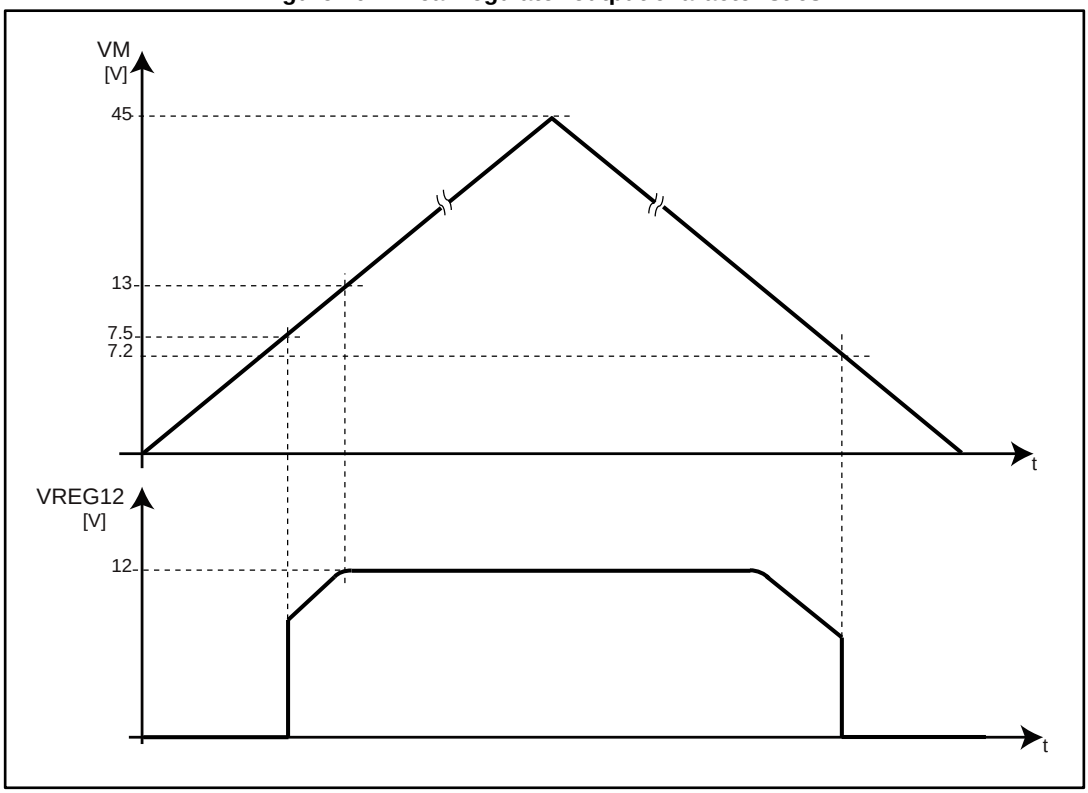


Figure 10: Linear regulator output characteristics



The linear regulator is designed to supply the internal circuitry only and must not be used to supply external components.

6.4 Standby mode

The device is forced into the standby mode to reduce power consumption forcing both the OC_TH_STBY1 and OC_TH_STBY2 analog IC inputs low (see *Table 12: "OC threshold values"*).

When the standby mode is set the analog IC is put into the low consumption mode after a t_{sleep} time, in particular:

- The linear regulator is switched off
- All the output drivers are forced low (external power switches turned off)
- Op amps and comparators disabled
- The DC/DC regulator remains operative.

When the device exits from the standby mode a set time is necessary to recover a proper value of the 12 V internal regulator. This set time is strictly dependent by the capacitor connected on the VREG12 pin and can be calculated with *Equation 1*.

Figure 12: HSE clock source timing diagram

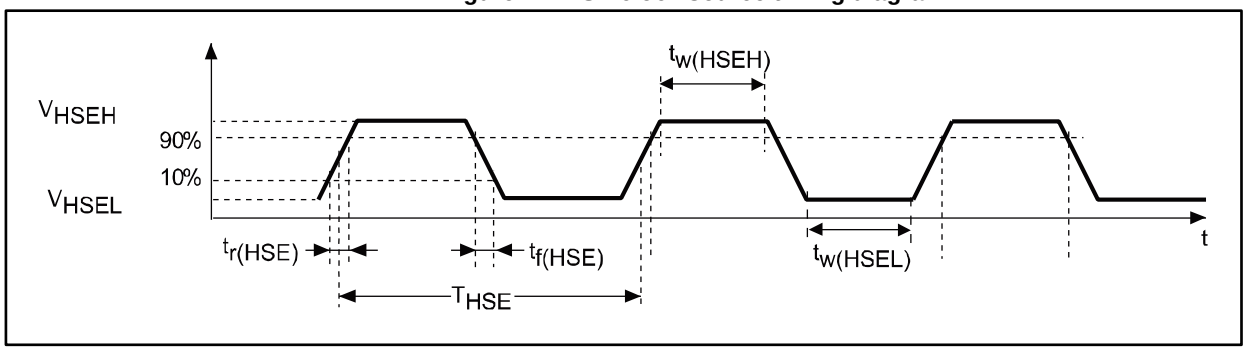
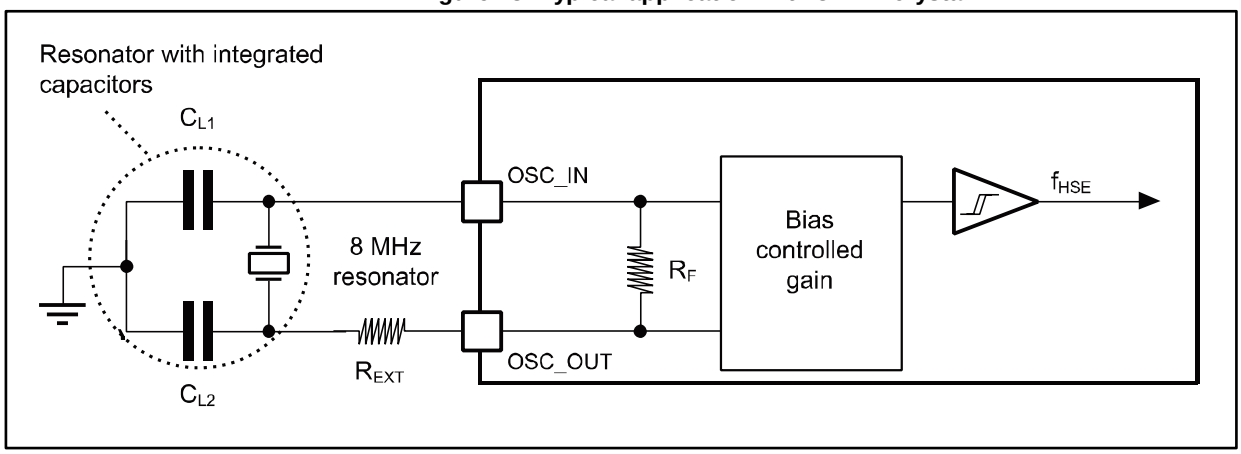


Figure 13: Typical application with 8 MHz crystal



In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The R_{EXT} value depends on the crystal characteristics (refer to the crystal resonator manufacturer for more details on them).

6.6.4 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted deadtimes.

This timer is used to generate the PWM signal for the three half-bridge gate drivers as shown in *Table 10: "TIM1 channel configuration"*.

Table 10: TIM1 channel configuration

MCU I/O	Analog IC input	TIM1 channel
PB13	LS1	TIM1_CH1N
PB14	LS2	TIM1_CH2N
PB15	LS3	TIM1_CH3N
PA8	HS1	TIM1_CH1
PA9	HS2	TIM1_CH2
PA10	HS3	TIM1_CH3

6.7 Test mode

A dedicated pin TESTMODE is available to enter into the test mode.

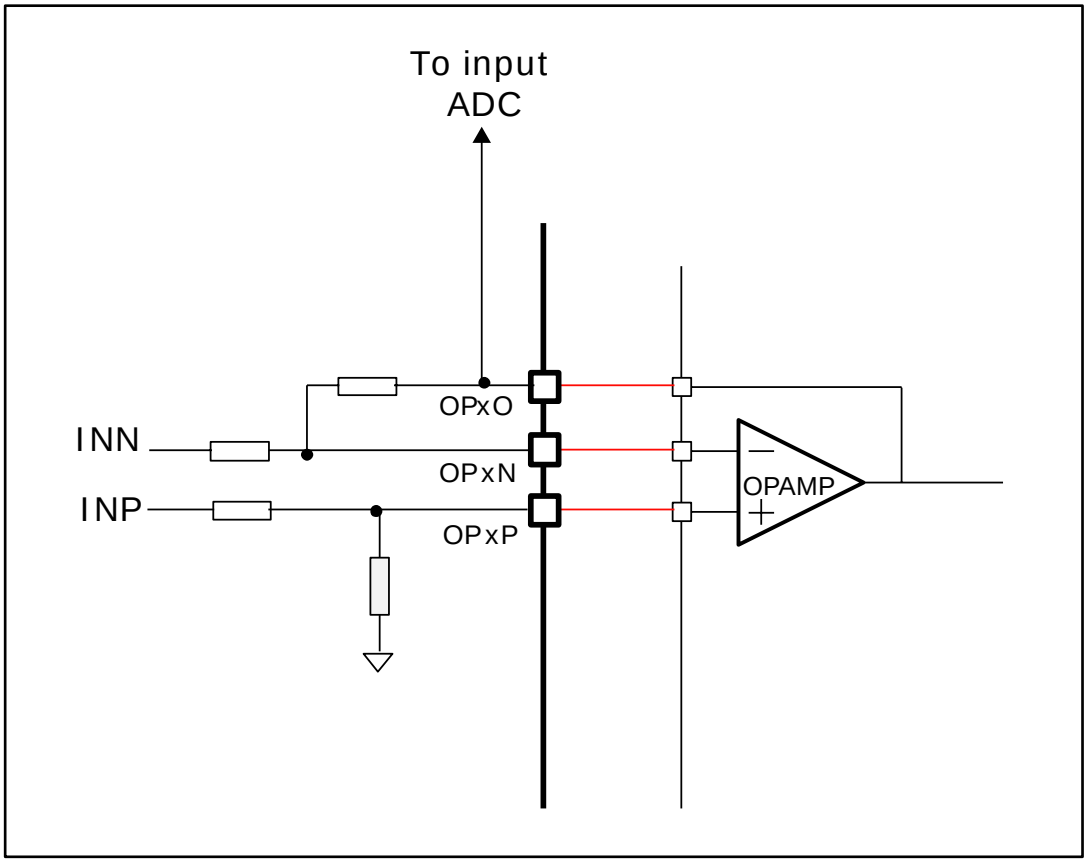
In the application, the TESTMODE pin should be shorted to GND in order not to enter the test mode inadvertently.

6.8 Operational amplifiers

The device integrates three rail-to-rail operational amplifiers suitable for signal conditioning, in particular for current sensing.

The operational amplifiers provide a rail-to-rail output stage with fast recovery in the saturation condition. The output stage saturation happens in linear applications when a high amplitude input signal occurs and causes the output of the operational amplifier to move outside its real capabilities.

Figure 14: Operational amplifiers



6.9 Comparator

A comparator is available to perform an overcurrent protection. The OC Comp pin can be connected to the shunt resistor to monitor the load current, the internal OC threshold can be set via MCU (PF6 and PF7 port, see *Table 12: "OC threshold values"*).

When an OC event is triggered, the OC comparator output signals the OC event to the PB12 and PA12 inputs of MCU (BKIN and ETR).

Depending on the status of the OC_SEL signal (see *Table 11: "OC protection selection"*) the OC event is acting directly on the control logic of the gate driver switching off all high-side gate outputs, and consequently the external high-side power switches.

Figure 15: Comparator

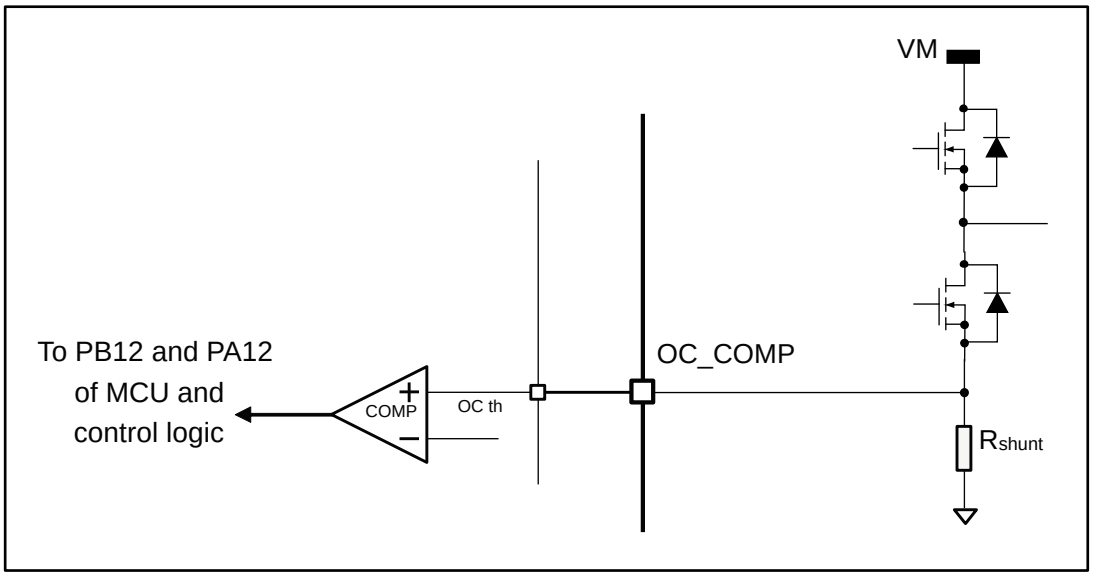


Table 11: OC protection selection

OC_SEL (PA11)	Function
0	OC comparator output signal is visible only to MCU (default)
1	OC comparator output signal is visible to MCU and also acts on gate driver control logic

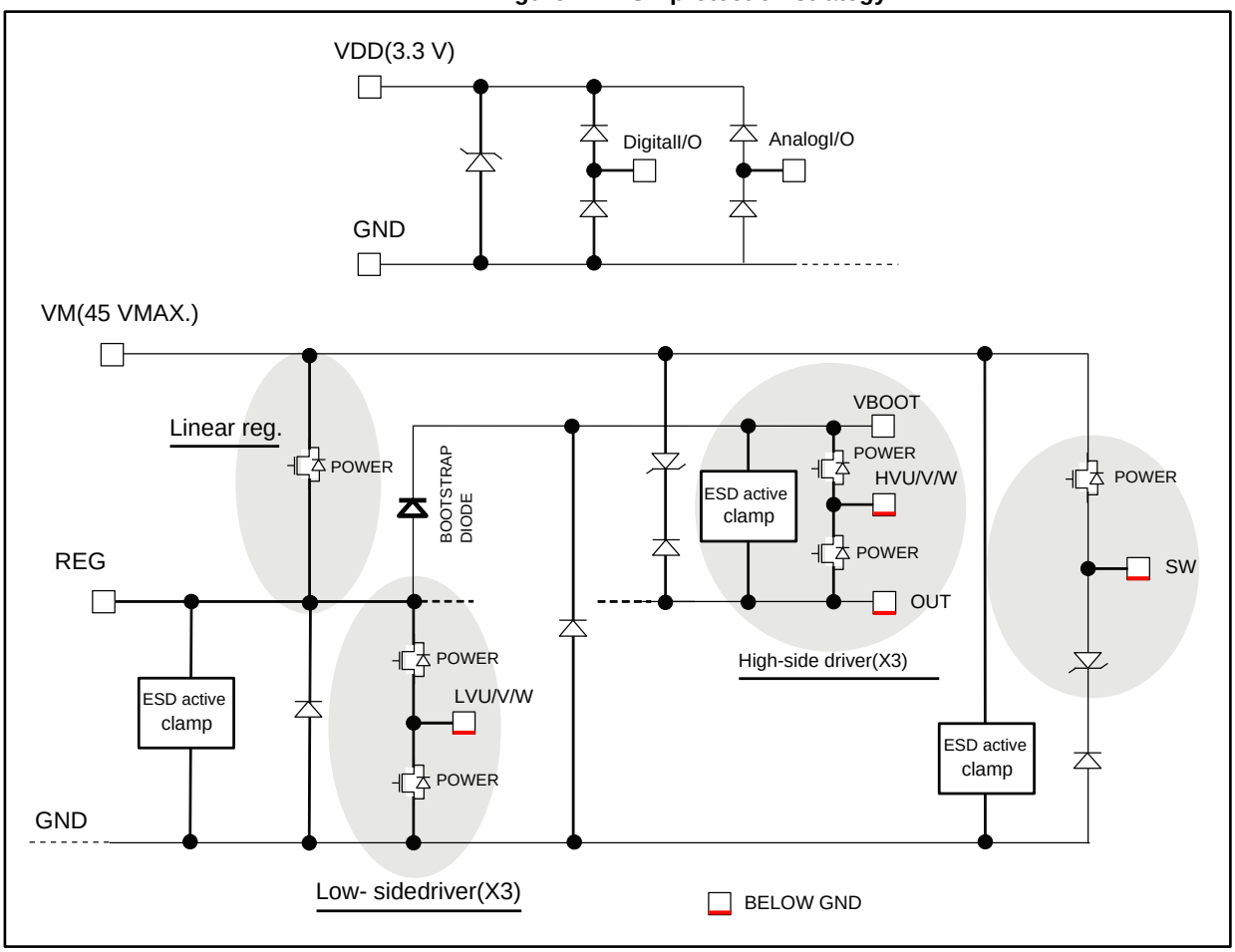
Table 12: OC threshold values

OC_TH_STBY2 (PF6)	OC_TH_STBY1 (PF7)	OC threshold [mV]	Note
0	0	N.A.	Standby mode (see *Section 6.4: "Standby mode"*)
0	1	100	-
1	0	250	-
1	1	500	-

When the overcurrent condition disappears, the latched overcurrent signal is released only after all the high-side outputs are kept low for at least $t_{OCrelease}$ time. (Refer to *Figure 16: "Driver logic overcurrent management signals"*).

6.10 ESD protection strategy

Figure 17: ESD protection strategy



7 Application example

Figure 18: "Application example" shows an application example using the STSPIN32F0A device to drive a three-phase motor with triple shunt configuration and field oriented control algorithm. The others features implemented are:

- VDD (3.3 V) power supply internally generated via DC/DC regulator
- VREG12 (12 V) power supply internally generated via LDO linear regulator
- USART serial interface (PB6 and PB7)
- Serial wire debug ports (PA13_SWD_IO, PA14_SWD_CLK)
- Ready and alarm lines (PF0, PF1)
- Reset dedicated pin
- Overcurrent protection using internal comparator
- Current sensing using internal operational amplifiers and ADCs (PA0, PA1, PA2)
- Bus voltage compensation using internal ADC (PA3)
- Application temperature monitoring using internal ADC (PA4)

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

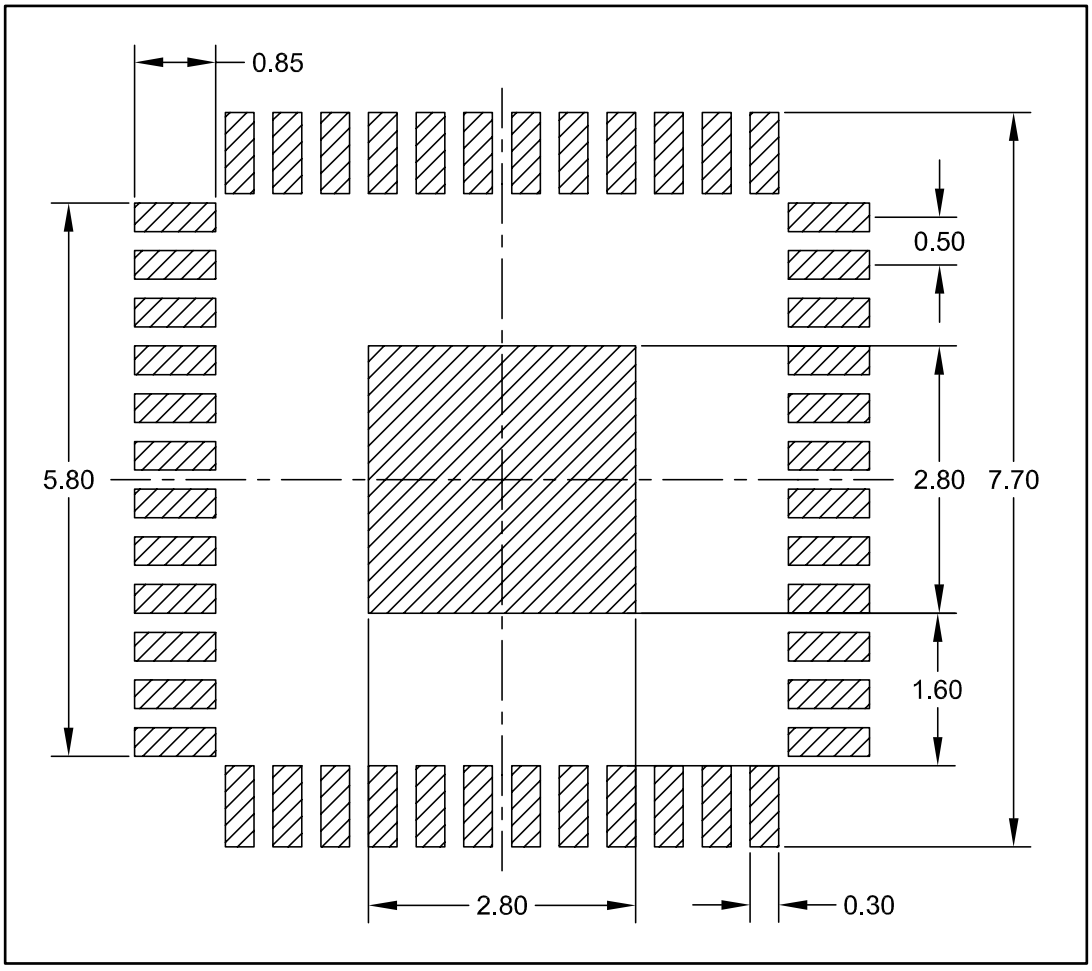
A customized VFQFPN48 7 x 7 package is proposed. A smaller EPAD, internally connected to the ground pin, is desired to place through holes on the bottom of the package.

Lead plating is Nickel/Palladium/Gold (Ni/Pd/Au).

Table 13: VFQFPN48 7 x 7 x 1.0 - 48L, pitch 0.5 - package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.90	0.95	1.00
A1	0.0	-	0.05
A2		0.75	
A3		0.203	
b	0.20	0.25	0.30
D	6.90	7.00	7.10
E	6.90	7.00	7.10
e		0.50	
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70
K		1.80	
L	0.30	0.40	0.50

Figure 20: VFQFPN48 7 x 7 x 1.0 - 48L, pitch 0.5 - suggested footprint



9 Ordering information

Table 14: Order codes

Order code	Package	Packaging
STSPIN32F0A	VFQFPN 7 x 7 x 1.0 - 48L	Tray
STSPIN32F0ATR	VFQFPN 7 x 7 x 1.0 - 48L	Tape and reel

10 Revision history

Table 15: Document revision history

Date	Revision	Changes
21-Jul-2017	1	Initial release.
21-Sep-2017	2	Updated document status to Production data. Added availability FW boot loader in whole document. Minor modifications throughout document.

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