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Details	
Product Status	Obsolete
Core Processor	-
Core Size	8/16-Bit
Speed	40MHz
Connectivity	UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (20x14)
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Name	Pin
a0	63
a1	62
a2	60
a3	59
a4	58
a5	57
a6	56
a7	55
a8	54
a9	53
a10	52
a11	51
a12	50
a13	49
a14	48
a15	47
a16	46
a17/pio7	45
a18/pio8	43
a19/pio9	42
ale	30
ad0	1
ad1	3
ad2	5
ad3	7
ad4	9
ad5	11
ad6	14
ad7	17
ao8	2
ao9	4
ao10	6
ao11	8
ao12	10

Name	Pin
ao13	13
ao14	16
ao15	18
ardy	30
clkouta	39
clkoutb	40
den_n/pio5	72
drq0/pio12	100
drq1/pio13	99
dt/r_n/pio4	71
gnd	12
gnd	35
gnd	41
gnd	64
gnd	65
gnd	87
gnd	93
hlda	67
hold	68
int0	79
int1/select_n	78
int2/inta0_n/pio31	77
int3/inta1_n/irq	76
int4/pio30	75
lcs_n/once0_n	81
mcs0_n/pio14	73
mcs1_n/pio15	74
mcs2_n/pio24	91
mcs3_n/rfsh_n/pio25	92
nmi	70
pcs0_n/pio16	89
pcs1_n/pio17	88
pcs2_n/pio18	86

Name	Pin
pcs3_n/pio19	85
pcs5_n/a1/pio3	83
pcs6_n/a2/pio2	82
rd_n	29
res_n	94
rfsh2_n/aden_n	27
rxd/pio28	22
s0_n	34
s1_n	33
s2_n	32
s6/lock_n/clkdiv2/pio29	19
sclk/pio20	26
sdata/pio21	23
sden0/pio22	25
sden1/pio23	24
srdy/pio6	69
tmrin0/pio11	98
tmrin1/pio0	95
tmrout0/pio10	97
tmrout1/pio1	96
txd/pio27	21
ucs_n/once1_n	80
uzi_n/pio26	20
V_{CC}	15
V_{CC}	38
V_{CC}	44
V_{CC}	61
V_{CC}	84
V_{CC}	90
wb_n	66
wr_n	28
x1	36
x2	37

2.2 Pin Descriptions

2.2.1 a19/pio9, a18/pio8, a17/pio7, a16–a0—Address Bus (synchronous outputs with tristate)

These pins are the system's source of non-multiplexed I/O or memory addresses and occur a half clkouta cycle before the multiplexed address/data bus (ad15–ad0 for the IA186EM or ao15–ao8 and ad7–ad0 for the IA188EM). The address bus is tristated during a bus hold or reset.

2.2.2 ad15–ad8 (IA186EM)—Address/data bus (level-sensitive synchronous inouts with tristate)

These pins are the system's source of time-multiplexed I/O or memory addresses and data. The address function of these pins can be disabled (see bhe_n/aden_n pin description). If the address function of these pins is enabled, the address will be present on this bus during t_1 of the bus cycle and data will be present during t_2, t_3, and t_4 of the same bus cycle.

If whb_n is not active, these pins are tristated during t_2, t_3, and t_4 of the bus cycle.

The address/data bus is tristated during a bus hold or reset.

These pins can be used to load the internal Reset Configuration register (RESCON, offset 0F6h) with configuration data during a power-on reset (POR).

2.2.3 ad7–ad0—Address/Data bus (level-sensitive synchronous inouts with tristate)

These pins are the system's source of time-multiplexed low-order byte of the addresses for I/O or memory and 8-bit data. The low-order address byte will be present on this bus during t_1 of the bus cycle and the 8-bit data will be present during t_2, t_3, and t_4 of the same bus cycle.

The address function of these pins can be disabled (see bhe_n/aden_n pin description).

If wlb_n (IA186EM) is not active, these pins are tristated during t_2, t_3, and t_4 of the bus cycle. The address/data bus is tristated during a bus hold or reset.

2.2.4 ao15–ao8 (IA188EM)—Address-only bus (level-sensitive synchronous outputs with tristate)

The address-only bus will contain valid high-order address bits during the bus cycle (t_1, t_2, t_3, and t_4) if the bus is enabled.

These pins are combined with ad7–ad0 to complete the multiplexed address bus and are tristated during a bus hold or reset condition.

2.2.21 lcs_n/once0_n—Lower Memory Chip Select (synchronous output with internal pull-up)/ONCE Mode Request (input)

The lcs_n pin provides an indication that a memory access is occurring to the lower memory block. The size of the Lower Memory Block and its base address are programmable, with the size adjustable up to 512 Kbytes. The lcs_n is held high during bus hold.

The once0_n pin (ONCE – ON Circuit Emulation) and its companion pin, once1_n, define the microcontroller mode during reset. These two pins are sampled on the rising edge of res_n and if both are asserted low the microcontroller starts in ONCE mode, else it starts normally. In ONCE mode, all pins are tristated and remain so until a subsequent reset. To prevent the microcontroller from entering ONCE mode inadvertently, this pin has a weak pull-up that is only present during reset. This pin is not tristated during bus hold.

2.2.22 mcs2_n—mcs0_n (no pio, pio15, pio 14)—Midrange Memory Chip Selects (synchronous outputs with internal pull-up)

The mcs2_n and mcs0_n pins provide an indication that a memory access is in progress to the second or third midrange memory block. The size of the Midrange Memory Block and its base address are programmable. The mcs2_n – mcs0_n are held high during bus hold and have weak pull-ups that are only present during reset.

2.2.23 mcs3_n/rfsh_n (pio25)—Midrange Memory Chip Select (synchronous output with internal pull-up)/Automatic Refresh (synchronous output)

The mcs3_n pin provides an indication that a memory access is in progress to the fourth region of the midrange memory block. The size of the Midrange Memory Block and its base address are programmable. The mcs3_n is held high during bus hold and has a weak pull-up that is present only during reset.

The rfsh_n signal is timed for auto refresh to PSRAM or DRAM devices. The refresh pulse is output only when the PSRAM or DRAM mode bit is set (EDRAM register Bit [15]). This pulse is of 1.5 clock-pulse duration with the rest of the refresh cycle made up of a deassertion period such that the overall refresh time is met. This pin is not tristated during a bus hold.

2.2.24 nmi—Nonmaskable Interrupt (synchronous edge-sensitive input)

Unlike int4 – int0, this is the highest priority interrupt signal and cannot be masked. Upon the assertion of this interrupt (transition from Low to High), program execution is transferred to the nonmaskable interrupt vector in the interrupt vector table and this interrupt is initiated at the next instruction boundary. For recognition to be assured, the nmi pin must be held high for at least a clkouta period so that the transition from low to high is latched and synchronized internally. The interrupt will begin at the next instruction boundary.

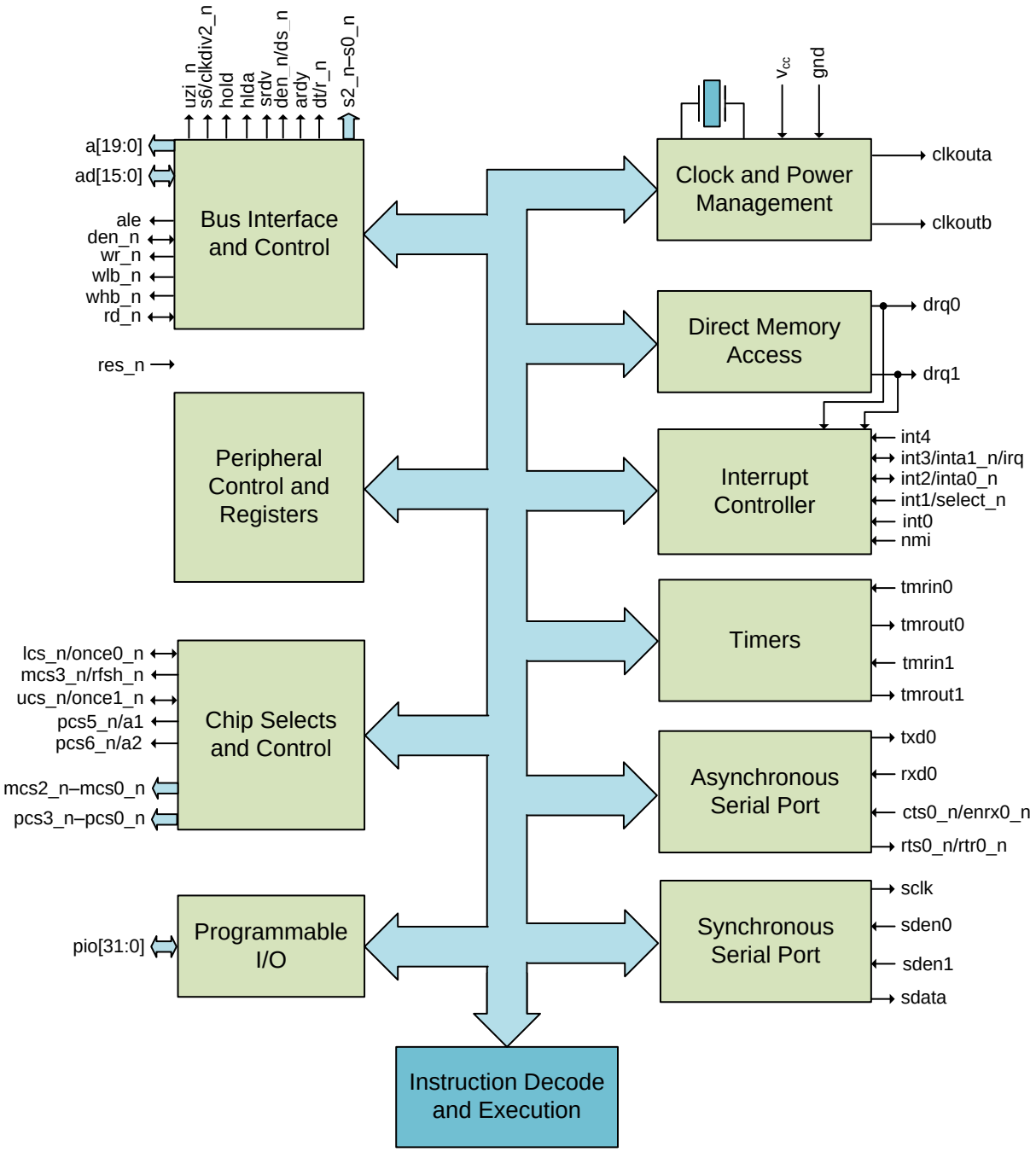

Figure 7. Functional Block Diagram

Note: See pin descriptions for pins that share other functions with PIO pins. Pins pwd, int5, int6, rts1_n/rtr1_n, and cts1_n/enrx1_n are multiplexed with int2_n/inta0_n, drq0_n, drq0_n, pcs3_n, and pcs2_n, respectively.

4.12 Low Memory Chip Select

The lcs_n chip-select is for lower memory. As the interrupt vector table is at the bottom of memory beginning at 00000h, this pin us usually used for control data memory. Unlike ucs_n, this pin is inactive on reset, but can be activated by any read or write to the LMCS register.

4.13 Midrange Memory Chip Selects

There are four midrange chip selects, mcs3_n–mcs0_n, which may be used in a user-located memory block. With some exceptions, the base address of the memory block may be located anywhere in the 1-Mbyte memory address space (those used by the ucs_n and lcs_n chip selects, as well as the pcs6_n, pcs5_n, and pcs3_n–pcs0_n, are excluded). If the pcs_n chip selects are mapped to I/O space, then the MCS address range can overlap the PCS address range.

Both the Midrange Memory Chip Select (MMCS) register and the MCS and PCS auxiliary (MPCS) registers are used to program the four midrange chip selects. The MPCS register is used to configure the block size, whereas the MMCS register configures the base address, the ready condition, and the wait states of the memory block accessed by the mcs_n pin. The chip selects (mcs3_n–mcs0_n) are activated by performing a read or write operation of the MMCS and MPCS registers. The assertion of the MCS outputs occurs with the same timing as the multiplexed AD address bus (ad15–ad0 on the IA186EM or ao15–ao8 and ad7–ad0 on the IA188EM). The a19–a0 may be used for address selection, but the timing will be delayed by a half clock cycle over the timing used for the ucs_n and lcs_n.

4.14 Peripheral Chip Selects

There are six peripheral chip selects (pcs6_n, pcs5_n, and pcs3_n–pcs0_n) that may be used within a user-defined memory or I/O block. The base address of this user-defined memory block can be located anywhere within the 1-Mbyte memory address space except for the spaces associated with the ucs_n, lcs_n, and mcs_n chip selects. Or it may be programmed to the 64 Kbyte I/O space. The pcs4_n is not available.

Both the Peripheral Chip Select (PACS) register and the MCS and PCS Auxiliary register (MPCS) registers are used to program the six peripheral chip selects pcs6_n, pcs5_n, and pcs3_n–pcs0_n. The PACS register sets the base address, the ready condition, and the wait states for the pcs3_n–pcs0_n outputs.

The MPCS register configures pcs6_n and pcs5_n pins as either chip selects or address pins a1 and a2, respectively. When these pins are chip selects, the MPCS register also configures them as being active during memory or I/O bus cycles and during their ready and wait states.

None of the pcs_n pins are active at reset. Both the Peripheral Chip Select (PACS) register and the MCS and PCS Auxiliary register (MPCS) registers must be read or written to activate the pcs_n pins as chip selects.

Table 16. Peripheral Control Registers

Register Name	Offset
Peripheral Control Block Registers	
PCB Relocation Register	FEh
Reset Configuration Register	F6h
Processor Release Level Register	F4h
Power-Save Control Register	F0h
Enable RCU Register	E4h
Clock Prescaler Register	E2h
Memory Partition Register	E0h
DMA Registers	
DMA1 Control Register	DAh
DMA1 Transfer Count Register	D8h
DMA1 Destination Address High Register	D6h
DMA1 Destination Address Low Register	D4h
DMA1 Source Address High Register	D2h
DMA1 Source Address Low Register	D0h
DMA0 Control Register	CAh
DMA0 Transfer Count Register	C8h
DMA0 Destination Address High Register	C6h
DMA0 Destination Address Low Register	C4h
DMA0 Source Address High Register	C2h
DMA0 Source Address Low Register	C0h
Chip-Select Registers	
pcs_n and mcs_n Auxiliary Register	A8h
Mid-Range Memory Chip-Select Register	A6h
Peripheral Chip-Select Register	A4h
Low-Memory Chip-Select Register	A2h
Upper-Memory Chip-Select Register	A0h
Asynchronous Serial Port Register	
Serial Port Baud Rate Divisor Register	88h
Serial Port Receive Register	86h
Serial Port Transmit Register	84h
Serial Port Status Register	82h
Serial Port Control Register	80h
PIO Registers	
PIO Data 1 Register	7Ah
PIO Direction 1 Register	78h
PIO Mode 1 Register	76h
PIO Data 0 Register	74h
PIO Direction 0 Register	72h
PIO Mode 0 Register	70h

Register Name	Offset
Timer Registers	
Timer 2 Mode and Control Register	66h
Timer 2 Max Count Compare A Register	62h
Timer 2 Count Register	60h
Timer 1 Mode and Control Register	5Eh
Timer 1 Max Count Compare B Register	5Ch
Timer 1 Max Count Compare A Register	5Ah
Timer 1 Count Register	58h
Timer 0 Mode and Control Register	56h
Timer 0 Max Count Compare B Register	54h
Timer 0 Max Count Compare A Register	52h
Timer 0 Count Register	50h
Interrupt Registers	
Serial Port 0 Interrupt Control Register	44h
Watchdog Timer Control Register	42h
INT4 Interrupt Control Register	40h
INT3 Interrupt Control Register	3Eh
INT2 Interrupt Control Register	3Ch
INT1 Interrupt Control Register	3Ah
INT0 Interrupt Control Register	38h
DMA1 Interrupt Control Register	36h
DMA0 Interrupt Control Register	34h
Timer Interrupt Control Register	32h
Interrupt Status Register	30h
Interrupt Request Register	2Eh
Interrupt In-Service Register	2Ch
Interrupt Priority Mask Register	2Ah
Interrupt Mask Register	28h
Interrupt Poll Status Register	26h
Interrupt Poll Register	24h
End-of-Interrupt (EOI) Register	22h
Interrupt Vector Register	20h
Serial Port 1 Registers	
Synchronous Serial Receive Register	18h
Synchronous Serial Transmit 0 Register	16h
Synchronous Serial Transmit 1 Register	14h
Synchronous Serial Enable Register	12h
Synchronous Serial Status Register	10h

5.1.1 RELREG (0feh)

The Peripheral Control Block RELocation REGister maps the entire Peripheral Control Block Register Bank to either I/O or memory space. In addition, RELREG contains a bit that places the interrupt controller in either master or slave mode. The RELREG contains 20ffh at reset (see Table 17).

Table 17. Peripheral Control Block Relocation Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	S/Mn	Reserved	IO/Mn	RA19– RA8											

- Bit [15]—Reserved.
- Bit [14]—S/Mn → When set to 1, this bit places the interrupt controller into slave mode. When 0, it is in master mode.
- Bit [13]—Reserved.
- Bit [12]—IO/Mn → When set to 1, the Peripheral Control Block is mapped into memory space. When 0, this bit maps the Peripheral Control Block Register Bank into IO space.
- Bits [11–0]—RA19–RA8 → Sets the base address (upper 12 bits) of the Peripheral Control Block Register Bank. RA7–RA0 default to 0. When Bit [12] (IO/Mn) is set to 1, RA19–RA16 are ignored.

5.1.2 RESCON (0f6h)

The RESet CONfiguration Register latches user-defined information present at specified pins at the rising edge of reset. The contents of this register are read-only and remain valid until the next reset. The RESCON contains user-defined information at reset (see Table 18).

Table 18. Reset Configuration Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RC15–RC0															

- Bits [15–0]—RC15–RC0 → At the rising edge of reset, the values of specified pins (ad15–ad0 for the IA186EM and ao15–ao8 and ad7–ad0 for the IA188EM) are latched into this register.

5.1.3 PRL (0f4h)

The Processor Release Level Register contains a code corresponding to the latest processor production release. The PRL is a Read-Only Register. The PRL contains 0400h (see Table 19).

- Bit [5]—P → Relative Priority. When set to 1, selects high priority for this channel relative to the other channel during simultaneous transfers.
- Bit [4]—TDRQ → Timer 2 Synchronization. When set to 1, enables DMA requests from Timer 2. When 0, disables them.
- Bit [3]—Reserved.
- Bit [2]—CHG → Change Start Bit. This bit must be set to 1 to allow modification of the ST bit during a write. During a write, when CHG is set to 0, ST is not changed when writing the control word. The result of reading this bit is always 0.
- Bit [1]—ST → Start/Stop DMA Channel. When set to 1, the DMA channel is started. The CHG bit must be set to 1 for this bit to be modified and only during the same register write. A processor reset causes this bit to be set to 0.
- Bit [0]—Bn/W → Byte/Word Select. When set to 1, word transfers are selected. When 0, byte transfers are selected.

Note: Word transfers are not supported if the chip selects are programmed for 8-bit transfers. The IA188EM does not support word transfers

5.1.9 D1TC (0d8h) and D0TC (0c8h)

DMA Transfer Count Registers. The DMA Transfer Count registers are maintained by each DMA channel. They are decremented after each DMA cycle. The state of the TC bit in the DMA control register has no influence on this activity. But, if unsynchronized transfers are programmed or if the TC bit in the DMA control word is set, DMA activity ceases when the transfer count register reaches 0. The D0TC and D1TC registers are undefined at reset (see Table 25).

Table 25. DMA Transfer Count Registers

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC15–TC0															

- Bits [15–0]—TC15–TC0 → DMA Transfer Count contains the transfer count for the respective DMA channel. Its value is decremented after each transfer.

5.1.10 D1DSTH (0d6h) and D0DSTH (0c6h)

The DMA DeSTination Address High Register. The 20-bit destination address consists of these 4 bits combined with the 16 bits of the respective Destination Address Low Register. A DMA transfer requires that two complete 16-bit registers (high and low registers) be used for both the source and destination addresses of each DMA channel involved. These four registers must be

these registers must be adjusted to reflect the new processor clock frequency if power-save mode is in effect. The baud rate divisor may be calculated from:

BAUDDIV = (Processor Frequency/(32 x baud rate)) -1 (Equation 1)

By setting the BAUDDIV to 0000h, the maximum baud rate of 1/32 of the internal processor frequency clock is set. Setting BAUDDIV to 129 (81h) provides a baud rate of 9600 at 40 MHz. The baud rate tolerance is +4.6% to –1.9% with respect to the actual serial port baud rate, not the target baud rate (see Table 35).

Table 35. Baud Rates

Baud Rate	Divisor Based on CPU Clock Rate			
	20 MHz	25 MHz	33 MHz	40 MHz
300	4166	5208	6875	8333
600	2083	2604	3437	4166
1200	1041	1302	1718	2083
2400	520	651	859	1041
4800	260	325	429	520
9600	130	162	214	260
14400	42	53	71	85
19200	31	39	53	64
625 Kbaud	0	NA	NA	1
781.25 Kbaud	NA	0	NA	NA
1.041 Mbaud	NA	NA	0	NA
1.25 Mbaud	NA	NA	NA	0

The value of the SPBAUD register at reset is undefined (see Table 36).

Table 36. Serial Port Baud Rate Divisor Registers

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAUDDIV															

- Bits [15–0]—BAUDDIV Baud Rate Divisor → Defines the divisor for the internal processor clock.

5.1.20 SPRD (086h)

Serial Port Receive Data Register. Data received over the serial port are stored in this register until read. The data are received initially by the receive shift register (no software access) permitting data to be received while the previous data are being read.

The RDR bit (Receive Data Ready) in the serial port status register indicates the status of the SPRD register. Setting the RDR bit to 1 indicates there is valid data in the receive register. The value of the SPRD register is undefined at reset (see Table 37).

- Bit [1]—RSIE Receive Status Interrupt Enable → When an exception occurs during data reception, an interrupt request is generated if enabled by this bit (RSIE = 1). Interrupt requests are made for the error conditions listed in the serial port status register (BRK, OER, PER, and FER). This bit is 0 at reset.

- Bit [0]—RMODE Receive Mode → When this bit is 1, the receive section of the serial port is enabled. When 0, it is disabled. This bit is 0 at reset.

5.1.24 PDATA1 (07ah) and PDATA0 (074h)

PIO DATA Registers. When a PIO pin is configured as an output, the value in the corresponding PIO data register bit is driven onto the pin. However, if the PIO pin is configured as an input, the value on the pin is put into the corresponding bit of the PIO data register. Table 41 lists the default states for the PIO pins.

Table 41. PIO Pin Assignments

PIO Number	Associated Pin Name	Power-On Reset Status
0	tmrin1	Input with pull-up
1	tmrout1	Input with pull-down
2	pcs6/a2	Input with pull-up
3	pcs5/a1	Input with pull-up
4	dt/r_n	Normal operation[a]
5	den_n/ds_n	Normal operation[a]
6	srdy	Normal operation[b]
7[c]	a17	Normal operation[a]
8[c]	a18	Normal operation[a]
9[c]	a19	Normal operation[a]
10	tmrout0	Input with pull-down
11	tmrin0	Input with pull-up
12	drq0	Input with pull-up
13	drq1	Input with pull-up
14	mcs0_n	Input with pull-up
15	mcs1_n	Input with pull-up
16	pcs0_n	Input with pull-up
17	pcs1_n	Input with pull-up
18	pcs2_n	Input with pull-up
19	pcs3_n	Input with pull-up
20	sclk	Input with pull-up
21	sdata	Input with pull-up
22	sden0	Input with pull-down
23	sden1	Input with pull-down

Table 63. Interrupt Status Register (Slave Mode)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DHLT	Reserved												TMR2–TMR0		

- Bit [15]—DHLT DMA Halt → DMA activity is halted when this bit is 1. It is set to 1 automatically when any non-maskable interrupt occurs and is cleared to 0 when an IRET instruction is executed.
- Bits [14–3]—Reserved.
- Bits [2–0]—TMR2–TMR0 Timer Interrupt Request → A pending interrupt request is indicated by the respective timer, when any of these bits is 1.

Note: The TMR bit in the REQST register is a logical OR of these timer interrupt requests.

5.1.42 REQST (02eh) (Master Mode)

Interrupt REQueST Register. This is a read-only register and such a read results in the status of the interrupt request bits presented to the interrupt controller. The REQST register is undefined on reset (see Table 64).

Table 64. Interrupt Request Register (Master Mode)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SP0	WD	I4–I0					D1–D0		Reserved	TMR

- Bits [15–11]—Reserved.
- Bit [10]—SP0 Serial Port 0 Interrupt Request → This is the serial port interrupt state and when enabled is the logical OR of all the serial port 0 interrupt sources, THRE, RDR, BRKI, FER, PER, and OER.
- Bit [9]—WD Watchdog Timer Interrupt Request → When it is a 1, the watchdog interrupt state indicates that an interrupt is pending.
- Bits [8–4]—I4–I0 Interrupt Requests → Setting any of these bits to 1 indicates that the relevant interrupt has a pending interrupt.
- Bits [3–2]—D1–D0 DMA Channel Interrupt Request → Setting either bit to 1 indicates that the respective DMA channel has a pending interrupt.
- Bit [1]—Reserved.

- Bits [3–2]—D1–D0 DMA Channel Interrupt In Service → The respective DMA channel is being serviced when this bit is set to 1.
- Bit [1]—Reserved.
- Bit [0]—TMR0 Timer Interrupt In Service → Timer 0 is being serviced when this bit is set to 1.

5.1.46 PRIMSK (02ah) (Master and Slave Mode)

PRIority MaSK Register. This register contains a value that sets the minimum priority level at which an interrupt can be generated by a maskable interrupt. The PRIMSK register contains 0007h on reset (see Table 68).

Table 68. Priority Mask Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													PRM2–PRM0		

- Bits [15–3]—Reserved → Set to 0.
- Bits [2–0]—PRM2–PRM0 Priority Field Mask → This three-bit field sets the minimum priority necessary for a maskable interrupt to generate an interrupt. Any maskable interrupt with a numerically higher value than that contained by these three bits is masked. The values of PR2–PR0 are shown below.

Values of PR2–PR0 by Priority

Priority	PR2–PR0
(High) 0	000b
1	001b
2	010b
3	011b
4	100b
5	101b
6	110b
(Low) 7	111b

Any unmasked interrupt can generate an interrupt if the priority level is set to 7. On the other hand, if the priority level is set to say 4, only unmasked interrupts with a priority of 0 to 5 are permitted to generate interrupts.

5.1.47 IMASK (028h) (Master Mode)

Interrupt MASK Register. The interrupt mask register is read/write. Setting a bit in this register has the same effect as setting the MSK bit in the corresponding interrupt control register. Setting

Table 81. Alphabetic Key to Waveform Parameters *(Continued)*

No.	Name	Description
7	tCLDV	Data Valid Delay
2	tCLDX	Data in Hold
71	tCLEV	clkouta Low to sden Valid
62	tCLHAV	hlda Valid Delay
82	tCLRF	clkouta High to rfsh_n Invalid
27	tCLRH	rd_n Inactive Delay
25	tCLRL	rd_n Active Delay
4	tCLSH	Status Inactive Delay
72	tCLSL	clkouta Low to sclk Low
48	tCLSRY	srdy Transition Hold Time
55	tCLTMV	Timer Output Delay
83	tCOAOB	clkouta to clkoutb Skew
20	tCVCTV	Control Active Delay 1
31	tCVCTX	Control Inactive Delay
21	tCVDEX	den_n Inactive Delay
17	tCXCSX	mcs_n/pcs_n Hold from Command Inactive
1	tDVCL	Data in Setup
75	tDVSH	Data Valid to SCLK High
19	tDXDL	den_n Inactive to dt/r_n Low
58	tHVCL	hld Setup Time
53	tINVCH	Peripheral Setup Time
54	tINVCL	drq Setup Time
86	tLCRF	lcs_n Inactive to rfsh_n Active Delay
23	tLHAV	ale High to Address Valid
10	tLHLL	ale Width
13	tLLAX	*ad* Address Hold from ALE Inactive
61	tLOCK	Maximum PLL Lock Time
84	tLRLL	lcs_n Precharge Pulse Width
57	tRESIN	res_n Setup Time
85	tRFCY	rfsh_n Cycle Time
29	tRHAV	rd_n Inactive to *ad* Address Active
59	tRHDX	rd_n High to Data Hold on *ad* Bus
28	tRHLH	rd_n Inactive to ale High
26	tRLRH	rd_n Pulse Width
77	tSHDX	sclk High to SPI Data Hold
78	tSLDV	sclk Low SPI Data Hold
47	tSRYCL	srdy Transition Setup Time
35	tWHDEX	wr_n Inactive to den_n Inactive
34	tWHDX	Data Hold after wr_n
33	tWHLH	wr_n Inactive to ale High
32	tWLWH	wr_n Pulse Width

Table 88. Interrupt Acknowledge Cycle Timing

No.	Name	Description	Min[a]	Max[a]
General Timing Requirements				
1	tDVCL	Data in Setup	10	–
2	tCLDX	Data in Hold	0	–
General Timing Responses				
3	tCHSV	Status Active Delay	0	6
4	tCLSH	Status Inactive Delay	0	6
7	tCLDV	Data Valid Delay	0	12
8	tCHDX	Status Hold Time	0	–
9	tCHLH	ale Active Delay	0	8
10	tLHLL	ale Width	tCLCH-5	–
11	tCHLL	ale Inactive Delay	0	8
12	tAVLL	*ad* Address Valid to ale Low	tCLCH	–
15	tCLAZ	*ad* Address Float Delay	0	12
19	tDXDL	den_n Inactive to dt/r_n Low	0	–
20	tCVCTV	Control Active Delay 1	0	10
21	tCVDEX	den_n Inactive Delay	0	9
22	tCHCTV	Control Active Delay 2	0	10
23	tLHAV	ale High to Address Valid	7.5	–
31	tCVCTX	Control Inactive Delay	0	10
68	tCHAV	clkouta High to *a* Address Valid	0	8

[a]In nanoseconds.

end of the timer interrupt routine being serviced, set the Interrupt Enable Bit in the Process Status Word to globally disable interrupts prior to clearing the timer interrupt being serviced and unmask the appropriate timer interrupts.

Errata No. 2

Problem: Lock up just after reset is released.

Description: Usually the first instruction is a long jump to the start of the user's code. In this case, the compiler apparently inserted a short jump instruction with zero displacement before the expected long jump instruction. The OEM device stuttered, but recovered to execute the long jump, while the device instruction pointer was corrupted, causing the lockup. In summary, a short jump with zero displacement is a corner case that does not work in the device.

Workaround: Do not use a short jump instruction with zero displacement.

Errata No. 3

Problem: Intermittent startup.

Description: Processor either came out of reset normally, or would go into a series of watchdog timeouts. The addition of 10K ohm pullups to the wr_n and rd_n outputs seemed to solve the issue. Further analysis of the OEM device shows the presence of undocumented pullups on these pins, which will pull them high when the reset condition tristates these pins. The device does not include internal pullups on these pins allowing these outputs to float during reset.

Workaround: Add 10K ohm pullups to wr_n and rd_n pins to guarantee proper logic levels at the end of reset.

Errata No. 4

Problem: Timer operation in continuous mode.

Description: The timers (Timer 0 and Timer 1) do not function per the specification when set in continuous mode with no external timer input stimulus to initiate/continue count.

Workaround: None.

Errata No. 5

Problem: DMA interrupt will not bring device out of halt state.