#### NXP USA Inc. - MK30DX64VLH7 Datasheet





#### Welcome to E-XFL.COM

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I <sup>2</sup> C, IrDA, SD, SPI, UART/USART
Peripherals	DMA, I <sup>2</sup> S, LCD, LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 22x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk30dx64vlh7

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



# 3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- Operating ratings apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

## 3.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	-0.3	1.2	V

# 3.5 Result of exceeding a rating





**Terminology and guidelines** 





# 3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

# 3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.



# 3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Тур.	Max.	Unit
I <sub>WP</sub>	Digital I/O weak pullup/pulldown current	10	70	130	μΑ

## 3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



# 3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T <sub>A</sub>	Ambient temperature	25	C°
V <sub>DD</sub>	3.3 V supply voltage	3.3	V



Symbol	Description	Min.	Max.	Unit
I <sub>DD</sub>	Digital supply current	—	185	mA
V <sub>DIO</sub>	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3	5.5	V
V <sub>AIO</sub>	Analog <sup>1</sup> , RESET, EXTAL, and XTAL input voltage	-0.3	V <sub>DD</sub> + 0.3	V
I <sub>D</sub>	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V <sub>DDA</sub>	Analog supply voltage	V <sub>DD</sub> – 0.3	V <sub>DD</sub> + 0.3	V
V <sub>BAT</sub>	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

# 5 General

## 5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is  $V_{IL} + (V_{IH} - V_{IL})/2$ .

#### Figure 1. Input signal measurement reference

All digital I/O switching characteristics assume:

- 1. output pins
  - have  $C_L=30$  pF loads,
  - are configured for fast slew rate (PORTx\_PCRn[SRE]=0), and
  - are configured for high drive strength (PORTx\_PCRn[DSE]=1)
- 2. input pins
  - have their passive filter disabled (PORTx\_PCRn[PFE]=0)

## 5.2 Nonswitching electrical specifications





### 5.2.1 Voltage and current operating requirements Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>DD</sub>	Supply voltage	1.71	3.6	V	
V <sub>DDA</sub>	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V <sub>DD</sub> -to-V <sub>DDA</sub> differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	V <sub>SS</sub> -to-V <sub>SSA</sub> differential voltage	-0.1	0.1	V	
V <sub>BAT</sub>	RTC battery supply voltage	1.71	3.6	V	
V <sub>IH</sub>	Input high voltage				
	• $2.7 \text{ V} \le \text{V}_{\text{DD}} \le 3.6 \text{ V}$	$0.7 \times V_{DD}$	_	V	
	• $1.7 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}$	$0.75 \times V_{DD}$	_	V	
V <sub>IL</sub>	Input low voltage				
	• 2.7 V $\leq$ V <sub>DD</sub> $\leq$ 3.6 V	—	$0.35 \times V_{DD}$	V	
	• $1.7 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}$	—	$0.3 \times V_{DD}$	V	
V <sub>HYS</sub>	Input hysteresis	$0.06 \times V_{DD}$	_	V	
I <sub>ICDIO</sub>	Digital pin negative DC injection current — single pin				1
	• V <sub>IN</sub> < V <sub>SS</sub> -0.3V	-5	_	mA	
I <sub>ICAIO</sub>	Analog <sup>2</sup> , EXTAL, and XTAL pin DC injection current —				3
	single pin			mA	
	<ul> <li>V<sub>IN</sub> &lt; V<sub>SS</sub>-0.3V (Negative current injection)</li> </ul>	-5	_		
	• V <sub>IN</sub> > V <sub>DD</sub> +0.3V (Positive current injection)	—	+5		
I <sub>ICcont</sub>	Contiguous pin DC injection current —regional limit,				
	positive injection currents of 16 contiguous pins				
	Negative current injection	-25	_	mA	
	Positive current injection	—	+25		
V <sub>RAM</sub>	V <sub>DD</sub> voltage required to retain RAM	1.2		V	
V <sub>RFVBAT</sub>	$V_{\text{BAT}}$ voltage required to retain the VBAT register file	V <sub>POR_VBAT</sub>	_	V	

- 1. All 5 V tolerant digital I/O pins are internally clamped to  $V_{SS}$  through a ESD protection diode. There is no diode connection to  $V_{DD}$ . If  $V_{IN}$  greater than  $V_{DIO\_MIN}$  (= $V_{SS}$ -0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R=( $V_{DIO\_MIN}$ - $V_{IN}$ )/II<sub>IC</sub>.
- 2. Analog pins are defined as pins that do not have an associated general purpose I/O port function.
- 3. All analog pins are internally clamped to  $V_{SS}$  and  $V_{DD}$  through ESD protection diodes. If  $V_{IN}$  is greater than  $V_{AIO\_MIN}$  (= $V_{SS}$ -0.3V) and  $V_{IN}$  is less than  $V_{AIO\_MAX}$ (= $V_{DD}$ +0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If these limits cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R=( $V_{AIO\_MIN}$ - $V_{IN}$ )/II<sub>IC</sub>I. The positive injection current limiting resistor is calculated as R=( $V_{AIO\_MIN}$ - $V_{IN}$ )/II<sub>IC</sub>I. The positive injection current limiting resistor is calculated as R=( $V_{IN}$ - $V_{AIO\_MAX}$ )/II<sub>IC</sub>I. Select the larger of these two calculated resistances.



5.2.3	Voltage and current operating behaviors			
	Table 4. Voltage and current operating behavior			

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>OH</sub>	Output high voltage — high drive strength				
	• 2.7 V $\leq$ V <sub>DD</sub> $\leq$ 3.6 V, I <sub>OH</sub> = -9mA	V <sub>DD</sub> – 0.5	_	V	
	• $1.71 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}, \text{ I}_{\text{OH}} = -3\text{mA}$	V <sub>DD</sub> – 0.5	_	V	
	Output high voltage — low drive strength				
	• 2.7 V $\leq$ V <sub>DD</sub> $\leq$ 3.6 V, I <sub>OH</sub> = -2mA	V <sub>DD</sub> – 0.5	_	V	
	• $1.71 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}, \text{ I}_{\text{OH}} = -0.6 \text{mA}$	V <sub>DD</sub> – 0.5	_	V	
I <sub>OHT</sub>	Output high current total for all ports	_	100	mA	
V <sub>OL</sub>	Output low voltage — high drive strength				
	• 2.7 V $\leq$ V <sub>DD</sub> $\leq$ 3.6 V, I <sub>OL</sub> = 9mA	_	0.5	V	
	• $1.71 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}, \text{ I}_{\text{OL}} = 3\text{mA}$	—	0.5	V	
	Output low voltage — low drive strength				
	• 2.7 V $\leq$ V <sub>DD</sub> $\leq$ 3.6 V, I <sub>OL</sub> = 2mA	_	0.5	V	
	• $1.71 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}, \text{ I}_{\text{OL}} = 0.6 \text{mA}$	_	0.5	V	
I <sub>OLT</sub>	Output low current total for all ports	_	100	mA	
I <sub>IN</sub>	Input leakage current (per pin) for full temperature range	-	1	μA	1
l <sub>IN</sub>	Input leakage current (per pin) at 25°C	_	0.025	μA	1
I <sub>OZ</sub>	Hi-Z (off-state) leakage current (per pin)	_	1	μA	
R <sub>PU</sub>	Internal pullup resistors	20	50	kΩ	2
R <sub>PD</sub>	Internal pulldown resistors	20	50	kΩ	3

1. Measured at VDD=3.6V

2. Measured at V<sub>DD</sub> supply voltage = V<sub>DD</sub> min and Vinput = V<sub>SS</sub>

3. Measured at  $V_{\text{DD}}$  supply voltage =  $V_{\text{DD}}$  min and Vinput =  $V_{\text{DD}}$ 

## 5.2.4 Power mode transition operating behaviors

All specifications except  $t_{POR}$ , and VLLSx $\rightarrow$ RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 72 MHz
- Bus clock = 36 MHz
- Flash clock = 24 MHz



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I <sub>DD_VLPW</sub>	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	_	0.61	_	mA	8
I <sub>DD_STOP</sub>	Stop mode current at 3.0 V					
	• @ -40 to 25°C	—	0.35	0.567	mA	
	• @ 70°C	—	0.384	0.793	mA	
	• @ 105°C	—	0.628	1.2	mA	
I <sub>DD_VLPS</sub>	Very-low-power stop mode current at 3.0 V					
	• @ –40 to 25°C	—	5.9	32.7	μA	
	• @ 70°C	—	26.1	59.8	μA	
	• @ 105°C	—	98.1	188	μA	
I <sub>DD_LLS</sub>	Low leakage stop mode current at 3.0 V					9
	• @ -40 to 25°C	—	2.6	8.6	μA	
	• @ 70°C	—	10.3	29.1	μA	
	• @ 105°C	—	42.5	92.5	μA	
I <sub>DD_VLLS3</sub>	Very low-leakage stop mode 3 current at 3.0 V					9
	• @ –40 to 25°C	—	1.9	5.8	μA	
	• @ 70°C	—	6.9	12.1	μA	
	• @ 105°C	—	28.1	41.9	μA	
I <sub>DD_VLLS2</sub>	Very low-leakage stop mode 2 current at 3.0 V					
	• @ –40 to 25°C	—	1.59	5.5	μA	
	• @ 70°C	—	4.3	9.5	μA	
	• @ 105°C	—	17.5	34	μA	
I <sub>DD_VLLS1</sub>	Very low-leakage stop mode 1 current at 3.0 V					
	• @ –40 to 25°C	—	1.47	5.4	μA	
	• @ 70°C	—	2.97	8.1	μA	
	• @ 105°C	—	12.41	32	μA	
I <sub>DD_VBAT</sub>	Average current with RTC and 32kHz disabled at 3.0 V					
	• @ -40 to 25°C		0.19	0.22	uА	
	• @ 70°C		0.49	0.64	uA	
	• @ 105°C	_	2.2	3.2	μΑ	

## Table 6. Power consumption operating behaviors (continued)

Table continues on the next page ...





Figure 2. Run mode supply current vs. core frequency





### Figure 3. VLPR mode supply current vs. core frequency

## 5.2.6 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

- 1. Go to www.freescale.com.
- 2. Perform a keyword search for "EMC design."

## 5.2.7 Capacitance attributes

Table 7. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C <sub>IN_A</sub>	Input capacitance: analog pins	—	7	pF
C <sub>IN_D</sub>	Input capacitance: digital pins		7	pF

#### K30 Sub-Family Data Sheet, Rev. 3, 11/2012.



Symbol	Description	Min.	Max.	Unit	Notes
	Mode select (EZP_CS) hold time after reset deassertion	2	_	Bus clock cycles	
	Port rise and fall time (high drive strength)				4
	Slew disabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	12	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	6	ns	
	Slew enabled				
	• $1.71 \le V_{DD} \le 2.7V$	_	36	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	24	ns	
	Port rise and fall time (low drive strength)				5
	Slew disabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	12	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	6	ns	
	Slew enabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	36	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	24	ns	
1					

#### Table 9. General switching specifications (continued)

- 1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
- 2. The greater synchronous and asynchronous timing must be met.
- 3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
- 4. 75pF load
- 5. 15pF load

# 5.4 Thermal specifications

## 5.4.1 Thermal operating requirements

#### Table 10. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
TJ	Die junction temperature	-40	125	°C
T <sub>A</sub>	Ambient temperature	-40	105	°C





Figure 8. Test Access Port timing





# 6.2 System modules

There are no specifications necessary for the device's system modules.

# 6.3 Clock modules



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V <sub>DD</sub>	Supply voltage	1.71	—	3.6	V	
I <sub>DDOSC</sub>	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	_	μA	
	• 8 MHz (RANGE=01)	—	300	_	μA	
	• 16 MHz	—	950	_	μA	
	• 24 MHz	—	1.2	_	mA	
	• 32 MHz	—	1.5	_	mA	
IDDOSC	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	_	μA	
	• 4 MHz	—	400	_	μA	
	• 8 MHz (RANGE=01)	—	500	_	μA	
	• 16 MHz	—	2.5	_	mA	
	• 24 MHz	—	3	_	mA	
	• 32 MHz	—	4	_	mA	
C <sub>x</sub>	EXTAL load capacitance					2, 3
Cy	XTAL load capacitance	_	—	—		2, 3
R <sub>F</sub>	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	_	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	_	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—			MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1		MΩ	
R <sub>S</sub>	Series resistor — low-frequency, low-power mode (HGO=0)	_			kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)		200		kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	_	_		kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)					
		—	0	_	kΩ	

## 6.3.2.1 Oscillator DC electrical specifications Table 15. Oscillator DC electrical specifications

Table continues on the next page...



Symbol	Description	Min.	Тур.	Max.	Unit	Notes			
t <sub>vfykey</sub>	Verify Backdoor Access Key execution time	—	_	30	μs	1			
	Swap Control execution time								
t <sub>swapx01</sub>	<ul> <li>control code 0x01</li> </ul>	_	200	_	μs				
t <sub>swapx02</sub>	control code 0x02	_	70	150	μs				
t <sub>swapx04</sub>	<ul> <li>control code 0x04</li> </ul>	_	70	150	μs				
t <sub>swapx08</sub>	control code 0x08	_	—	30	μs				
	Program Partition for EEPROM execution time								
t <sub>pgmpart32k</sub>	• 32 KB FlexNVM	_	70	_	ms				
	Set FlexRAM Function execution time:								
t <sub>setramff</sub>	Control Code 0xFF	—	50	—	μs				
t <sub>setram8k</sub>	8 KB EEPROM backup	_	0.3	0.5	ms				
t <sub>setram32k</sub>	32 KB EEPROM backup	_	0.7	1.0	ms				
	Byte-write to FlexRAM for EEPROM operation								
t <sub>eewr8bers</sub>	Byte-write to erased FlexRAM location execution time	_	175	260	μs	3			
	Byte-write to FlexRAM execution time:								
t <sub>eewr8b8k</sub>	8 KB EEPROM backup	_	340	1700	μs				
t <sub>eewr8b16k</sub>	16 KB EEPROM backup	_	385	1800	μs				
t <sub>eewr8b32k</sub>	32 KB EEPROM backup	_	475	2000	μs				
	Word-write to FlexRAM	for EEPRON	A operation		1				
t <sub>eewr16bers</sub>	Word-write to erased FlexRAM location execution time	_	175	260	μs				
	Word-write to FlexRAM execution time:								
t <sub>eewr16b8k</sub>	8 KB EEPROM backup	_	340	1700	μs				
t <sub>eewr16b16k</sub>	16 KB EEPROM backup	_	385	1800	μs				
t <sub>eewr16b32k</sub>	32 KB EEPROM backup	_	475	2000	μs				
	Longword-write to FlexRA	M for EEPR	OM operation	ו	1	I			
t <sub>eewr32bers</sub>	Longword-write to erased FlexRAM location execution time	_	360	540	μs				
	Longword-write to FlexRAM execution time:								
t <sub>eewr32b8k</sub>	8 KB EEPROM backup	_	545	1950	μs				
t <sub>eewr32b16k</sub>	16 KB EEPROM backup	_	630	2050	μs				
t <sub>eewr32b32k</sub>	32 KB EEPROM backup	—	810	2250	μs				

### Table 20. Flash command timing specifications (continued)

1. Assumes 25 MHz flash clock frequency.

2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.



### 6.4.1.3 Flash high voltage current behaviors Table 21. Flash high voltage current behaviors

Symbol	Description	Min.	Тур.	Max.	Unit
I <sub>DD_PGM</sub>	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I <sub>DD_ERS</sub>	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

### 6.4.1.4 Reliability specifications Table 22. NVM reliability specifications

Symbol	Description	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
	Program	n Flash				
t <sub>nvmretp10k</sub>	Data retention after up to 10 K cycles	5	50	—	years	
t <sub>nvmretp1k</sub>	Data retention after up to 1 K cycles	20	100	—	years	
n <sub>nvmcycp</sub>	Cycling endurance	10 K	50 K		cycles	2
	Data	Flash				
t <sub>nvmretd10k</sub>	Data retention after up to 10 K cycles	5	50		years	
t <sub>nvmretd1k</sub>	Data retention after up to 1 K cycles	20	100		years	
n <sub>nvmcycd</sub>	Cycling endurance	10 K	50 K		cycles	2
	FlexRAM a	s EEPROM				
t <sub>nvmretee100</sub>	Data retention up to 100% of write endurance	5	50		years	
t <sub>nvmretee10</sub>	Data retention up to 10% of write endurance	20	100		years	
	Write endurance					3
n <sub>nvmwree16</sub>	<ul> <li>EEPROM backup to FlexRAM ratio = 16</li> </ul>	35 K	175 K	—	writes	
n <sub>nvmwree128</sub>	<ul> <li>EEPROM backup to FlexRAM ratio = 128</li> </ul>	315 K	1.6 M	—	writes	
n <sub>nvmwree512</sub>	<ul> <li>EEPROM backup to FlexRAM ratio = 512</li> </ul>	1.27 M	6.4 M	—	writes	
n <sub>nvmwree4k</sub>	EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	—	writes	
n <sub>nvmwree8k</sub>	• EEPROM backup to FlexRAM ratio = 8192	20 M	100 M	—	writes	
L						

 Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.

2. Cycling endurance represents number of program/erase cycles at -40°C  $\leq$  T<sub>i</sub>  $\leq$  125°C.

3. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup per subsystem. Minimum and typical values assume all byte-writes to FlexRAM.

## 6.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

K30 Sub-Family Data Sheet, Rev. 3, 11/2012.



#### rempheral operating requirements and behaviors



Figure 17. Typical INL error vs. digital code



## 6.8.1 CAN switching specifications

See General switching specifications.

## 6.8.2 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	_	25	MHz	
DS1	DSPI_SCK output cycle time	2 x t <sub>BUS</sub>	—	ns	
DS2	DSPI_SCK output high/low time	(t <sub>SCK</sub> /2) – 2	(t <sub>SCK</sub> /2) + 2	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	(t <sub>BUS</sub> x 2) – 2	_	ns	1
DS4	DSPI_SCK to DSPI_PCSn invalid delay	(t <sub>BUS</sub> x 2) – 2	_	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	15		ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

 Table 35.
 Master mode DSPI timing (limited voltage range)

1. The delay is programmable in SPIx\_CTARn[PSSCK] and SPIx\_CTARn[CSSCK].

2. The delay is programmable in SPIx\_CTARn[PASC] and SPIx\_CTARn[ASC].







# Table 39. I2S/SAI master mode timing in Normal Run, Wait and Stop modes<br/>(full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	_	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	-1.0	-	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	20.5	-	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	_	ns



Figure 23. I2S/SAI timing — master modes

# Table 40.I2S/SAI slave mode timing in Normal Run, Wait and Stop modes<br/>(full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period

Table continues on the next page ...

# Table 40. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	5.8	-	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	_	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	5.8	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid <sup>1</sup>	_	25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear



Figure 24. I2S/SAI timing — slave modes

# 6.8.6.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

# Table 41. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period

Table continues on the next page...

#### K30 Sub-Family Data Sheet, Rev. 3, 11/2012.



64 LQFP QFN	Pin Name	Default	ALTO	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
21	VBAT	VBAT	VBAT								
22	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSI0_CH1	PTA0	UART0_CTS_ b/ UART0_COL_b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
23	PTA1	JTAG_TDI/ EZP_DI	TSI0_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
24	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO	TSI0_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
25	PTA3	JTAG_TMS/ SWD_DIO	TSI0_CH4	PTA3	UART0_RTS_b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
26	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSI0_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
27	PTA5	DISABLED		PTA5		FTM0_CH2		CMP2_OUT	I2S0_TX_BCLK	JTAG_TRST_b	
28	PTA12	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0			I2S0_TXD0	FTM1_QD_ PHA	
29	PTA13/ LLWU_P4	CMP2_IN1	CMP2_IN1	PTA13/ LLWU_P4	CAN0_RX	FTM1_CH1			12S0_TX_FS	FTM1_QD_ PHB	
30	VDD	VDD	VDD								
31	VSS	VSS	VSS								
32	PTA18	EXTALO	EXTALO	PTA18		FTM0_FLT2	FTM_CLKIN0				
33	PTA19	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ALT1		
34	RESET_b	RESET_b	RESET_b								
35	PTB0/ LLWU_P5	LCD_P0/ ADC0_SE8/ ADC1_SE8/ TSI0_CH0	LCD_P0/ ADC0_SE8/ ADC1_SE8/ TSI0_CH0	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_ PHA	LCD_P0	
36	PTB1	LCD_P1/ ADC0_SE9/ ADC1_SE9/ TSI0_CH6	LCD_P1/ ADC0_SE9/ ADC1_SE9/ TSI0_CH6	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_ PHB	LCD_P1	
37	PTB2	LCD_P2/ ADC0_SE12/ TSI0_CH7	LCD_P2/ ADC0_SE12/ TSI0_CH7	PTB2	I2C0_SCL	UARTO_RTS_b			FTM0_FLT3	LCD_P2	
38	PTB3	LCD_P3/ ADC0_SE13/ TSI0_CH8	LCD_P3/ ADC0_SE13/ TSI0_CH8	PTB3	I2C0_SDA	UART0_CTS_ b/ UART0_COL_b			FTM0_FLT0	LCD_P3	
39	PTB16	LCD_P12/ TSI0_CH9	LCD_P12/ TSI0_CH9	PTB16		UARTO_RX			EWM_IN	LCD_P12	
40	PTB17	LCD_P13/ TSI0_CH10	LCD_P13/ TSI0_CH10	PTB17		UART0_TX			EWM_OUT_b	LCD_P13	
41	PTB18	LCD_P14/ TSI0_CH11	LCD_P14/ TSI0_CH11	PTB18	CAN0_TX	FTM2_CH0	I2S0_TX_BCLK		FTM2_QD_ PHA	LCD_P14	
42	PTB19	LCD_P15/ TSI0_CH12	LCD_P15/ TSI0_CH12	PTB19	CAN0_RX	FTM2_CH1	12S0_TX_FS		FTM2_QD_ PHB	LCD_P15	
43	PTC0	LCD_P20/ ADC0_SE14/ TSI0_CH13	LCD_P20/ ADC0_SE14/ TSI0_CH13	PTC0	SPI0_PCS4	PDB0_EXTRG			12S0_TXD1	LCD_P20	



#### How to Reach Us:

Home Page: www.freescale.com

Web Support: http://www.freescale.com/support

#### **USA/Europe or Locations Not Listed:**

Freescale Semiconductor Technical Information Center, EL516 2100 East Elliot Road Tempe, Arizona 85284 +1-800-521-6274 or +1-480-768-2130 www.freescale.com/support

#### Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH Technical Information Center Schatzbogen 7 81829 Muenchen, Germany +44 1296 380 456 (English) +46 8 52200080 (English) +49 89 92103 559 (German) +33 1 69 35 48 48 (French) www.freescale.com/support

#### Japan:

Freescale Semiconductor Japan Ltd. Headquarters ARCO Tower 15F 1-8-1, Shimo-Meguro, Meguro-ku, Tokyo 153-0064 Japan 0120 191014 or +81 3 5437 9125 support.japan@freescale.com

#### Asia/Pacific:

Freescale Semiconductor China Ltd. Exchange Building 23F No. 118 Jianguo Road Chaoyang District Beijing 100022 China +86 10 5879 8000 support.asia@freescale.com Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductors products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claims alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics as their non-RoHS-complaint and/or non-Pb-free counterparts. For further information, see http://www.freescale.com or contact your Freescale sales representative.

For information on Freescale's Environmental Products program, go to http://www.freescale.com/epp.

 $\label{eq:FreescaleTM} Freescale TM and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.$ 

© 2012 Freescale Semiconductor, Inc.





Document Number: K30P64M72SF1 Rev. 3, 11/2012