Infineon Technologies - XMC4100F64F128BAXQMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP Exposed Pad
Supplier Device Package	PG-TQFP-64-19
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4100f64f128baxqma1

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Table 4 Features of XMC4[12]00 Device Types

Derivative[1)]	ADC Chan.	DAC Chan.	CCU4 Slice	CCU8 Slice	POSIF Intf.	HRPWM Intf.
XMC4200-F64x256	10	2	2 x 4	1 x 4	1	1
XMC4200-Q48x256	9	2	2 x 4	1 x 4	1	1
XMC4100-F64x128	10	2	2 x 4	1 x 4	1	1
XMC4100-Q48x128	9	2	2 x 4	1 x 4	1	1
XMC4104-F64x64	10	2	2 x 4	1 x 4	1	1
XMC4104-Q48x64	9	2	2 x 4	1 x 4	1	1
XMC4104-F64x128	10	2	2 x 4	1 x 4	1	1
XMC4104-Q48x128	9	2	2 x 4	1 x 4	1	1
XMC4108-F64x64	10	2	2 x 4	1 x 4	1	–
XMC4108-Q48x64	9	2	2 x 4	1 x 4	1	–

1) x is a placeholder for the supported temperature range.

1.5 Definition of Feature Variants

The XMC4[12]00 types are offered with several memory sizes and number of available VADC channels. **Table 5** describes the location of the available Flash memory, **Table 6** describes the location of the available SRAMs, **Table 7** the available VADC channels.

Table 5 Flash Memory Ranges

Total Flash Size	Cached Range	Uncached Range
256 Kbytes	$0800\ 0000_H$ – $0803\ FFFF_H$	$0C00\ 0000_H$ – $0C03\ FFFF_H$
128 Kbytes	$0800\ 0000_H$ – $0801\ FFFF_H$	$0C00\ 0000_H$ – $0C01\ FFFF_H$
64 Kbytes	$0800\ 0000_H$ – $0800\ FFFF_H$	$0C00\ 0000_H$ – $0C00\ FFFF_H$

Table 9 XMC4100 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	0004 2001$_H$	EES-AA, ES-AA
SCU_IDCHIP	0004 2002$_H$	ES-AB, AB
SCU_IDCHIP	0004 1003$_H$	BA
JTAG IDCODE	101D D083$_H$	EES-AA, ES-AA
JTAG IDCODE	201D D083$_H$	ES-AB, AB
JTAG IDCODE	301D D083$_H$	BA

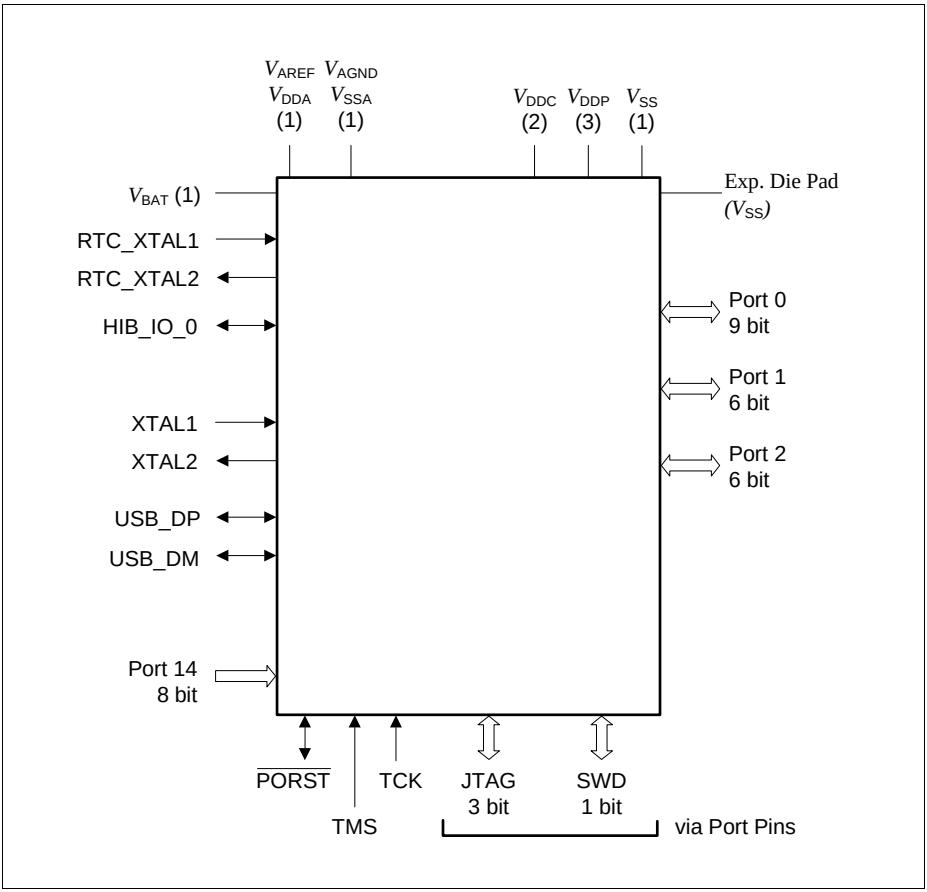

Figure 3 XMC4[12]00 Logic Symbol PG-VQFN-48

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

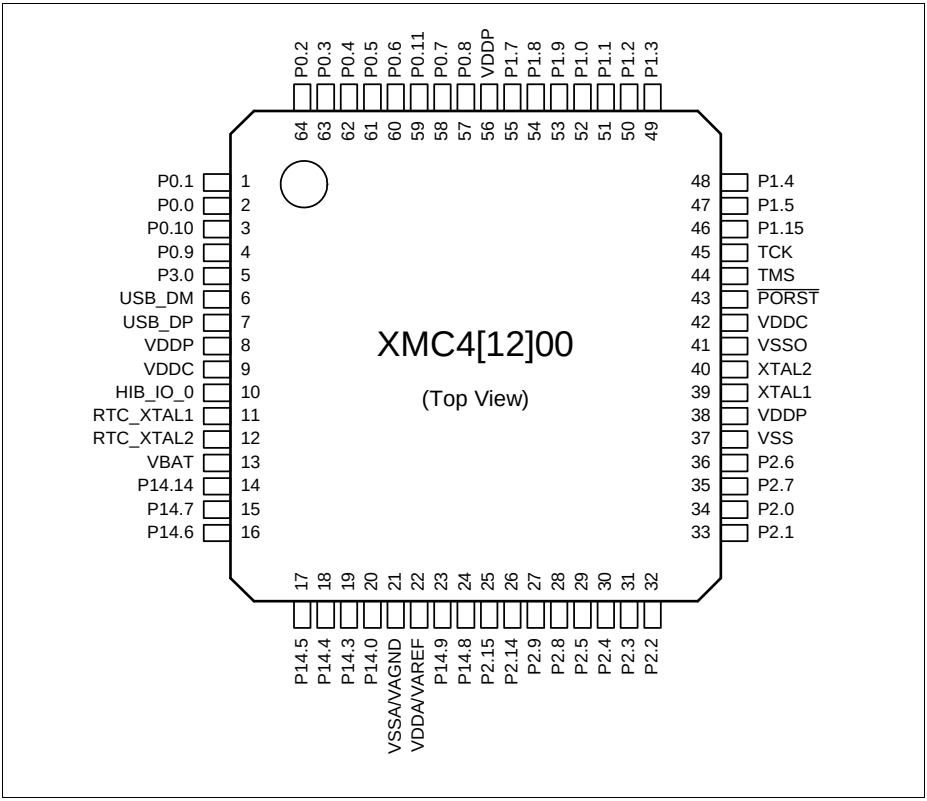

Figure 4 XMC4[12]00 PG-LQFP-64 and PG-TQFP-64 Pin Configuration (top view)

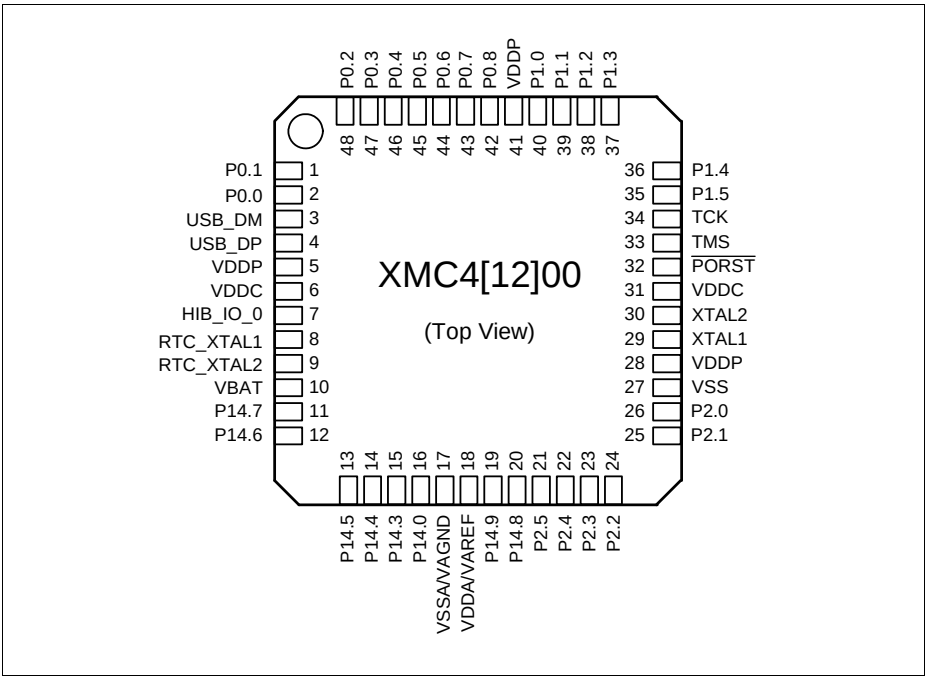

Figure 5 XMC4[12]00 PG-VQFN-48 Pin Configuration (top view)

Figure 8 explains the input voltage ranges of V_{IN} and V_{AIN} and its dependency to the supply level of V_{DDP}.The input voltage must not exceed 4.3 V, and it must not be more than 1.0 V above V_{DDP}. For the range up to V_{DDP} + 1.0 V also see the definition of the overload conditions in **Section 3.1.3**.

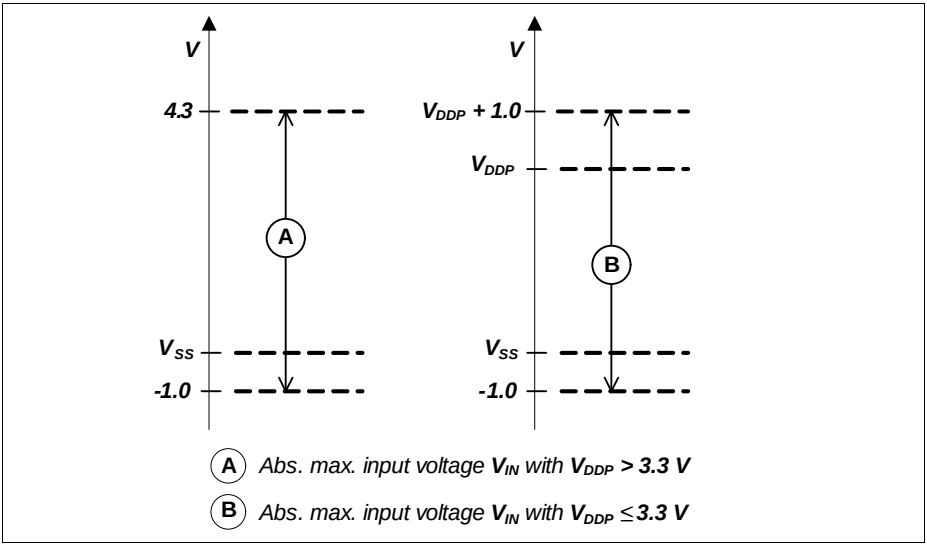

Figure 8 Absolute Maximum Input Voltage Ranges

3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 15 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
  - pad supply levels (V_{DDP} or V_{DDA})
  - temperature

If a pin current is outside of the **Operating Conditions** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

Table 15 Overload Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Input current on any port pin during overload condition	I_{OV}	SR	-5	–	5	mA	
Absolute sum of all input circuit currents for one port group during overload condition[1)]	I_{OVG}	SR	–	–	20	mA	$\Sigma\|I_{OVx}\|$, for all $I_{OVx} < 0$ mA
			–	–	20	mA	$\Sigma\|I_{OVx}\|$, for all $I_{OVx} > 0$ mA
Absolute sum of all input circuit currents during overload condition	I_{OVS}	SR	–	–	80	mA	ΣI_{OVG}

1) The port groups are defined in **Table 18**.

Figure 9 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

Table 22 Standard Pads Class_A1

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Input leakage current	I_{OZA1} CC	-500		500	nA	0 V ≤ V_{IN} ≤ V_{DDP}
Input high voltage	V_{IHA1} SR	0.6 × V_{DDP}		V_{DDP} + 0.3	V	max. 3.6 V
Input low voltage	V_{ILA1} SR	-0.3		0.36 × V_{DDP}	V	
Output high voltage, POD[1] = weak	V_{OHA1} CC	V_{DDP} - 0.4		–	V	I_{OH} ≥ -400 µA
		2.4		–	V	I_{OH} ≥ -500 µA
Output high voltage, POD[1] = medium		V_{DDP} - 0.4		–	V	I_{OH} ≥ -1.4 mA
		2.4		–	V	I_{OH} ≥ -2 mA
Output low voltage	V_{OLA1} CC	–		0.4	V	I_{OL} ≤ 500 µA; POD[1] = weak
		–		0.4	V	I_{OL} ≤ 2 mA; POD[1] = medium
Fall time	t_{FA1} CC	–		150	ns	C_L = 20 pF; POD[1] = weak
		–		50	ns	C_L = 50 pF; POD[1] = medium
Rise time	t_{RA1} CC	–		150	ns	C_L = 20 pF; POD[1] = weak
		–		50	ns	C_L = 50 pF; POD[1] = medium

1) POD = Pin Out Driver

Table 23 Standard Pads Class_A1+

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Input leakage current	I_{OZA1+} CC	-1		1	µA	0 V ≤ V_{IN} ≤ V_{DDP}
Input high voltage	V_{IHA1+} SR	0.6 × V_{DDP}		V_{DDP} + 0.3	V	max. 3.6 V
Input low voltage	V_{ILA1+} SR	-0.3		0.36 × V_{DDP}	V	

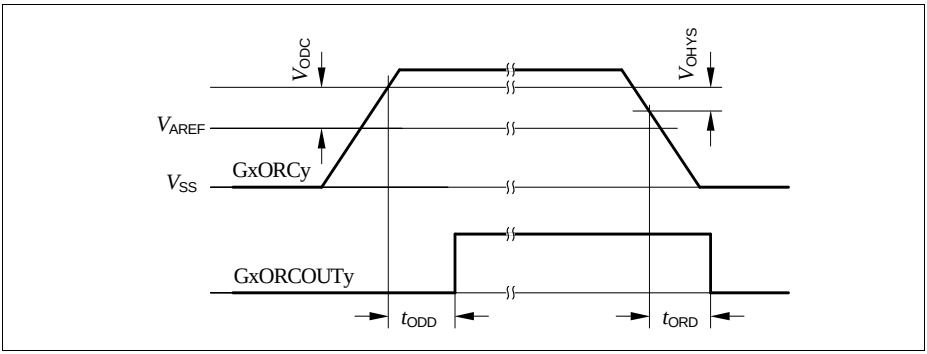

Figure 16 GxORCOUTy Trigger Generation

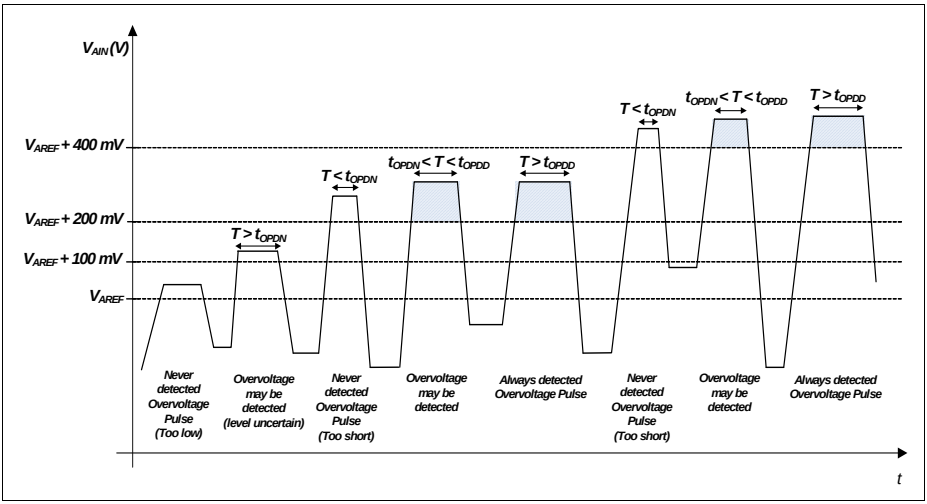

Figure 17 ORC Detection Ranges

Table 30 CMP and 10-bit DAC characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
CSG Output Jitter	D_{CSG} CC	–	–	1	clk	
Bias startup time	t_{start} CC	–	–	98	us	
Bias supply current	I_{DDbias} CC	–	–	400	µA	
CSGy startup time	t_{CSGS} CC	–	–	2	µs	
Input operation current[1]	I_{DDCIN} CC	-10	–	33	µA	See **Figure 19**
High Speed Mode						
DAC output voltage range	V_{DOUT} CC	V_{SS}	–	V_{DDP}	V	
DAC propagation delay - Full scale	t_{FShs} CC	–	–	80	ns	See **Figure 20**
Input Selector propagation delay - Full scale	t_{Dhs} CC	–	–	100	ns	See **Figure 20**
Comparator bandwidth	t_{Dhs} CC	20	–	–	ns	
DAC CLK frequency	f_{clk} SR	–	–	30	MHz	
Supply current	I_{DDhs} CC	–	–	940	µA	
Low Speed Mode						
DAC output voltage range	V_{DOUT} CC	0.1 × V_{DDP}[2]	–	V_{DDP}	V	
DAC propagation delay - Full Scale	t_{FSls} CC	–	–	160	ns	See **Figure 20**
Input Selector propagation delay - Full Scale	t_{Dls} CC	–	–	200	ns	See **Figure 20**
Comparator bandwidth	t_{Dls} CC	20	–	–	ns	
DAC CLK frequency	f_{clk} SR	–	–	30	MHz	
Supply current	I_{DDls} CC	–	–	300	µA	

1) Typical input resistance R_{CIN} = 100kOhm.

2) The INL error increases for DAC output voltages below this limit.

3.2.7 Die Temperature Sensor

The Die Temperature Sensor (DTS) measures the junction temperature T_J.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 34 Die Temperature Sensor Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Temperature sensor range	T_{SR}	SR	-40	–	150	°C	
Linearity Error (to the below defined formula)	ΔT_{LE}	CC	–	±1	–	°C	per $\Delta T_J \leq 30$ °C
Offset Error	ΔT_{OE}	CC	–	±6	–	°C	$\Delta T_{OE} = T_J - T_{DTS}$ $V_{DDP} \leq 3.3$ V[1]
Measurement time	t_M	CC	–	–	100	µs	
Start-up time after reset inactive	t_{TSST}	SR	–	–	10	µs	

1) At V_{DDP_max} = 3.63 V the typical offset error increases by an additional ΔT_{OE} = ±1 °C.

The following formula calculates the temperature measured by the DTS in [°C] from the RESULT bit field of the DTSSTAT register.

Temperature T_{DTS} = (RESULT - 605) / 2.05 [°C]

This formula and the values defined in **Table 34** apply with the following calibration values:

- DTSCON.BGTRIM = 8_H
- DTSCON.REFTRIM = 4_H

3.2.9 Oscillator Pins

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The oscillator pins can be operated with an external crystal (see **Figure 21**) or in direct input mode (see **Figure 22**).

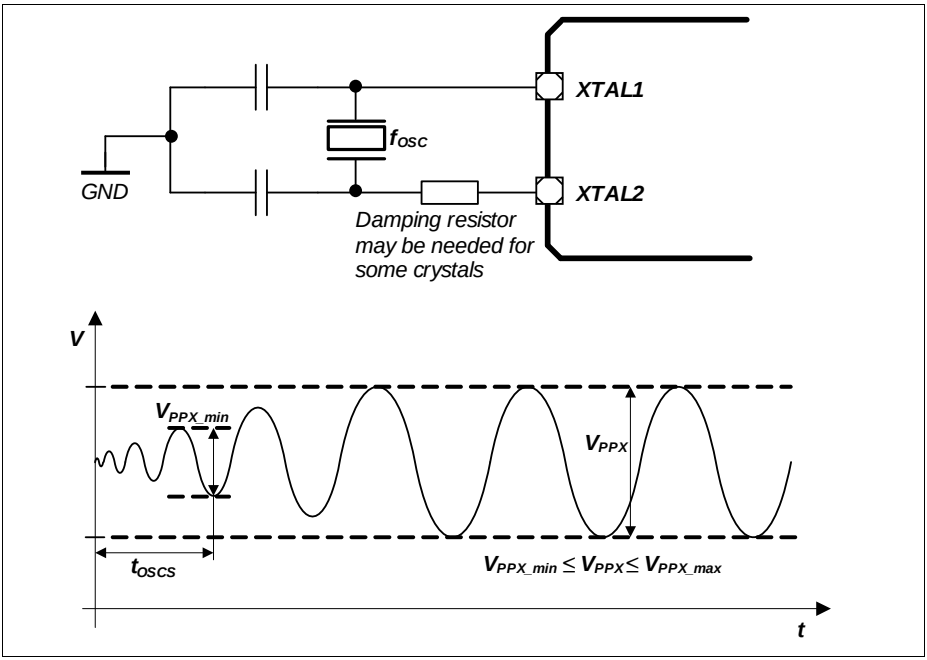

Figure 21 Oscillator in Crystal Mode

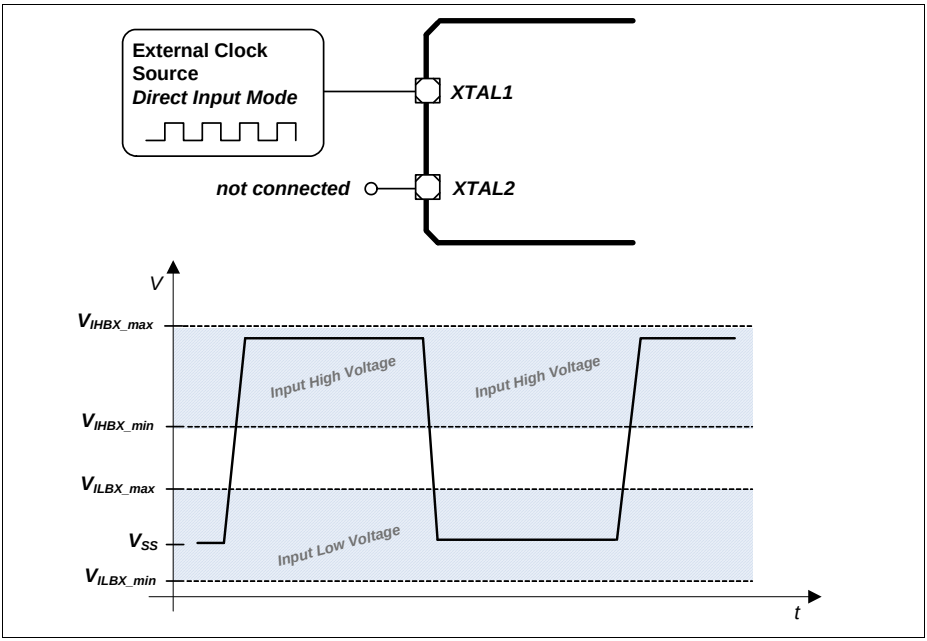

Figure 22 Oscillator in Direct Input Mode

Table 38 Power Supply Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sleep supply current[3] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS} CC	–	76	–	mA	80 / 80 / 80
		–	73	–		80 / 40 / 40
		–	70	–		40 / 40 / 80
		–	56	–		24 / 24 / 24
		–	47	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	46	–		100 / 100 / 100
Sleep supply current[4] Peripherals disabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS} CC	–	59	–	mA	80 / 80 / 80
		–	58	–		80 / 40 / 40
		–	57	–		40 / 40 / 80
		–	51	–		24 / 24 / 24
		–	46	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	46	–		100 / 100 / 100
Deep Sleep supply current[5] Flash in Sleep mode Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPD} CC	–	6.9	–	mA	24 / 24 / 24
		–	4.3	–		4 / 4 / 4
		–	3.8	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	4.5	–		100 / 100 / 100 [6]
Hibernate supply current RTC on[7]	I_{DDPH} CC	–	10.8	–	µA	V_{BAT} = 3.3 V
		–	8.0	–		V_{BAT} = 2.4 V
		–	6.8	–		V_{BAT} = 2.0 V
Hibernate supply current RTC off[8]	I_{DDPH} CC	–	10.3	–	µA	V_{BAT} = 3.3 V
		–	7.5	–		V_{BAT} = 2.4 V
		–	6.3	–		V_{BAT} = 2.0 V
Worst case active supply current[9]	I_{DDPA} CC	–	–	140 [10]	mA	V_{DDP} = 3.6 V, T_J = 150 °C
V_{DDA} power supply current	I_{DDA} CC	–	–	–[11]	mA	
I_{DDP} current at $\overline{\text{PORST}}$ Low	I_{DDP_PORST} CC	–	–	24	mA	V_{DDP} = 3.6 V, T_J = 150 °C

3.3.2 Power-Up and Supply Monitoring

$\overline{\text{PORST}}$ is always asserted when V_{DDP} and/or V_{DDC} violate the respective thresholds.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

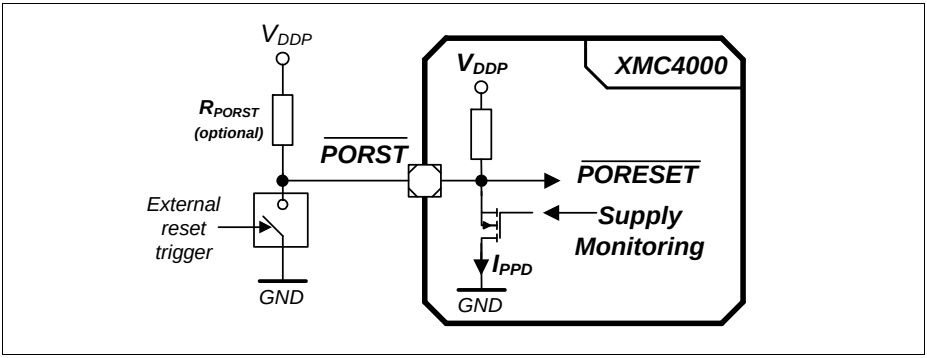

Figure 26 $\overline{\text{PORST}}$ Circuit

Table 41 Supply Monitoring Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage reset threshold	V_{POR} CC	2.79[1]	–	3.05[2]	V	[3]
Core supply voltage reset threshold	V_{PV} CC	–	–	1.17	V	
V_{DDP} voltage to ensure defined pad states	V_{DDPPA} CC	–	1.0	–	V	
$\overline{\text{PORST}}$ rise time	t_{PR} SR	–	–	2	µs	
Startup time from power-on reset with code execution from Flash	t_{SSW} CC	–	2.5	3.5	ms	Time to the first user code instruction
V_{DDC} ramp up time	t_{VCR} CC	–	550	–	µs	Ramp up after power-on or after a reset triggered by a violation of V_{POR} or V_{PV}

1) Minimum threshold for reset assertion.

3.3.7 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

Table 47 SWD Interface Timing Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SWDCLK clock period	t_{SC}	SR	25	–	–	ns	C_L = 30 pF
			40	–	–	ns	C_L = 50 pF
SWDCLK high time	t_1	SR	10	–	500000	ns	
SWDCLK low time	t_2	SR	10	–	500000	ns	
SWDIO input setup to SWDCLK rising edge	t_3	SR	6	–	–	ns	
SWDIO input hold after SWDCLK rising edge	t_4	SR	6	–	–	ns	
SWDIO output valid time after SWDCLK rising edge	t_5	CC	–	–	17	ns	C_L = 50 pF
			–	–	13	ns	C_L = 30 pF
SWDIO output hold time from SWDCLK rising edge	t_6	CC	3	–	–	ns	

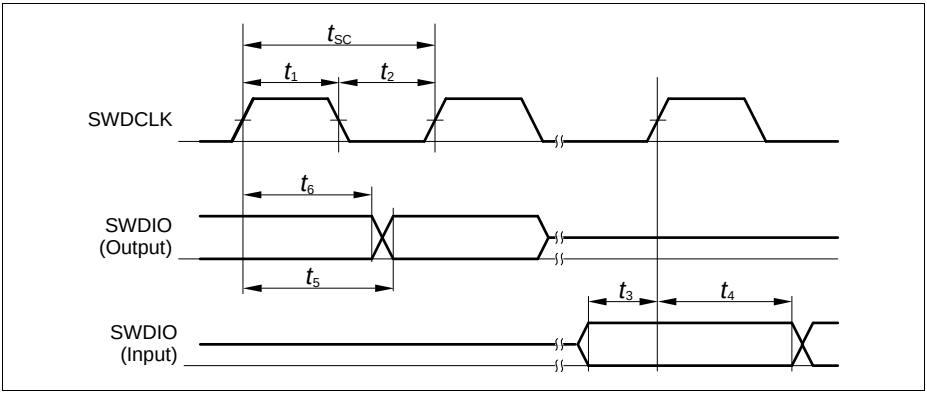

Figure 30 SWD Timing

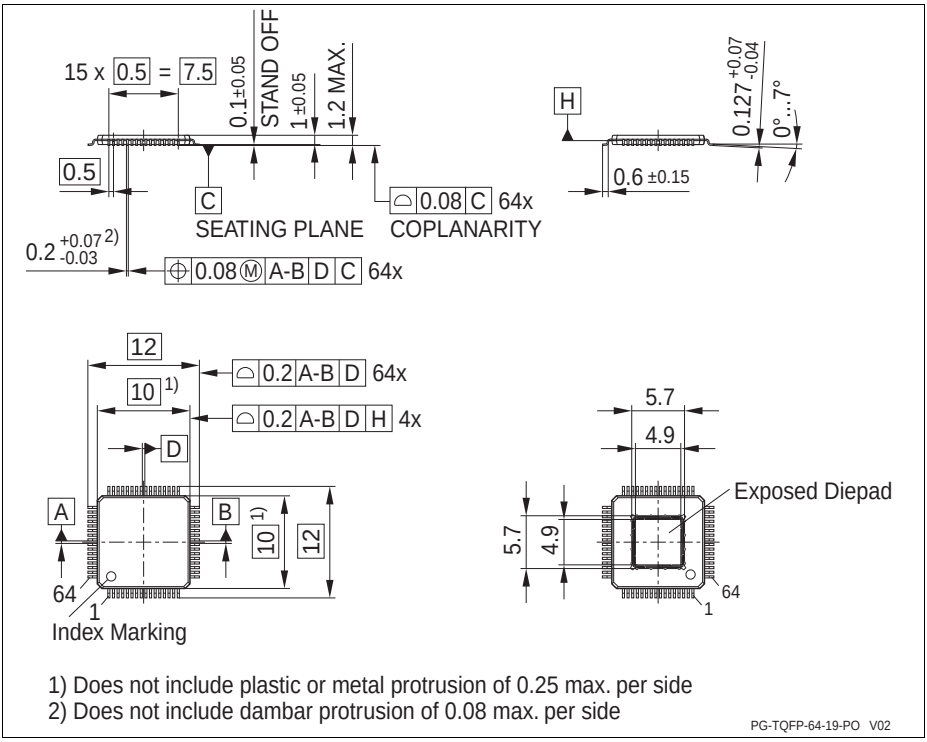

Figure 37 PG-TQFP-64-19 (Plastic Green Thin Profile Quad Flat Package)

Table 57 Differences PG-VQFN-48-53 to PG-VQFN-48-71

Change	PG-VQFN-48-53	PG-VQFN-48-71
Package corner	chamfered	right-angled
Lead width	$0.23^{\pm 0.05}$ mm	$0.25^{(+0.05, -0.07)}$ mm
Lead height	$0.4^{\pm 0.07}$ mm	$0.4^{\pm 0.05}$ mm

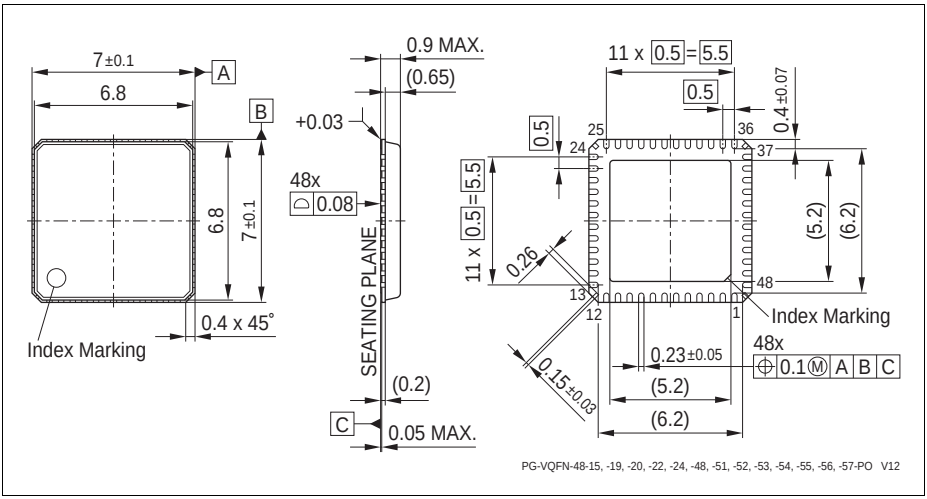

Figure 38 **PG-VQFN-48-53** (Plastic Green Very Thin Profile Flat Non Leaded Package)

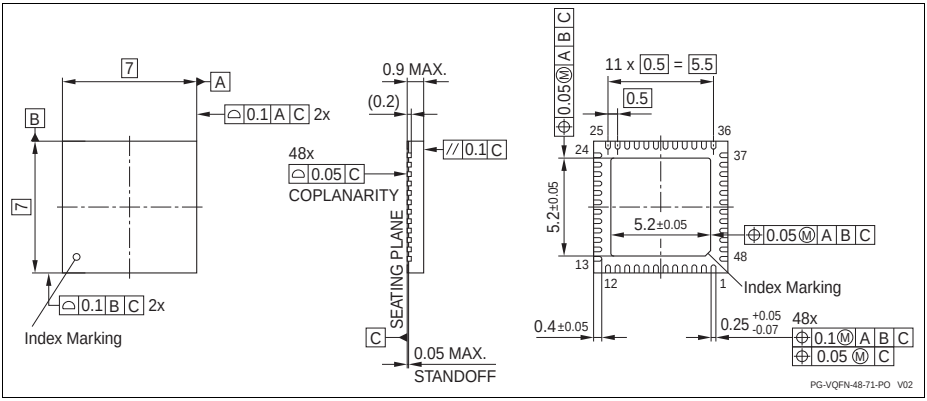

Figure 39 **PG-VQFN-48-71** (Plastic Green Very Thin Profile Flat Non Leaded Package)

All dimensions in mm.

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