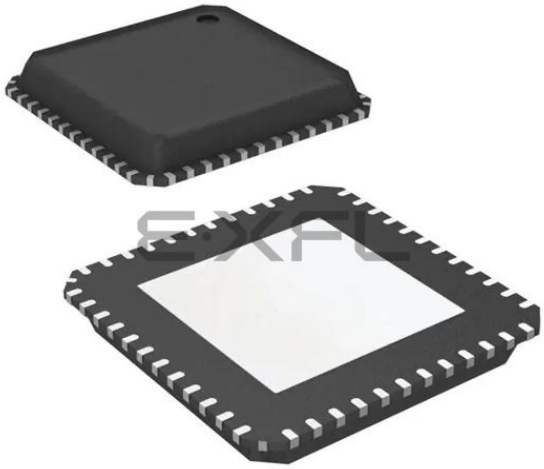
Infineon Technologies - XMC4100Q48K128ABXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 9x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-22
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4100q48k128abxuma1

About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC4[12]00 series devices.

The document describes the characteristics of a superset of the XMC4[12]00 series devices. For simplicity, the various device types are referred to by the collective term XMC4[12]00 throughout this manual.

XMC4000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  – decribes the functionality of the superset of devices.
- **Data Sheets**
  – list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  – list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to **http://www.infineon.com/xmc4000** to get access to the latest versions of those documents.

Table 4 Features of XMC4[12]00 Device Types

Derivative[1)]	ADC Chan.	DAC Chan.	CCU4 Slice	CCU8 Slice	POSIF Intf.	HRPWM Intf.
XMC4200-F64x256	10	2	2 x 4	1 x 4	1	1
XMC4200-Q48x256	9	2	2 x 4	1 x 4	1	1
XMC4100-F64x128	10	2	2 x 4	1 x 4	1	1
XMC4100-Q48x128	9	2	2 x 4	1 x 4	1	1
XMC4104-F64x64	10	2	2 x 4	1 x 4	1	1
XMC4104-Q48x64	9	2	2 x 4	1 x 4	1	1
XMC4104-F64x128	10	2	2 x 4	1 x 4	1	1
XMC4104-Q48x128	9	2	2 x 4	1 x 4	1	1
XMC4108-F64x64	10	2	2 x 4	1 x 4	1	–
XMC4108-Q48x64	9	2	2 x 4	1 x 4	1	–

1) x is a placeholder for the supported temperature range.

1.5 Definition of Feature Variants

The XMC4[12]00 types are offered with several memory sizes and number of available VADC channels. **Table 5** describes the location of the available Flash memory, **Table 6** describes the location of the available SRAMs, **Table 7** the available VADC channels.

Table 5 Flash Memory Ranges

Total Flash Size	Cached Range	Uncached Range
256 Kbytes	$0800\ 0000_H$ – $0803\ FFFF_H$	$0C00\ 0000_H$ – $0C03\ FFFF_H$
128 Kbytes	$0800\ 0000_H$ – $0801\ FFFF_H$	$0C00\ 0000_H$ – $0C01\ FFFF_H$
64 Kbytes	$0800\ 0000_H$ – $0800\ FFFF_H$	$0C00\ 0000_H$ – $0C00\ FFFF_H$

Table 9 XMC4100 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	0004 2001$_H$	EES-AA, ES-AA
SCU_IDCHIP	0004 2002$_H$	ES-AB, AB
SCU_IDCHIP	0004 1003$_H$	BA
JTAG IDCODE	101D D083$_H$	EES-AA, ES-AA
JTAG IDCODE	201D D083$_H$	ES-AB, AB
JTAG IDCODE	301D D083$_H$	BA

2.2.1 Package Pin Summary

The following general scheme is used to describe each pin:

Table 10 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type	Notes
Name	N	Ax	...	A1+	

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the dedicated pins (i.e. PORST) and supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type (A1, A1+, special=special pad, In=input pad, AN/DIG_IN=analog and digital input, Power=power supply). Details about the pad properties are defined in the Electrical Parameters.

In the “Notes”, special information to the respective pin/function is given, i.e. deviations from the default configuration after reset. Per default the regular Port pins are configured as direct input with no internal pull device active.

Table 11 Package Pin Mapping

Function	LQFP-64 TQFP-64	VQFN-48	Pad Type	Notes
P0.0	2	2	A1+	
P0.1	1	1	A1+	
P0.2	64	48	A1+	
P0.3	63	47	A1+	
P0.4	62	46	A1+	
P0.5	61	45	A1+	
P0.6	60	44	A1+	
P0.7	58	43	A1+	After a system reset, via HWSEL this pin selects the DB.TDI function.
P0.8	57	42	A1+	After a system reset, via HWSEL this pin selects the DB.TRST function, with a weak pull-down active.
P0.9	4	-	A1+	
P0.10	3	-	A1+	

Table 11 Package Pin Mapping (cont'd)

Function	LQFP-64 TQFP-64	VQFN-48	Pad Type	Notes
P0.11	59	-	A1+	
P1.0	52	40	A1+	
P1.1	51	39	A1+	
P1.2	50	38	A1+	
P1.3	49	37	A1+	
P1.4	48	36	A1+	
P1.5	47	35	A1+	
P1.7	55	-	A1+	
P1.8	54	-	A1+	
P1.9	53	-	A1+	
P1.15	46	-	A1+	
P2.0	34	26	A1+	
P2.1	33	25	A1+	After a system reset, via HWSEL this pin selects the DB.TDO function.
P2.2	32	24	A1+	
P2.3	31	23	A1+	
P2.4	30	22	A1+	
P2.5	29	21	A1+	
P2.6	36	-	A1+	
P2.7	35	-	A1+	
P2.8	28	-	A1+	
P2.9	27	-	A1+	
P2.14	26	-	A1+	
P2.15	25	-	A1+	
P3.0	5	-	A1+	
P14.0	20	16	AN/DIG_IN	
P14.3	19	15	AN/DIG_IN	
P14.4	18	14	AN/DIG_IN	
P14.5	17	13	AN/DIG_IN	
P14.6	16	12	AN/DIG_IN	
P14.7	15	11	AN/DIG_IN	
P14.8	24	20	AN/DAC/DIG_IN	

Table 11 Package Pin Mapping (cont'd)

Function	LQFP-64 TQFP-64	VQFN-48	Pad Type	Notes
P14.9	23	19	AN/DAC/DIG_IN	
P14.14	14	-	AN/DIG_IN	
USB_DP	7	4	special	
USB_DM	6	3	special	
HIB_IO_0	10	7	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as open-drain output and drives "0". As output the medium driver mode is active.
TCK	45	34	A1	Weak pull-down active.
TMS	44	33	A1+	Weak pull-up active. As output the strong-soft driver mode is active.
$\overline{\text{PORST}}$	43	32	special	Strong pull-down controlled by EVR. Weak pull-up active while strong pull-down is not active.
XTAL1	39	29	clock_IN	
XTAL2	40	30	clock_O	
RTC_XTAL1	11	8	clock_IN	
RTC_XTAL2	12	9	clock_O	
VBAT	13	10	Power	When VDDP is supplied VBAT has to be supplied as well.
VDDA/VAREF	22	18	AN_Power/AN_ Ref	Shared analog supply and reference voltage pin.
VSSA/VAGND	21	17	AN_Power/AN_ Ref	Shared analog supply and reference ground pin.
VDDC	9	6	Power	
VDDC	42	31	Power	
VDDP	8	5	Power	
VDDP	38	28	Power	
VDDP	56	41	Power	
VSS	37	27	Power	

3 Electrical Parameters

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the XMC4[12]00 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are a distinctive feature of the XMC4[12]00 and must be regarded for system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC4[12]00 is designed in.

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 14 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Storage temperature	T_{ST}	SR	-65	–	150	°C	–
Junction temperature	T_J	SR	-40	–	150	°C	–
Voltage at 3.3 V power supply pins with respect to V_{SS}	V_{DDP}	SR	–	–	4.3	V	–
Voltage on any Class A and dedicated input pin with respect to V_{SS}	V_{IN}	SR	-1.0	–	V_{DDP} + 1.0 or max. 4.3	V	whichever is lower
Voltage on any analog input pin with respect to V_{AGND}	V_{AIN} V_{AREF}	SR	-1.0	–	V_{DDP} + 1.0 or max. 4.3	V	whichever is lower
Input current on any pin during overload condition	I_{IN}	SR	-10	–	+10	mA	
Absolute maximum sum of all input circuit currents for one port group during overload condition[1)]	ΣI_{IN}	SR	-25	–	+25	mA	
Absolute maximum sum of all input circuit currents during overload condition	ΣI_{IN}	SR	-100	–	+100	mA	

1) The port groups are defined in **Table 18**.

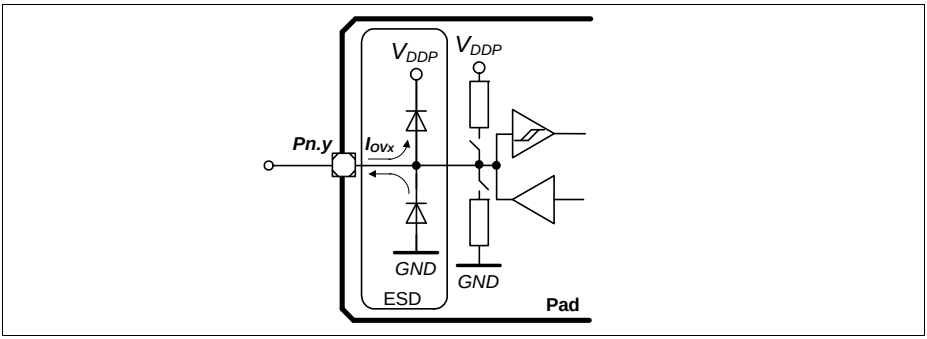

Figure 9 Input Overload Current via ESD structures

Table 16 and **Table 17** list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the **Absolute Maximum Ratings** must not be exceeded during overload.

Table 16 PN-Junction Characterisitics for positive Overload

Pad Type	I_{OV} = 5 mA, T_J = -40 °C	I_{OV} = 5 mA, T_J = 150 °C
A1 / A1+	$V_{IN} = V_{DDP} + 1.0$ V	$V_{IN} = V_{DDP} + 0.75$ V
AN/DIG_IN	$V_{IN} = V_{DDP} + 1.0$ V	$V_{IN} = V_{DDP} + 0.75$ V

Table 17 PN-Junction Characterisitics for negative Overload

Pad Type	I_{OV} = 5 mA, T_J = -40 °C	I_{OV} = 5 mA, T_J = 150 °C
A1 / A1+	$V_{IN} = V_{SS} - 1.0$ V	$V_{IN} = V_{SS} - 0.75$ V
AN/DIG_IN	$V_{IN} = V_{DDP} - 1.0$ V	$V_{IN} = V_{DDP} - 0.75$ V

Table 18 Port Groups for Overload and Short-Circuit Current Sum Parameters

Group	Pins
1	P0.[12:0], P3.0
2	P14.[8:0]
3	P2.[15:0]
4	P1.[15:0]

3.1.5 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC4[12]00. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 20 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A SR	-40	–	85	°C	Temp. Range F
		-40	–	125	°C	Temp. Range K
Digital supply voltage	V_{DDP} SR	3.13[1]	3.3	3.63[2]	V	
Core Supply Voltage	V_{DDC} CC	–[1]	1.3	–	V	Generated internally
Digital ground voltage	V_{SS} SR	0	–	–	V	
ADC analog supply voltage	V_{DDA} SR	3.0	3.3	3.6[2]	V	
Analog ground voltage for V_{DDA}	V_{SSA} SR	-0.1	0	0.1	V	
Battery Supply Voltage for Hibernate Domain[3]	V_{BAT} SR	1.95[4]	–	3.63	V	When V_{DDP} is supplied V_{BAT} has to be supplied as well.
System Frequency	f_{SYS} SR	–	–	80	MHz	
Short circuit current of digital outputs	I_{SC} SR	-5	–	5	mA	
Absolute sum of short circuit currents per pin group[5]	ΣI_{SC_PG} SR	–	–	20	mA	
Absolute sum of short circuit currents of the device	ΣI_{SC_D} SR	–	–	100	mA	

1) See also the Supply Monitoring thresholds, **Section 3.3.2**.

2) Voltage overshoot to 4.0 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h over lifetime.

3) Different limits apply for LPAC operation, **Section 3.2.6**

4) To start the hibernate domain it is required that $V_{BAT} \geq 2.1$ V, for a reliable start of the oscillation of RTC_XTAL in crystal mode it is required that $V_{BAT} \geq 3.0$ V.

5) The port groups are defined in **Table 18**.

3.2 DC Parameters

3.2.1 Input/Output Pins

The digital input stage of the shared analog/digital input pins is identical to the input stage of the standard digital input/output pins.
The pull-up characteristics (I_{PUH}) and the input high and low voltage levels (V_{IH} and V_{IL}) of the $\overline{\text{PORST}}$ pin are identical to the respective values of the standard digital input/output pins.

Table 21 Standard Pad Parameters

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Pin capacitance (digital inputs/outputs)	C_{IO} CC	–	10	pF	
Pull-down current	$\lvert I_{PDL}\rvert$ SR	150	–	µA	1) $V_{IN} \geq 0.6 \times V_{DDP}$
		–	10	µA	2) $V_{IN} \leq 0.36 \times V_{DDP}$
Pull-up current	$\lvert I_{PUH}\rvert$ SR	–	10	µA	2) $V_{IN} \geq 0.6 \times V_{DDP}$
		100	–	µA	1) $V_{IN} \leq 0.36 \times V_{DDP}$
Input Hysteresis for pads of all A classes[3]	$HYSA$ CC	$0.1 \times V_{DDP}$	–	V	
$\overline{\text{PORST}}$ spike filter always blocked pulse duration	t_{SF1} CC	–	10	ns	
$\overline{\text{PORST}}$ spike filter pass-through pulse duration	t_{SF2} CC	100	–	ns	
$\overline{\text{PORST}}$ pull-down current	$\lvert I_{PPD}\rvert$ CC	13	–	mA	$V_i = 1.0$ V

1) Current required to override the pull device with the opposite logic level (“force current”).
With active pull device, at load currents between force and keep current the input state is undefined.

2) Load current at which the pull device still maintains the valid logic level (“keep current”).
With active pull device, at load currents between force and keep current the input state is undefined.

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

Table 23 Standard Pads Class_A1+

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Output high voltage, POD[1] = weak	V_{OHA1+} CC	V_{DDP} - 0.4		–	V	$I_{OH} \geq$ -400 µA
		2.4		–	V	$I_{OH} \geq$ -500 µA
Output high voltage, POD[1] = medium		V_{DDP} - 0.4		–	V	$I_{OH} \geq$ -1.4 mA
		2.4		–	V	$I_{OH} \geq$ -2 mA
Output high voltage, POD[1] = strong		V_{DDP} - 0.4		–	V	$I_{OH} \geq$ -1.4 mA
		2.4		–	V	$I_{OH} \geq$ -2 mA
Output low voltage	V_{OLA1+} CC	–		0.4	V	$I_{OL} \leq$ 500 µA; POD[1] = weak
		–		0.4	V	$I_{OL} \leq$ 2 mA; POD[1] = medium
		–		0.4	V	$I_{OL} \leq$ 2 mA; POD[1] = strong
Fall time	t_{FA1+} CC	–		150	ns	C_L = 20 pF; POD[1] = weak
		–		50	ns	C_L = 50 pF; POD[1] = medium
		–		28	ns	C_L = 50 pF; POD[1] = strong; edge = slow
		–		16	ns	C_L = 50 pF; POD[1] = strong; edge = soft;
Rise time	t_{RA1+} CC	–		150	ns	C_L = 20 pF; POD[1] = weak
		–		50	ns	C_L = 50 pF; POD[1] = medium
		–		28	ns	C_L = 50 pF; POD[1] = strong; edge = slow
		–		16	ns	C_L = 50 pF; POD[1] = strong; edge = soft

1) POD = Pin Out Driver

Table 30 CMP and 10-bit DAC characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
CSG Output Jitter	D_{CSG} CC	–	–	1	clk	
Bias startup time	t_{start} CC	–	–	98	us	
Bias supply current	I_{DDbias} CC	–	–	400	µA	
CSGy startup time	t_{CSGS} CC	–	–	2	µs	
Input operation current[1]	I_{DDCIN} CC	-10	–	33	µA	See **Figure 19**
High Speed Mode						
DAC output voltage range	V_{DOUT} CC	V_{SS}	–	V_{DDP}	V	
DAC propagation delay - Full scale	t_{FShs} CC	–	–	80	ns	See **Figure 20**
Input Selector propagation delay - Full scale	t_{Dhs} CC	–	–	100	ns	See **Figure 20**
Comparator bandwidth	t_{Dhs} CC	20	–	–	ns	
DAC CLK frequency	f_{clk} SR	–	–	30	MHz	
Supply current	I_{DDhs} CC	–	–	940	µA	
Low Speed Mode						
DAC output voltage range	V_{DOUT} CC	0.1 × V_{DDP}[2]	–	V_{DDP}	V	
DAC propagation delay - Full Scale	t_{FSls} CC	–	–	160	ns	See **Figure 20**
Input Selector propagation delay - Full Scale	t_{Dls} CC	–	–	200	ns	See **Figure 20**
Comparator bandwidth	t_{Dls} CC	20	–	–	ns	
DAC CLK frequency	f_{clk} SR	–	–	30	MHz	
Supply current	I_{DDls} CC	–	–	300	µA	

1) Typical input resistance R_{CIN} = 100kOhm.

2) The INL error increases for DAC output voltages below this limit.

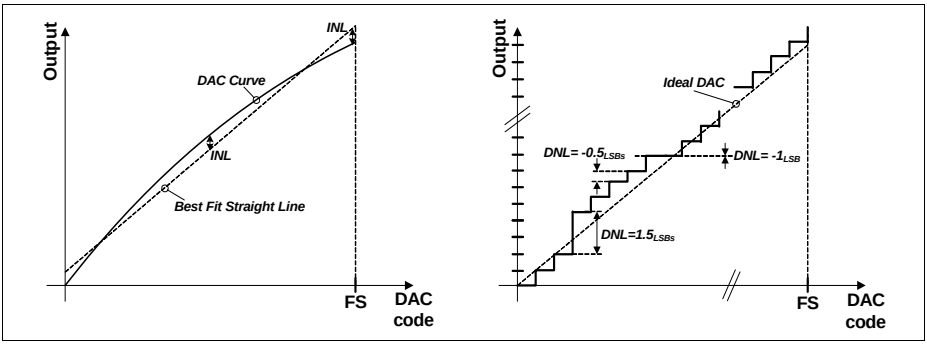

Figure 18 CSG DAC INL and DNL example

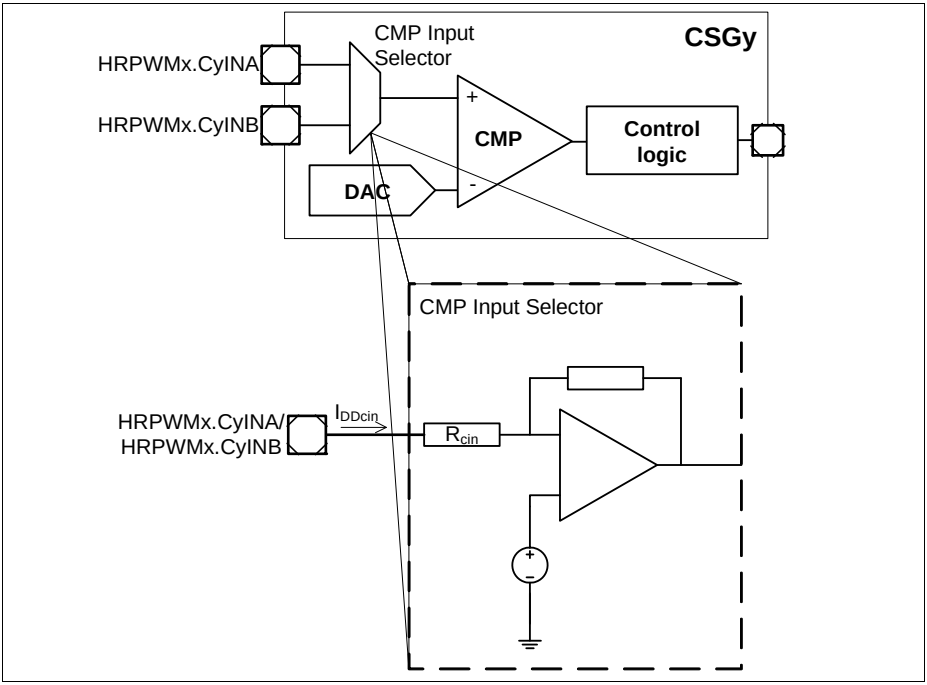

Figure 19 Input operation current

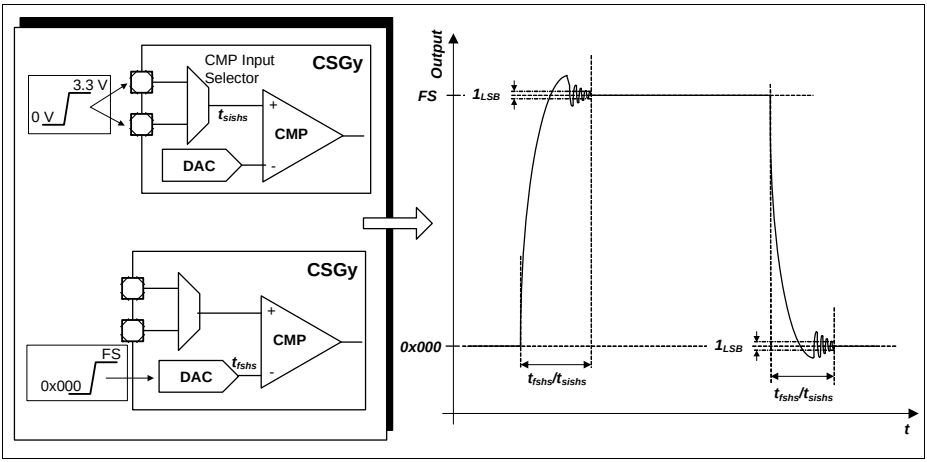

Figure 20 DAC and Input Selector Propagation Delay

3.2.5.3 Clocks

HRPWM DAC Conversion Clock

The DAC conversion clock can be generated internally or it can be controlled via a HRPWM module pin.

Table 31 External DAC conversion trigger operating conditions

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Frequency	f_{etrg}	SR	–	–	30[2)]	MHz	
ON time	t_{onetrg}	SR	$2T_{ccu}$[1)2)]	–	–	ns	
OFF time	$t_{offetrg}$	SR	$2T_{ccu}$[1)2)]	–	–	ns	

1) 50% duty cycle is not obligatory

2) Only valid if the signal was not previously synchronized/generated with the fccu clock (or a synchronous clock)

CSG External Clock

It is possible to select an external source, that can be used as a clock for the slope generation, HRPWMx.ECLKy. This clock is synchronized internally with the module clock and therefore the external clock needs to meet the criterion described on **Table 32**.

3.2.9 Oscillator Pins

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The oscillator pins can be operated with an external crystal (see **Figure 21**) or in direct input mode (see **Figure 22**).

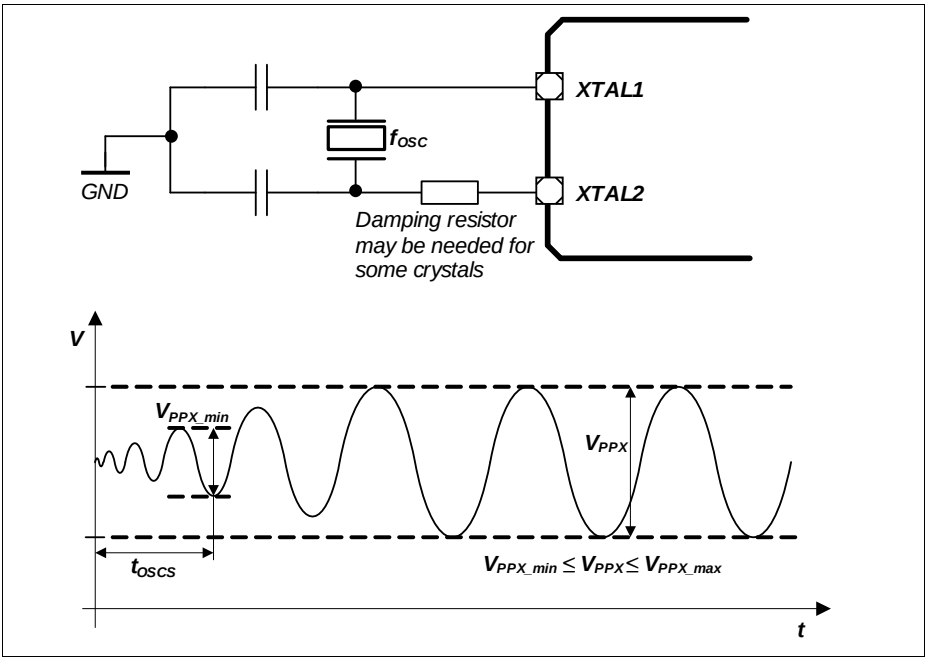

Figure 21 Oscillator in Crystal Mode

Table 42 Power Sequencing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Positive Load Step Current	ΔI_{PLS} SR	-	–	50	mA	Load increase on V_{DDP} $\Delta t \leq 10$ ns
Negative Load Step Current	ΔI_{NLS} SR	-	–	150	mA	Load decrease on V_{DDP} $\Delta t \leq 10$ ns
V_{DDC} Voltage Over- / Undershoot from Load Step	ΔV_{LS} CC	-	–	±100	mV	For maximum positive or negative load step
Positive Load Step Settling Time	t_{PLSS} SR	50	–	-	µs	
Negative Load Step Settling Time	t_{NLSS} SR	100	–	-	µs	
External Buffer Capacitor on V_{DDC}	C_{EXT} SR	3	4.7	6	µF	In addition C = 100 nF capacitor on each V_{DDC} pin

Positive Load Step Examples

System assumptions:
$f_{CPU} = f_{SYS}$, target frequency f_{CPU} = 80 MHz, main PLL f_{VCO} = 480 MHz, stepping done by K2 divider, t_{PLSS} between individual steps:

24 MHz - 48 MHz - 80 MHz (K2 steps 20 - 10 - 6)
24 MHz - 60 MHz - 80 MHz (K2 steps 20 - 8 - 6)

3.3.5 Internal Clock Source Characteristics

Fast Internal Clock Source

Table 44 Fast Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal frequency	f_{OFINC} CC	–	36.5	–	MHz	not calibrated
		–	24	–	MHz	calibrated
Accuracy	Δf_{OFI} CC	-0.5	–	0.5	%	automatic calibration[1)2)]
		-15	–	15	%	factory calibration, V_{DDP} = 3.3 V
		-25	–	25	%	no calibration, V_{DDP} = 3.3 V
		-7	–	7	%	Variation over voltage range[3)] 3.13 V ≤ V_{DDP} ≤ 3.63 V
Start-up time	t_{OFIS} CC	–	50	–	µs	

1) Error in addition to the accuracy of the reference clock.

2) Automatic calibration compensates variations of the temperature and in the V_{DDP} supply voltage.

3) Deviations from the nominal V_{DDP} voltage induce an additional error to the uncalibrated and/or factory calibrated oscillator frequency.

Slow Internal Clock Source

Table 45 Slow Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal frequency	f_{OSI} CC	–	32.768	–	kHz	
Accuracy	Δf_{OSI} CC	-4	–	4	%	V_{BAT} = const. 0 °C ≤ T_A ≤ 85 °C
		-5	–	5	%	V_{BAT} = const. T_A < 0 °C or T_A > 85 °C
		-5	–	5	%	2.4 V ≤ V_{BAT}, T_A = 25 °C
		-10	–	10	%	1.95 V ≤ V_{BAT} < 2.4 V, T_A = 25 °C
Start-up time	t_{OSIS} CC	–	50	–	µs	

4.2 Package Outlines

The availability of different packages for different devices types is listed in **Table 1**, specific packages for different device markings are listed in **Table 2**.

The exposed die pad dimensions are listed in **Table 55**.

Table 56 Differences PG-LQFP-64-19 to PG-TQFP-64-19

Change	PG-LQFP-64-19	PG-TQFP-64-19
Thermal Resistance Junction Ambient ($R_{\Theta JA}$)	30 K/W	23.4 K/W
Package thickness	$1.4^{\pm 0.05}$ mm	$1.0^{\pm 0.05}$ mm
	1.6 mm MAX	1.2 mm MAX
Exposed Die Pad size	5.8 mm × 5.8 mm	5.7 mm × 5.7 mm