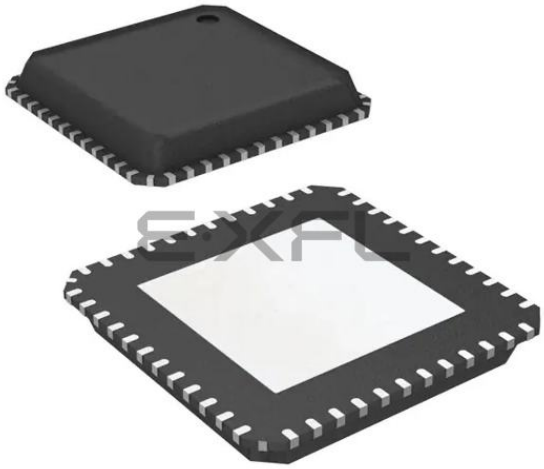
# Infineon Technologies - XMC4100Q48K128BAXUMA1 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | CANbus, I²C, LINbus, SPI, UART/USART, USB |
| Peripherals | DMA, I²S, LED, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 20K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.13V ~ 3.63V |
| Data Converters | A/D 9x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-VFQFN Exposed Pad |
| Supplier Device Package | PG-VQFN-48-53 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xmc4100q48k128baxuma1 |

**Table 9 XMC4100 Identification Registers**

| Register Name | Value | Marking |
|---|---|---|
| SCU_IDCHIP | 0004 2001$_H$ | EES-AA, ES-AA |
| SCU_IDCHIP | 0004 2002$_H$ | ES-AB, AB |
| SCU_IDCHIP | 0004 1003$_H$ | BA |
| JTAG IDCODE | 101D D083$_H$ | EES-AA, ES-AA |
| JTAG IDCODE | 201D D083$_H$ | ES-AB, AB |
| JTAG IDCODE | 301D D083$_H$ | BA |

### 2.2.1 Package Pin Summary

The following general scheme is used to describe each pin:

**Table 10 Package Pin Mapping Description**

| Function | Package A | Package B | ... | Pad Type | Notes |
|---|---|---|---|---|---|
| Name | N | Ax | ... | A1+ | |

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the dedicated pins (i.e. PORST) and supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type (A1, A1+, special=special pad, In=input pad, AN/DIG_IN=analog and digital input, Power=power supply). Details about the pad properties are defined in the Electrical Parameters.

In the “Notes”, special information to the respective pin/function is given, i.e. deviations from the default configuration after reset. Per default the regular Port pins are configured as direct input with no internal pull device active.

**Table 11 Package Pin Mapping**

| Function | LQFP-64 TQFP-64 | VQFN-48 | Pad Type | Notes |
|---|---|---|---|---|
| P0.0 | 2 | 2 | A1+ | |
| P0.1 | 1 | 1 | A1+ | |
| P0.2 | 64 | 48 | A1+ | |
| P0.3 | 63 | 47 | A1+ | |
| P0.4 | 62 | 46 | A1+ | |
| P0.5 | 61 | 45 | A1+ | |
| P0.6 | 60 | 44 | A1+ | |
| P0.7 | 58 | 43 | A1+ | After a system reset, via HWSEL this pin selects the DB.TDI function. |
| P0.8 | 57 | 42 | A1+ | After a system reset, via HWSEL this pin selects the DB.TRST function, with a weak pull-down active. |
| P0.9 | 4 | - | A1+ | |
| P0.10 | 3 | - | A1+ | |

**Table 11 Package Pin Mapping** (cont'd)

| Function | LQFP-64 TQFP-64 | VQFN-48 | Pad Type | Notes |
|---|---|---|---|---|
| P14.9 | 23 | 19 | AN/DAC/DIG_IN | |
| P14.14 | 14 | - | AN/DIG_IN | |
| USB_DP | 7 | 4 | special | |
| USB_DM | 6 | 3 | special | |
| HIB_IO_0 | 10 | 7 | A1 special | At the first power-up and with every reset of the hibernate domain this pin is configured as open-drain output and drives "0".<br>As output the medium driver mode is active. |
| TCK | 45 | 34 | A1 | Weak pull-down active. |
| TMS | 44 | 33 | A1+ | Weak pull-up active.<br>As output the strong-soft driver mode is active. |
| $\overline{\text{PORST}}$ | 43 | 32 | special | Strong pull-down controlled by EVR.<br>Weak pull-up active while strong pull-down is not active. |
| XTAL1 | 39 | 29 | clock_IN | |
| XTAL2 | 40 | 30 | clock_O | |
| RTC_XTAL1 | 11 | 8 | clock_IN | |
| RTC_XTAL2 | 12 | 9 | clock_O | |
| VBAT | 13 | 10 | Power | When VDDP is supplied VBAT has to be supplied as well. |
| VDDA/VAREF | 22 | 18 | AN_Power/AN_ Ref | Shared analog supply and reference voltage pin. |
| VSSA/VAGND | 21 | 17 | AN_Power/AN_ Ref | Shared analog supply and reference ground pin. |
| VDDC | 9 | 6 | Power | |
| VDDC | 42 | 31 | Power | |
| VDDP | 8 | 5 | Power | |
| VDDP | 38 | 28 | Power | |
| VDDP | 56 | 41 | Power | |
| VSS | 37 | 27 | Power | |

The XMC4[12]00 has a common ground concept, all $V_{SS}$, $V_{SSA}$ and $V_{SSO}$ pins share the same ground potential. In packages with an exposed die pad it must be connected to the common ground as well.

There are no dedicated connections for the analog reference $V_{AREF}$ and $V_{AGND}$. Instead, they share the same pins as the analog supply pins $V_{DDA}$ and $V_{SSA}$.Some analog channels can optionally serve as “Alternate Reference”; further details on this operating mode are described in the Reference Manual.

When $V_{DDP}$ is supplied, $V_{BAT}$ must be supplied as well. If no other supply source (e.g. battery) is connected to $V_{BAT}$, the $V_{BAT}$ pin can also be connected directly to $V_{DDP}$.

### 3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 14 Absolute Maximum Rating Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Storage temperature | $T_{ST}$ | SR | -65 | – | 150 | °C | – |
| Junction temperature | $T_J$ | SR | -40 | – | 150 | °C | – |
| Voltage at 3.3 V power supply pins with respect to $V_{SS}$ | $V_{DDP}$ | SR | – | – | 4.3 | V | – |
| Voltage on any Class A and dedicated input pin with respect to $V_{SS}$ | $V_{IN}$ | SR | -1.0 | – | $V_{DDP}$ + 1.0 or max. 4.3 | V | whichever is lower |
| Voltage on any analog input pin with respect to $V_{AGND}$ | $V_{AIN}$<br>$V_{AREF}$ | SR | -1.0 | – | $V_{DDP}$ + 1.0 or max. 4.3 | V | whichever is lower |
| Input current on any pin during overload condition | $I_{IN}$ | SR | -10 | – | +10 | mA | |
| Absolute maximum sum of all input circuit currents for one port group during overload condition[1)] | $\Sigma I_{IN}$ | SR | -25 | – | +25 | mA | |
| Absolute maximum sum of all input circuit currents during overload condition | $\Sigma I_{IN}$ | SR | -100 | – | +100 | mA | |

1) The port groups are defined in **Table 18**.

### 3.1.4 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in the **Section 3.2.1**.

**Table 19 Pad Driver and Pad Classes Overview**

| Class | Power Supply | Type | Sub-Class | Speed Grade | Load | Termination |
|---|---|---|---|---|---|---|
| **A** | 3.3 V | LVTTL I/O, LVTTL outputs | **A1** (e.g. GPIO) | 6 MHz | 100 pF | No |
| | | | **A1+** (e.g. serial I/Os) | 25 MHz | 50 pF | Series termination recommended |

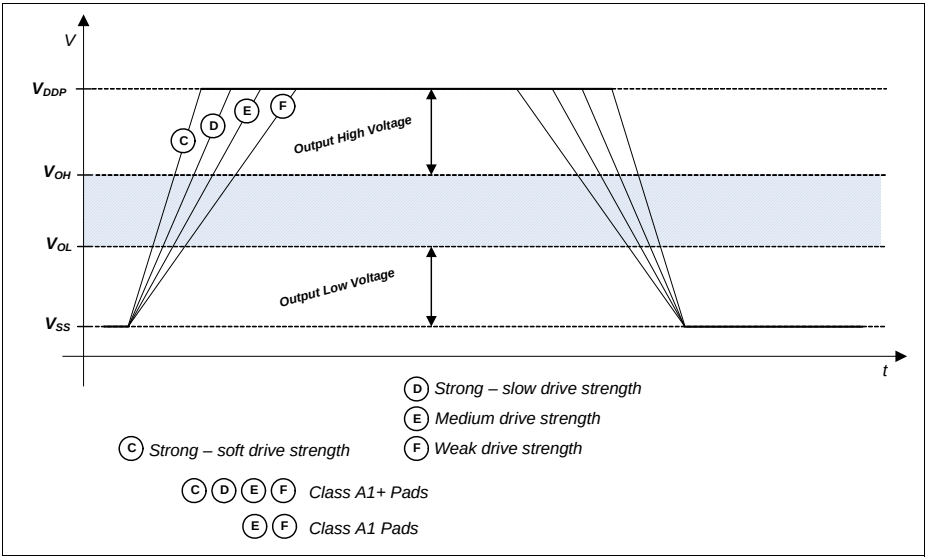


**Figure 10 Output Slopes with different Pad Driver Modes**

**Figure 10** is a qualitative display of the resulting output slope performance with different output driver modes. The detailed input and output characteristics are listed in **Section 3.2.1**.

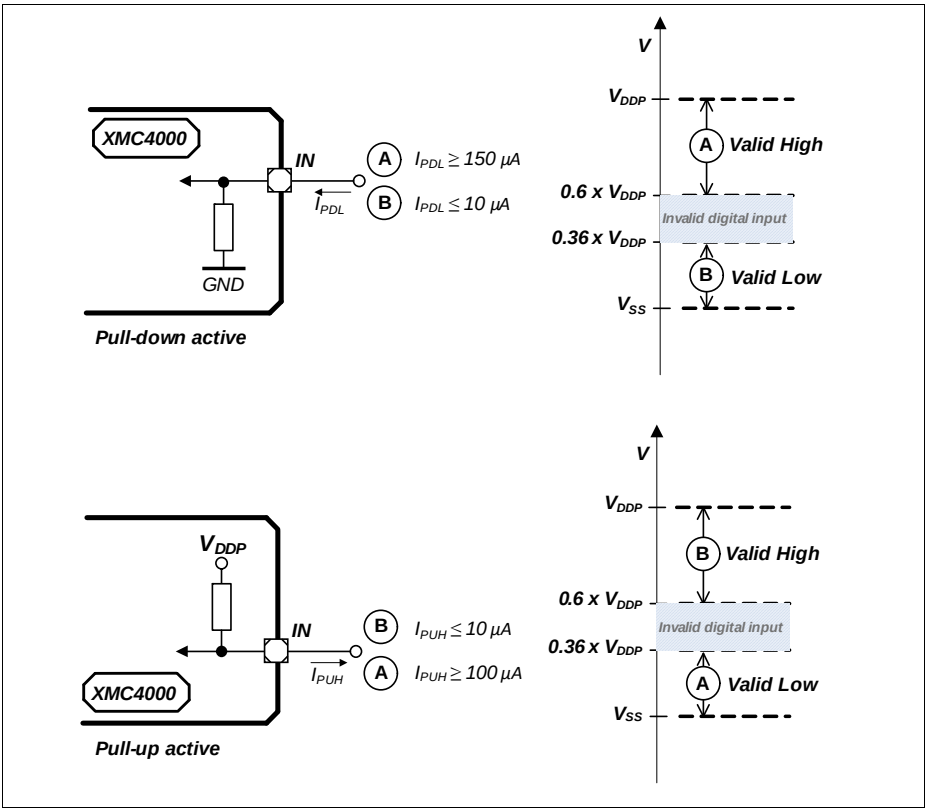


**Figure 11 Pull Device Input Characteristics**

**Figure 11** visualizes the input characteristics with an active internal pull device:

- in the cases “A” the internal pull device is overridden by a strong external driver;
- in the cases “B” the internal pull device defines the input logical state against a weak external load.

**Table 22 Standard Pads Class_A1**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | | Max. | | |
| Input leakage current | $I_{OZA1}$ CC | -500 | | 500 | nA | 0 V ≤ $V_{IN}$ ≤ $V_{DDP}$ |
| Input high voltage | $V_{IHA1}$ SR | 0.6 × $V_{DDP}$ | | $V_{DDP}$ + 0.3 | V | max. 3.6 V |
| Input low voltage | $V_{ILA1}$ SR | -0.3 | | 0.36 × $V_{DDP}$ | V | |
| Output high voltage, POD[1] = weak | $V_{OHA1}$ CC | $V_{DDP}$ - 0.4 | | – | V | $I_{OH}$ ≥ -400 µA |
| | | 2.4 | | – | V | $I_{OH}$ ≥ -500 µA |
| Output high voltage, POD[1] = medium | | $V_{DDP}$ - 0.4 | | – | V | $I_{OH}$ ≥ -1.4 mA |
| | | 2.4 | | – | V | $I_{OH}$ ≥ -2 mA |
| Output low voltage | $V_{OLA1}$ CC | – | | 0.4 | V | $I_{OL}$ ≤ 500 µA; POD[1] = weak |
| | | – | | 0.4 | V | $I_{OL}$ ≤ 2 mA; POD[1] = medium |
| Fall time | $t_{FA1}$ CC | – | | 150 | ns | $C_L$ = 20 pF; POD[1] = weak |
| | | – | | 50 | ns | $C_L$ = 50 pF; POD[1] = medium |
| Rise time | $t_{RA1}$ CC | – | | 150 | ns | $C_L$ = 20 pF; POD[1] = weak |
| | | – | | 50 | ns | $C_L$ = 50 pF; POD[1] = medium |

1) POD = Pin Out Driver

**Table 23 Standard Pads Class_A1+**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | | Max. | | |
| Input leakage current | $I_{OZA1+}$ CC | -1 | | 1 | µA | 0 V ≤ $V_{IN}$ ≤ $V_{DDP}$ |
| Input high voltage | $V_{IHA1+}$ SR | 0.6 × $V_{DDP}$ | | $V_{DDP}$ + 0.3 | V | max. 3.6 V |
| Input low voltage | $V_{ILA1+}$ SR | -0.3 | | 0.36 × $V_{DDP}$ | V | |

**Table 24 HIB_IO Class_A1 special Pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | | Max. | | |
| Input leakage current | $I_{OZHIB}$ CC | -500 | | 500 | nA | $0\ V \le V_{IN} \le V_{BAT}$ |
| Input high voltage | $V_{IHHIB}$ SR | $0.6 \times V_{BAT}$ | | $V_{BAT}$ + 0.3 | V | max. 3.6 V |
| Input low voltage | $V_{ILHIB}$ SR | -0.3 | | $0.36 \times V_{BAT}$ | V | |
| Input Hysteresis for HIB_IO pins[1] | $HYSHIB$ CC | $0.1 \times V_{BAT}$ | | – | V | $V_{BAT} \ge 3.13$ V |
| | | $0.06 \times V_{BAT}$ | | – | V | $V_{BAT} < 3.13$ V |
| Output high voltage, POD[1] = medium | $V_{OHHIB}$ CC | $V_{BAT}$ - 0.4 | | – | V | $I_{OH} \ge$ -1.4 mA |
| Output low voltage | $V_{OLHIB}$ CC | – | | 0.4 | V | $I_{OL} \le 2$ mA |
| Fall time | $t_{FHIB}$ CC | – | | 50 | ns | $V_{BAT} \ge 3.13$ V, $C_L = 50$ pF |
| | | – | | 100 | ns | $V_{BAT} < 3.13$ V, $C_L = 50$ pF |
| Rise time | $t_{RHIB}$ CC | – | | 50 | ns | $V_{BAT} \ge 3.13$ V, $C_L = 50$ pF |
| | | – | | 100 | ns | $V_{BAT} < 3.13$ V, $C_L = 50$ pF |

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

**Table 25 ADC Parameters** (Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Total capacitance of the alternate reference inputs[5] | $C_{AREFTOT}$ CC | – | 20 | 40 | pF | |
| Total Unadjusted Error | $TUE$ CC | -6 | – | 6 | LSB | 12-bit resolution; $V_{DDA}$ = 3.3 V; $V_{AREF} = V_{DDA}$[7] |
| Differential Non-Linearity Error[8] | $EA_{DNL}$ CC | -4.5 | – | 4.5 | LSB | |
| Gain Error[8] | $EA_{GAIN}$ CC | -6 | – | 6 | LSB | |
| Integral Non-Linearity[8] | $EA_{INL}$CC | -4.5 | – | 4.5 | LSB | |
| Offset Error[8] | $EA_{OFF}$ CC | -6 | – | 6 | LSB | |
| Worst case ADC $V_{DDA}$ power supply current per active converter | $I_{DDAA}$ CC | – | 1.5 | 2 | mA | during conversion $V_{DDP}$ = 3.6 V, $T_J$ = 150 °C |
| Charge consumption on alternate reference per conversion[5] | $Q_{CONV}$ CC | – | 30 | – | pC | 0 V ≤ $V_{AREF}$ ≤ $V_{DDA}$[9] |
| ON resistance of the analog input path | $R_{AIN}$ CC | – | 600 | 1 200 | Ohm | |
| ON resistance for the ADC test (pull down for AIN7) | $R_{AIN7T}$ CC | 180 | 550 | 900 | Ohm | |

1) A running conversion may become imprecise in case the normal conditions are violated (voltage overshoot).
2) If the analog reference voltage is below $V_{DDA}$, then the ADC converter errors increase. If the reference voltage is reduced by the factor k (k<1), TUE, DNL, INL, Gain, and Offset errors increase also by the factor 1/k.
3) The leakage current definition is a continuous function, as shown in figure ADCx Analog Inputs Leakage. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function (see **Figure 14**).
4) The sampling capacity of the conversion C-network is pre-charged to $V_{AREF}$/2 before the sampling moment. Because of the parasitic elements, the voltage measured at AINx can deviate from $V_{AREF}$/2.
5) Applies to AINx, when used as alternate reference input.
6) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead, smaller capacitances are successively switched to the reference voltage.
7) For 10-bit conversions, the errors are reduced to 1/4; for 8-bit conversions, the errors are reduced to 1/16. Never less than ±1 LSB.
8) The sum of DNL/INL/GAIN/OFF errors does not exceed the related total unadjusted error TUE.

### 3.2.3 Digital to Analog Converters (DACx)

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 27 DAC Parameters** (Operating Conditions apply)

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| RMS supply current | $I_{DD}$ | CC | – | 2.5 | 4 | mA | per active DAC channel, without load currents of DAC outputs |
| Resolution | $RES$ | CC | – | 12 | – | Bit | |
| Update rate | $f_{URATE\_A}$ | CC | – | | 2 | Msample/s | data rate, where DAC can follow 64 LSB code jumps to ± 1LSB accuracy |
| Update rate | $f_{URATE\_F}$ | CC | – | | 5 | Msample/s | data rate, where DAC can follow 64 LSB code jumps to ± 4 LSB accuracy |
| Settling time | $t_{SETTLE}$ | CC | – | 1 | 2 | µs | at full scale jump, output voltage reaches target value ± 20 LSB |
| Slew rate | $SR$ | CC | 2 | 5 | – | V/µs | |
| Minimum output voltage | $V_{OUT\_MIN}$ | CC | – | 0.3 | – | V | code value unsigned: $000_H$; signed: $800_H$ |
| Maximum output voltage | $V_{OUT\_MAX}$ | CC | – | 2.5 | – | V | code value unsigned: $FFF_H$; signed: $7FF_H$ |
| Integral non-linearity[1)] | $INL$ | CC | -5.5 | ±2.5 | 5.5 | LSB | $R_L \geq 5$ kOhm, $C_L \leq 50$ pF |
| Differential non-linearity | $DNL$ | CC | -2 | ±1 | 2 | LSB | $R_L \geq 5$ kOhm, $C_L \leq 50$ pF |

### 3.2.4 Out-of-Range Comparator (ORC)

The Out-of-Range Comparator (ORC) triggers on analog input voltages ($V_{AIN}$) above the analog reference[1] ($V_{AREF}$) on selected input pins (GxORCy) and generates a service request trigger (GxORCOUTy).

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

The parameters in **Table 28** apply for the maximum reference voltage $V_{AREF} = V_{DDA} + 50$ mV.

**Table 28 ORC Parameters** (Operating Conditions apply)

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| DC Switching Level | $V_{ODC}$ | CC | 100 | 125 | 200 | mV | Ax-marking devices $V_{AIN} \geq V_{AREF} + V_{ODC}$ |
| Hysteresis | $V_{OHYS}$ | CC | 50 | – | $V_{ODC}$ | mV | |
| Detection Delay of a persistent Overvoltage | $t_{ODD}$ | CC | 55 | – | 450 | ns | Ax-marking devices $V_{AIN} \geq V_{AREF} + 200$ mV |
| | | | 45 | – | 105 | ns | $V_{AIN} \geq V_{AREF} + 400$ mV |
| Always detected Overvoltage Pulse | $t_{OPDD}$ | CC | 440 | – | – | ns | Ax-marking devices $V_{AIN} \geq V_{AREF} + 200$ mV |
| | | | 90 | – | – | ns | $V_{AIN} \geq V_{AREF} + 400$ mV |
| Never detected Overvoltage Pulse | $t_{OPDN}$ | CC | – | – | 49 | ns | Ax-marking devices $V_{AIN} \geq V_{AREF} + 200$ mV |
| | | | – | – | 30 | ns | $V_{AIN} \geq V_{AREF} + 400$ mV |
| Release Delay | $t_{ORD}$ | CC | 65 | – | 105 | ns | $V_{AIN} \leq V_{AREF}$ |
| Enable Delay | $t_{OED}$ | CC | – | 100 | 200 | ns | |

1) Always the standard VADC reference, alternate references do not apply to the ORC.

**Table 30 CMP and 10-bit DAC characteristics** (Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| CSG Output Jitter | $D_{CSG}$ CC | – | – | 1 | clk | |
| Bias startup time | $t_{start}$ CC | – | – | 98 | us | |
| Bias supply current | $I_{DDbias}$ CC | – | – | 400 | µA | |
| CSGy startup time | $t_{CSGS}$ CC | – | – | 2 | µs | |
| Input operation current[1] | $I_{DDCIN}$ CC | -10 | – | 33 | µA | See **Figure 19** |
| High Speed Mode | | | | | | |
| DAC output voltage range | $V_{DOUT}$ CC | $V_{SS}$ | – | $V_{DDP}$ | V | |
| DAC propagation delay - Full scale | $t_{FShs}$ CC | – | – | 80 | ns | See **Figure 20** |
| Input Selector propagation delay - Full scale | $t_{Dhs}$ CC | – | – | 100 | ns | See **Figure 20** |
| Comparator bandwidth | $t_{Dhs}$ CC | 20 | – | – | ns | |
| DAC CLK frequency | $f_{clk}$ SR | – | – | 30 | MHz | |
| Supply current | $I_{DDhs}$ CC | – | – | 940 | µA | |
| Low Speed Mode | | | | | | |
| DAC output voltage range | $V_{DOUT}$ CC | 0.1 × $V_{DDP}$[2] | – | $V_{DDP}$ | V | |
| DAC propagation delay - Full Scale | $t_{FSls}$ CC | – | – | 160 | ns | See **Figure 20** |
| Input Selector propagation delay - Full Scale | $t_{Dls}$ CC | – | – | 200 | ns | See **Figure 20** |
| Comparator bandwidth | $t_{Dls}$ CC | 20 | – | – | ns | |
| DAC CLK frequency | $f_{clk}$ SR | – | – | 30 | MHz | |
| Supply current | $I_{DDls}$ CC | – | – | 300 | µA | |

1) Typical input resistance $R_{CIN}$ = 100kOhm.

2) The INL error increases for DAC output voltages below this limit.

**Table 32 External clock operating conditions**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Frequency | $f_{eclk}$ | SR | – | – | $f_{hrpwm}/4$ | MHz | |
| ON time | $t_{oneclk}$ | SR | $2T_{ccu}$ [1)2)] | – | – | ns | |
| OFF time | $t_{offeclk}$ | SR | $2T_{ccu}$ [1)2)] | – | – | ns | Only the rising edge is used |

1) 50% duty cycle is not obligatory

2) Only valid if the signal was not previously synchronized/generated with the fccu clock (or a synchronous clock)

### 3.2.6 Low Power Analog Comparator (LPAC)

The Low Power Analog Comparator (LPAC) triggers a wake-up event from Hibernate state or an interrupt trigger during normal operation. It does so by comparing $V_{BAT}$ or another external sensor voltage $V_{LPS}$ with a pre-programmed threshold voltage.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 33 Low Power Analog Comparator Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| $V_{BAT}$ supply voltage range for LPAC operation | $V_{BAT}$ | SR | 2.1 | – | 3.6 | V | |
| Sensor voltage range | $V_{LPCS}$ | CC | 0 | – | 1.2 | V | |
| Threshold step size | $V_{th}$ | CC | – | 18.75 | – | mV | |
| Threshold trigger accuracy | $\Delta V_{th}$ | CC | – | – | ±10 | % | for $V_{th}$ > 0.4 V |
| Conversion time | $t_{LPCC}$ | CC | – | – | 250 | µs | |
| Average current consumption over time | $I_{LPCAC}$ | CC | – | – | 15 | µA | conversion interval 10 ms[1)] |
| Current consumption during conversion | $I_{LPCC}$ | CC | – | 150 | – | µA | [1)] |

1) Single channel conversion, measuring $V_{BAT}$ = 3.3 V, 8 cycles settling time

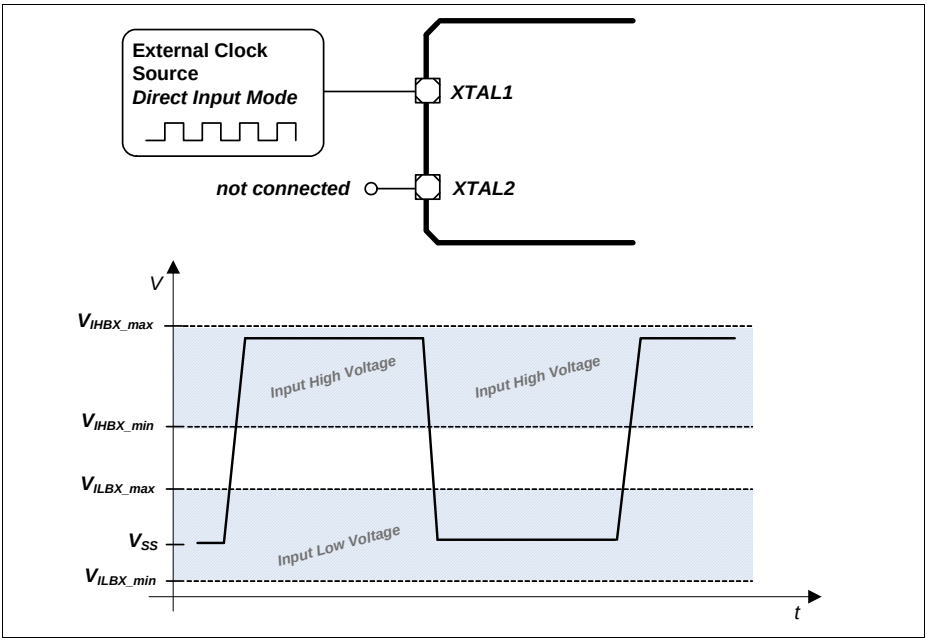


**Figure 22 Oscillator in Direct Input Mode**

### 3.3.2 Power-Up and Supply Monitoring

$\overline{\text{PORST}}$ is always asserted when $V_{DDP}$ and/or $V_{DDC}$ violate the respective thresholds.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

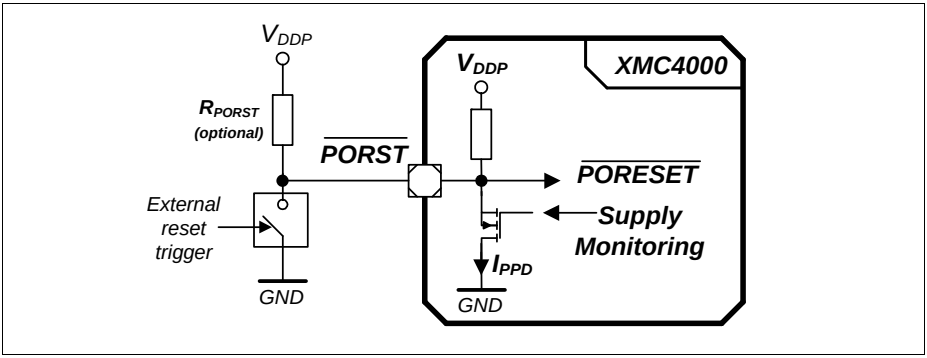


**Figure 26 $\overline{\text{PORST}}$ Circuit**

**Table 41 Supply Monitoring Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Digital supply voltage reset threshold | $V_{POR}$ CC | 2.79[1] | – | 3.05[2] | V | [3] |
| Core supply voltage reset threshold | $V_{PV}$ CC | – | – | 1.17 | V | |
| $V_{DDP}$ voltage to ensure defined pad states | $V_{DDPPA}$ CC | – | 1.0 | – | V | |
| $\overline{\text{PORST}}$ rise time | $t_{PR}$ SR | – | – | 2 | µs | |
| Startup time from power-on reset with code execution from Flash | $t_{SSW}$ CC | – | 2.5 | 3.5 | ms | Time to the first user code instruction |
| $V_{DDC}$ ramp up time | $t_{VCR}$ CC | – | 550 | – | µs | Ramp up after power-on or after a reset triggered by a violation of $V_{POR}$ or $V_{PV}$ |

1) Minimum threshold for reset assertion.

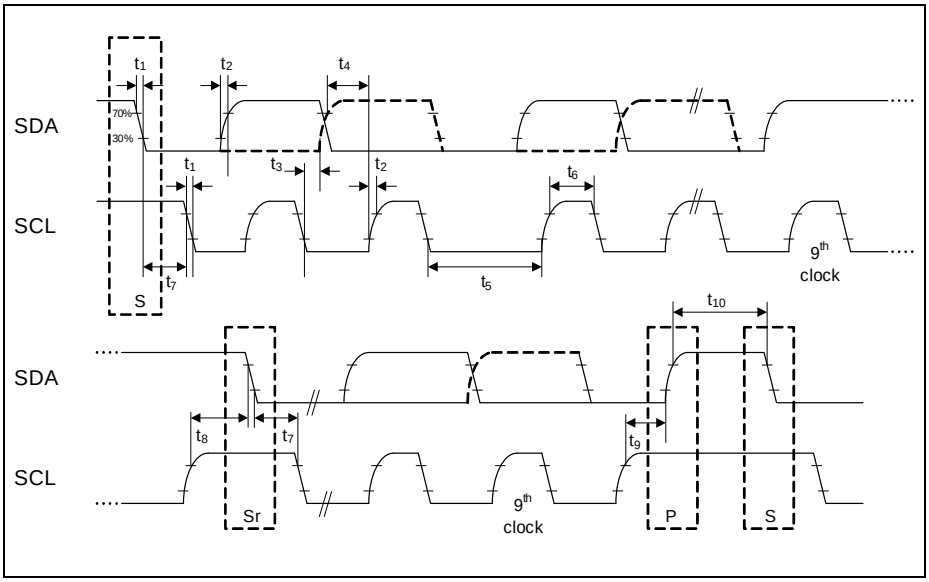


**Figure 32 USIC IIC Stand and Fast Mode Timing**

### 3.3.8.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

*Note: Operating Conditions apply.*

**Table 52 USIC IIS Master Transmitter Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Clock period | $t_1$ CC | 33.3 | – | – | ns | |
| Clock high time | $t_2$ CC | 0.35 x $t_{1min}$ | – | – | ns | |
| Clock low time | $t_3$ CC | 0.35 x $t_{1min}$ | – | – | ns | |
| Hold time | $t_4$ CC | 0 | – | – | ns | |
| Clock rise time | $t_5$ CC | – | – | 0.15 x $t_{1min}$ | ns | |

### 3.3.9 USB Interface Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification. High-Speed Mode is not supported.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 54 USB Timing Parameters** (operating conditions apply)

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Rise time | $t_R$ | CC | 4 | – | 20 | ns | $C_L$ = 50 pF |
| Fall time | $t_F$ | CC | 4 | – | 20 | ns | $C_L$ = 50 pF |
| Rise/Fall time matching | $t_R/t_F$ | CC | 90 | – | 111.11 | % | $C_L$ = 50 pF |
| Crossover voltage | $V_{CRS}$ | CC | 1.3 | – | 2.0 | V | $C_L$ = 50 pF |

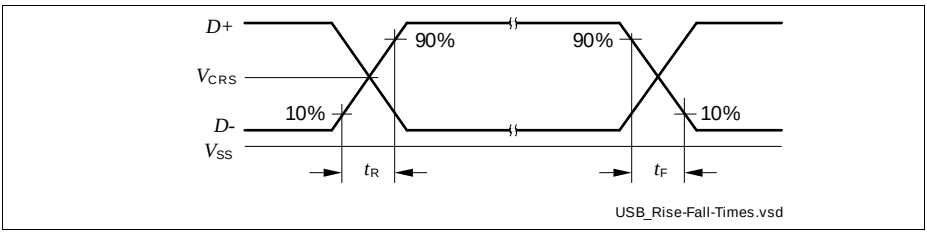


**Figure 35 USB Signal Timing**

power dissipation must be limited so that the average junction temperature does not exceed 150 °C.

The difference between junction temperature and ambient temperature is determined by
$\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers ($P_{IODYN}$) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce $V_{DDP}$, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

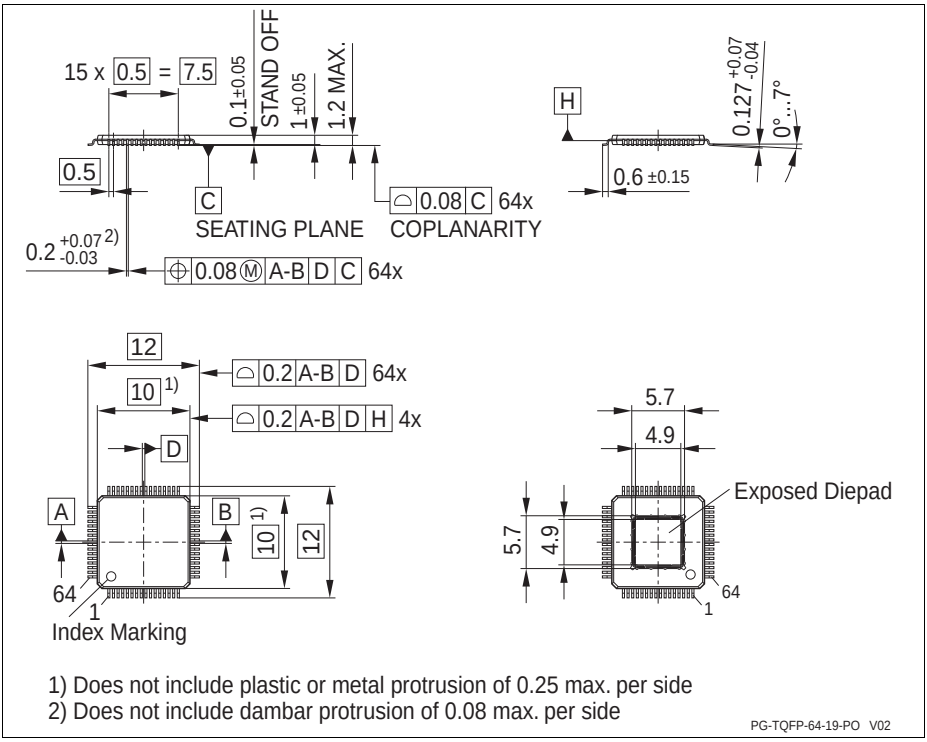


**Figure 37 PG-TQFP-64-19** (Plastic Green Thin Profile Quad Flat Package)

**Table 57 Differences PG-VQFN-48-53 to PG-VQFN-48-71**

| Change | PG-VQFN-48-53 | PG-VQFN-48-71 |
|---|---|---|
| Package corner | chamfered | right-angled |
| Lead width | $0.23^{\pm 0.05}$ mm | $0.25^{(+0.05, -0.07)}$ mm |
| Lead height | $0.4^{\pm 0.07}$ mm | $0.4^{\pm 0.05}$ mm |