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Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP Exposed Pad
Supplier Device Package	PG-TQFP-64-19
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4104f64f128baxqma1

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XMC4[12]00 Data Sheet

Revision History: V1.3 2015-10

Previous Versions:
V1.2 2014-06
V1.1 2014-03
V1.0 2013-10
V0.6 2012-11

Page	Subjects
12	Added a section listing the packages of the different markings.
14	Added BA marking variant.
14	Corrected SCU_IDCHIP value of XMC4100 EES-AA/ES-AA.
36	Added footnote explaining minimum V_{BAT} requirements to start the hibernate domain and/or oscillation of a crystal on RTC_XTAL.
37	Changed pull device definition to System Requirement (SR) to reflect that the specified currents are defined by the characteristics of the external load/driver.
37	Added information that $\overline{\text{PORST}}$ Pull-up is identical to the pull-up on standard I/O pins.
42	Updated C_{AINSW}, C_{AINTOT} and R_{AIN} parameters with improved values.
56	Added footnote on test configuration for LPAC measurement.
58	Corrected parameter name of of USB pull device (upstream port receiving) definition according to USB standard (referenced to DM instead of DP)
62	Relaxed RTC_XTAL V_{PPX} parameter value and changed it to a system requirement.
66	Added footnote on current consumption by enabling of f_{CCU}.
67	Added Flash endurance parameter for 64 Kbytes Physical Sector PS4 N_{EPS4} for devices with BA marking.
many	Added PG-TQFP-64-19 and PG-VQFN-48-71 package information.
89, 91	Added tables describing the differences between PG-LQFP-64-19 to PG-TQFP-64-19 as well as PG-VQFN-48-53 to PG-VQFN-48-71 packages.
93	Updated to JEDEC standard J-STD-020D for the moisture sensitivity level and added solder temperature parameter according to the same standard.

1.3 Package Variants

Different markings of the XMC4[12]00 use different package variants. Details of those packages are given in the **Package Parameters** section of the Data Sheet.

Table 2 XMC4[12]00 Package Variants

Package Variant	Marking	Package
XMC4[12]00-F64	EES-AA, ES-AA, ES-AB, AB	PG-LQFP-64-19
XMC4[12]00-Q48		PG-VQFN-48-53
XMC4[12]00-F64	BA	PG-TQFP-64-19
XMC4[12]00-Q48		PG-VQFN-48-71

1.4 Device Type Features

The following table lists the available features per device type.

Table 3 Features of XMC4[12]00 Device Types

Derivative[1)]	LEDTS Intf.	USB Intf.	USIC Chan.	MultiCAN Nodes, MO
XMC4200-F64x256	1	1	2 x 2	N0, N1 MO[0..63]
XMC4200-Q48x256	1	1	2 x 2	N0, N1 MO[0..63]
XMC4100-F64x128	1	1	2 x 2	N0, N1 MO[0..63]
XMC4100-Q48x128	1	1	2 x 2	N0, N1 MO[0..63]
XMC4104-F64x64	1	–	2 x 2	–
XMC4104-Q48x64	1	–	2 x 2	–
XMC4104-F64x128	1	–	2 x 2	–
XMC4104-Q48x128	1	–	2 x 2	–
XMC4108-F64x64	–	–	2 x 2	N0, MO[0..31]
XMC4108-Q48x64	–	–	2 x 2	N0, MO[0..31]

1) x is a placeholder for the supported temperature range.

Table 6 SRAM Memory Ranges

Total SRAM Size	Program SRAM	System Data SRAM
40 Kbytes	1FFF C000$_H$ – 1FFF FFFF$_H$	2000 0000$_H$ – 2000 5FFF$_H$
20 Kbytes	1FFF E000$_H$ – 1FFF FFFF$_H$	2000 0000$_H$ – 2000 2FFF$_H$

Table 7 ADC Channels[1)]

Package	VADC G0	VADC G1
LQFP-64, TQFP-64	CH0, CH3..CH7	CH0, CH1, CH3, CH6
PG-VQFN-48	CH0, CH3..CH7	CH0, CH1, CH3

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

1.6 Identification Registers

The identification registers allow software to identify the marking.

Table 8 XMC4200 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	0004 2001$_H$	EES-AA, ES-AA
SCU_IDCHIP	0004 2002$_H$	ES-AB, AB
SCU_IDCHIP	0004 2003$_H$	BA
JTAG IDCODE	101D D083$_H$	EES-AA, ES-AA
JTAG IDCODE	201D D083$_H$	ES-AB, AB
JTAG IDCODE	301D D083$_H$	BA

Table 9 XMC4100 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	0004 2001$_H$	EES-AA, ES-AA
SCU_IDCHIP	0004 2002$_H$	ES-AB, AB
SCU_IDCHIP	0004 1003$_H$	BA
JTAG IDCODE	101D D083$_H$	EES-AA, ES-AA
JTAG IDCODE	201D D083$_H$	ES-AB, AB
JTAG IDCODE	301D D083$_H$	BA

2.2.1 Package Pin Summary

The following general scheme is used to describe each pin:

Table 10 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type	Notes
Name	N	Ax	...	A1+	

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the dedicated pins (i.e. PORST) and supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type (A1, A1+, special=special pad, In=input pad, AN/DIG_IN=analog and digital input, Power=power supply). Details about the pad properties are defined in the Electrical Parameters.

In the “Notes”, special information to the respective pin/function is given, i.e. deviations from the default configuration after reset. Per default the regular Port pins are configured as direct input with no internal pull device active.

Table 11 Package Pin Mapping

Function	LQFP-64 TQFP-64	VQFN-48	Pad Type	Notes
P0.0	2	2	A1+	
P0.1	1	1	A1+	
P0.2	64	48	A1+	
P0.3	63	47	A1+	
P0.4	62	46	A1+	
P0.5	61	45	A1+	
P0.6	60	44	A1+	
P0.7	58	43	A1+	After a system reset, via HWSEL this pin selects the DB.TDI function.
P0.8	57	42	A1+	After a system reset, via HWSEL this pin selects the DB.TRST function, with a weak pull-down active.
P0.9	4	-	A1+	
P0.10	3	-	A1+	

The XMC4[12]00 has a common ground concept, all V_{SS}, V_{SSA} and V_{SSO} pins share the same ground potential. In packages with an exposed die pad it must be connected to the common ground as well.

There are no dedicated connections for the analog reference V_{AREF} and V_{AGND}. Instead, they share the same pins as the analog supply pins V_{DDA} and V_{SSA}.Some analog channels can optionally serve as “Alternate Reference”; further details on this operating mode are described in the Reference Manual.

When V_{DDP} is supplied, V_{BAT} must be supplied as well. If no other supply source (e.g. battery) is connected to V_{BAT}, the V_{BAT} pin can also be connected directly to V_{DDP}.

3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 15 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
  - pad supply levels (V_{DDP} or V_{DDA})
  - temperature

If a pin current is outside of the **Operating Conditions** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

Table 15 Overload Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Input current on any port pin during overload condition	I_{OV}	SR	-5	–	5	mA	
Absolute sum of all input circuit currents for one port group during overload condition[1)]	I_{OVG}	SR	–	–	20	mA	$\Sigma\|I_{OVx}\|$, for all $I_{OVx} < 0$ mA
			–	–	20	mA	$\Sigma\|I_{OVx}\|$, for all $I_{OVx} > 0$ mA
Absolute sum of all input circuit currents during overload condition	I_{OVS}	SR	–	–	80	mA	ΣI_{OVG}

1) The port groups are defined in **Table 18**.

Figure 9 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

Table 22 Standard Pads Class_A1

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Input leakage current	I_{OZA1} CC	-500		500	nA	0 V ≤ V_{IN} ≤ V_{DDP}
Input high voltage	V_{IHA1} SR	0.6 × V_{DDP}		V_{DDP} + 0.3	V	max. 3.6 V
Input low voltage	V_{ILA1} SR	-0.3		0.36 × V_{DDP}	V	
Output high voltage, POD[1] = weak	V_{OHA1} CC	V_{DDP} - 0.4		–	V	I_{OH} ≥ -400 µA
		2.4		–	V	I_{OH} ≥ -500 µA
Output high voltage, POD[1] = medium		V_{DDP} - 0.4		–	V	I_{OH} ≥ -1.4 mA
		2.4		–	V	I_{OH} ≥ -2 mA
Output low voltage	V_{OLA1} CC	–		0.4	V	I_{OL} ≤ 500 µA; POD[1] = weak
		–		0.4	V	I_{OL} ≤ 2 mA; POD[1] = medium
Fall time	t_{FA1} CC	–		150	ns	C_L = 20 pF; POD[1] = weak
		–		50	ns	C_L = 50 pF; POD[1] = medium
Rise time	t_{RA1} CC	–		150	ns	C_L = 20 pF; POD[1] = weak
		–		50	ns	C_L = 50 pF; POD[1] = medium

1) POD = Pin Out Driver

Table 23 Standard Pads Class_A1+

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Input leakage current	I_{OZA1+} CC	-1		1	µA	0 V ≤ V_{IN} ≤ V_{DDP}
Input high voltage	V_{IHA1+} SR	0.6 × V_{DDP}		V_{DDP} + 0.3	V	max. 3.6 V
Input low voltage	V_{ILA1+} SR	-0.3		0.36 × V_{DDP}	V	

3.2.3 Digital to Analog Converters (DACx)

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 27 DAC Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
RMS supply current	I_{DD}	CC	–	2.5	4	mA	per active DAC channel, without load currents of DAC outputs
Resolution	RES	CC	–	12	–	Bit	
Update rate	f_{URATE_A}	CC	–		2	Msample/s	data rate, where DAC can follow 64 LSB code jumps to ± 1LSB accuracy
Update rate	f_{URATE_F}	CC	–		5	Msample/s	data rate, where DAC can follow 64 LSB code jumps to ± 4 LSB accuracy
Settling time	t_{SETTLE}	CC	–	1	2	µs	at full scale jump, output voltage reaches target value ± 20 LSB
Slew rate	SR	CC	2	5	–	V/µs	
Minimum output voltage	V_{OUT_MIN}	CC	–	0.3	–	V	code value unsigned: 000_H; signed: 800_H
Maximum output voltage	V_{OUT_MAX}	CC	–	2.5	–	V	code value unsigned: FFF_H; signed: $7FF_H$
Integral non-linearity[1)]	INL	CC	-5.5	±2.5	5.5	LSB	$R_L \geq 5$ kOhm, $C_L \leq 50$ pF
Differential non-linearity	DNL	CC	-2	±1	2	LSB	$R_L \geq 5$ kOhm, $C_L \leq 50$ pF

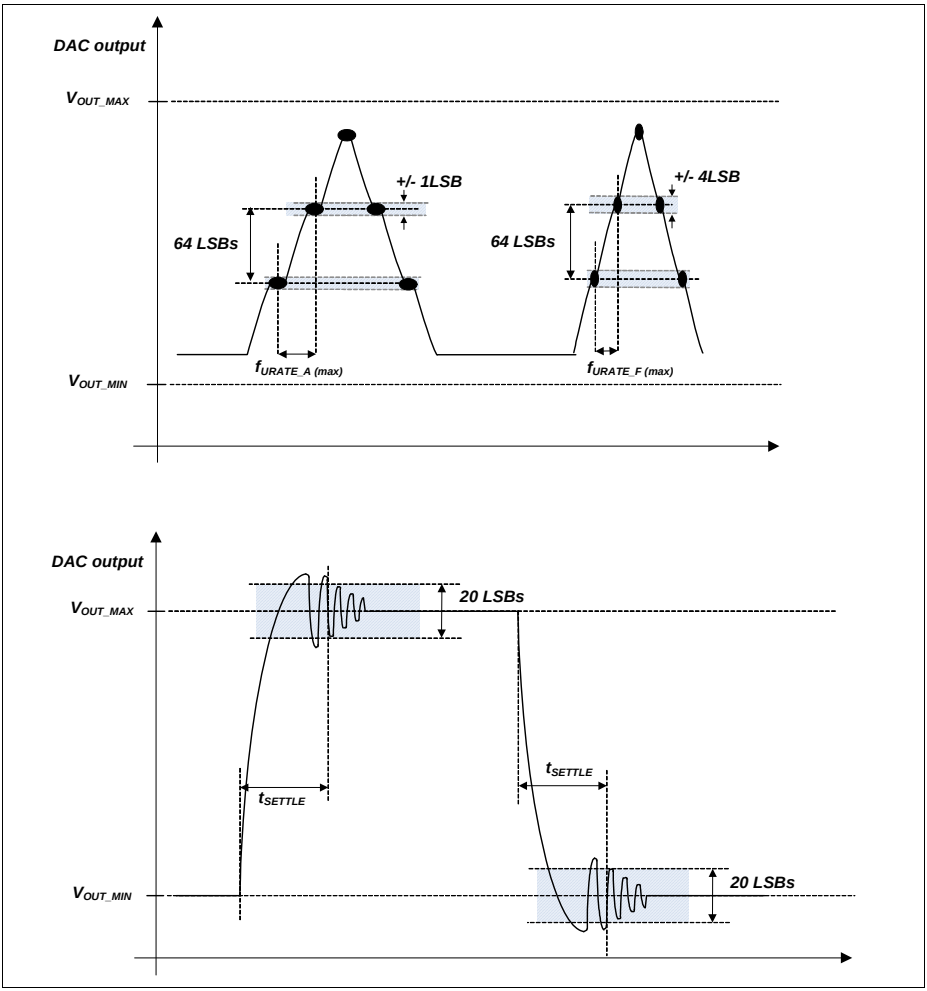

Figure 15 DAC Conversion Examples

3.2.4 Out-of-Range Comparator (ORC)

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above the analog reference[1] (V_{AREF}) on selected input pins (GxORCy) and generates a service request trigger (GxORCOUTy).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The parameters in **Table 28** apply for the maximum reference voltage $V_{AREF} = V_{DDA} + 50$ mV.

Table 28 ORC Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DC Switching Level	V_{ODC}	CC	100	125	200	mV	Ax-marking devices $V_{AIN} \geq V_{AREF} + V_{ODC}$
Hysteresis	V_{OHYS}	CC	50	–	V_{ODC}	mV	
Detection Delay of a persistent Overvoltage	t_{ODD}	CC	55	–	450	ns	Ax-marking devices $V_{AIN} \geq V_{AREF} + 200$ mV
			45	–	105	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Always detected Overvoltage Pulse	t_{OPDD}	CC	440	–	–	ns	Ax-marking devices $V_{AIN} \geq V_{AREF} + 200$ mV
			90	–	–	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Never detected Overvoltage Pulse	t_{OPDN}	CC	–	–	49	ns	Ax-marking devices $V_{AIN} \geq V_{AREF} + 200$ mV
			–	–	30	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Release Delay	t_{ORD}	CC	65	–	105	ns	$V_{AIN} \leq V_{AREF}$
Enable Delay	t_{OED}	CC	–	100	200	ns	

1) Always the standard VADC reference, alternate references do not apply to the ORC.

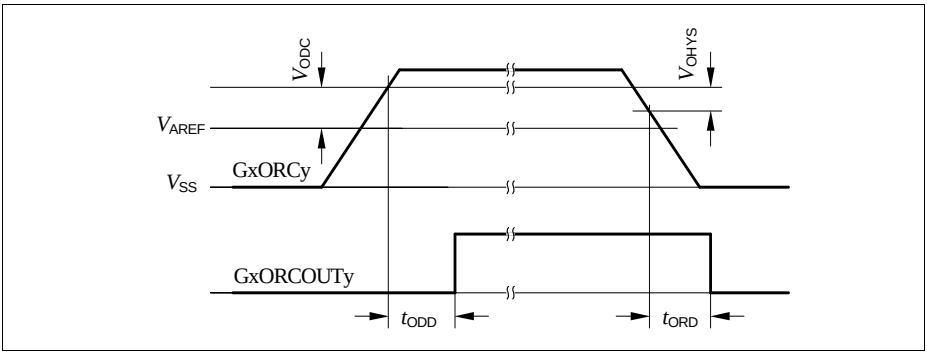

Figure 16 GxORCOUTy Trigger Generation

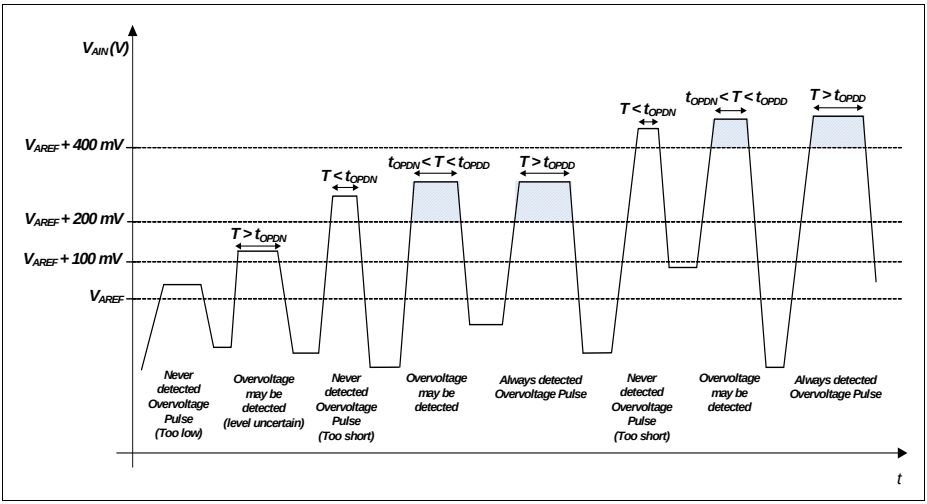

Figure 17 ORC Detection Ranges

Table 32 External clock operating conditions

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Frequency	f_{eclk}	SR	–	–	$f_{hrpwm}/4$	MHz	
ON time	t_{oneclk}	SR	$2T_{ccu}$ [1)2)]	–	–	ns	
OFF time	$t_{offeclk}$	SR	$2T_{ccu}$ [1)2)]	–	–	ns	Only the rising edge is used

1) 50% duty cycle is not obligatory

2) Only valid if the signal was not previously synchronized/generated with the fccu clock (or a synchronous clock)

3.2.6 Low Power Analog Comparator (LPAC)

The Low Power Analog Comparator (LPAC) triggers a wake-up event from Hibernate state or an interrupt trigger during normal operation. It does so by comparing V_{BAT} or another external sensor voltage V_{LPS} with a pre-programmed threshold voltage.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 33 Low Power Analog Comparator Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
V_{BAT} supply voltage range for LPAC operation	V_{BAT}	SR	2.1	–	3.6	V	
Sensor voltage range	V_{LPCS}	CC	0	–	1.2	V	
Threshold step size	V_{th}	CC	–	18.75	–	mV	
Threshold trigger accuracy	ΔV_{th}	CC	–	–	±10	%	for V_{th} > 0.4 V
Conversion time	t_{LPCC}	CC	–	–	250	µs	
Average current consumption over time	I_{LPCAC}	CC	–	–	15	µA	conversion interval 10 ms[1)]
Current consumption during conversion	I_{LPCC}	CC	–	150	–	µA	[1)]

1) Single channel conversion, measuring V_{BAT} = 3.3 V, 8 cycles settling time

3.2.8 USB Device Interface DC Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification. High-Speed Mode is not supported.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 35 USB Device Data Line (USB_DP, USB_DM) Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Input low voltage	V_{IL}	SR	–	–	0.8	V	
Input high voltage (driven)	V_{IH}	SR	2.0	–	–	V	
Input high voltage (floating) [1]	V_{IHZ}	SR	2.7	–	3.6	V	
Differential input sensitivity	V_{DIS}	CC	0.2	–	–	V	
Differential common mode range	V_{CM}	CC	0.8	–	2.5	V	
Output low voltage	V_{OL}	CC	0.0	–	0.3	V	1.5 kOhm pull-up to 3.6 V
Output high voltage	V_{OH}	CC	2.8	–	3.6	V	15 kOhm pull-down to 0 V
DP pull-up resistor (idle bus)	R_{PUI}	CC	900	–	1 575	Ohm	
DP pull-up resistor (upstream port receiving)	R_{PUA}	CC	1 425	–	3 090	Ohm	
Input impedance DP, DM	Z_{INP}	CC	300	–	–	kOhm	$0\ V \le V_{IN} \le V_{DDP}$
Driver output resistance DP, DM	Z_{DRV}	CC	28	–	44	Ohm	

1) Measured at A-connector with 1.5 kOhm ± 5% to 3.3 V ± 0.3 V connected to USB_DP or USB_DM and at B-connector with 15 kOhm ± 5% to ground connected to USB_DP and USB_DM.

3.2.10 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

If not stated otherwise, the operating conditions for the parameters in the following table are:
V_{DDP} = 3.3 V, T_A = 25 °C

Table 38 Power Supply Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Active supply current[1] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPA}	CC	–	80	–	mA	80 / 80 / 80
			–	75	–		80 / 40 / 40
			–	73	–		40 / 40 / 80
			–	59	–		24 / 24 / 24
			–	50	–		1 / 1 / 1
Active supply current Code execution from RAM Flash in Sleep mode Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPA}	CC	–	24	–	mA	80 / 80 / 80
			–	19	–		80 / 40 / 40
Active supply current[2] Peripherals disabled Frequency: f_{CPU} / f_{PERIPH} in MHz	I_{DDPA}	CC	–	63	–	mA	80 / 80 / 80
			–	62	–		80 / 40 / 40
			–	60	–		40 / 40 / 80
			–	54	–		24 / 24 / 24
			–	50	–		1 / 1 / 1

3.3.5 Internal Clock Source Characteristics

Fast Internal Clock Source

Table 44 Fast Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal frequency	f_{OFINC} CC	–	36.5	–	MHz	not calibrated
		–	24	–	MHz	calibrated
Accuracy	Δf_{OFI} CC	-0.5	–	0.5	%	automatic calibration[1)2)]
		-15	–	15	%	factory calibration, V_{DDP} = 3.3 V
		-25	–	25	%	no calibration, V_{DDP} = 3.3 V
		-7	–	7	%	Variation over voltage range[3)] 3.13 V ≤ V_{DDP} ≤ 3.63 V
Start-up time	t_{OFIS} CC	–	50	–	µs	

1) Error in addition to the accuracy of the reference clock.

2) Automatic calibration compensates variations of the temperature and in the V_{DDP} supply voltage.

3) Deviations from the nominal V_{DDP} voltage induce an additional error to the uncalibrated and/or factory calibrated oscillator frequency.

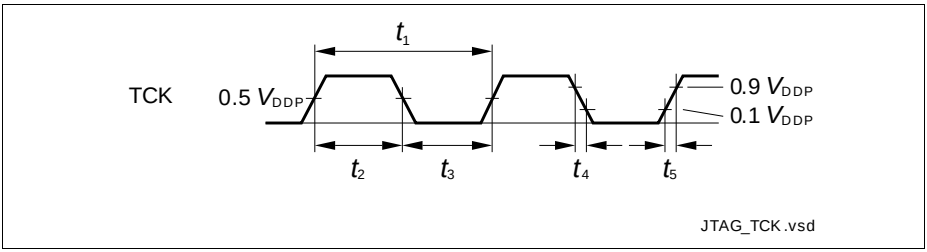

Figure 28 Test Clock Timing (TCK)

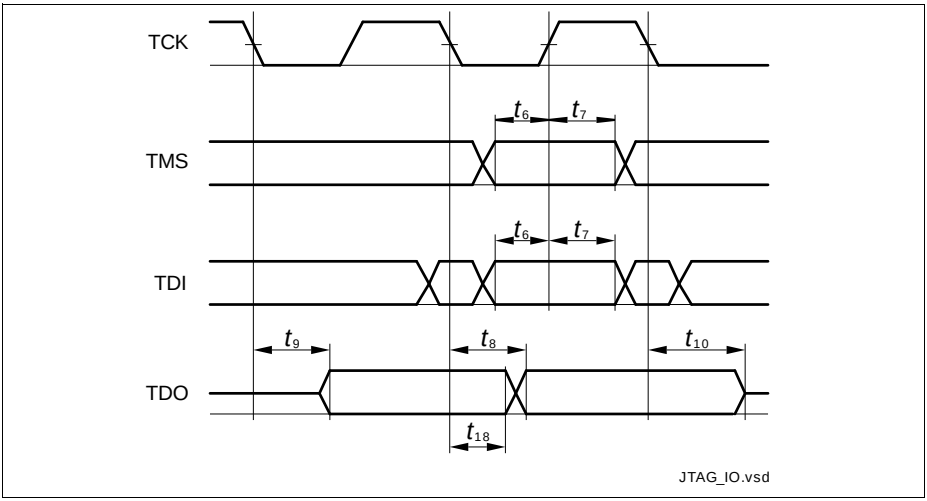

Figure 29 JTAG Timing

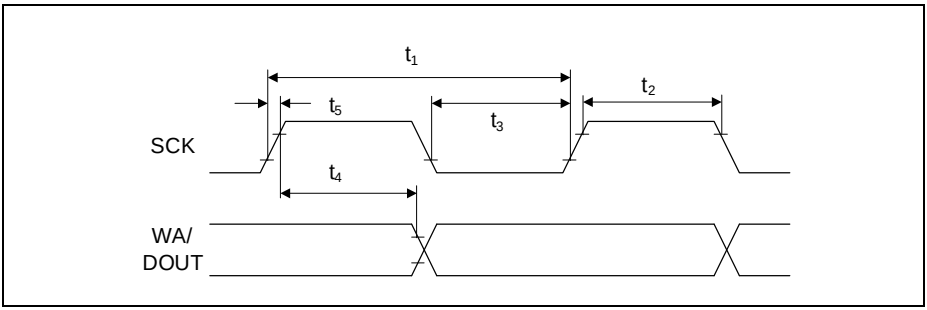

Figure 33 USIC IIS Master Transmitter Timing

Table 53 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	66.6	–	–	ns	
Clock high time	t_7 SR	0.35 x t_{6min}	–	–	ns	
Clock low time	t_8 SR	0.35 x t_{6min}	–	–	ns	
Set-up time	t_9 SR	0.2 x t_{6min}	–	–	ns	
Hold time	t_{10} SR	0	–	–	ns	

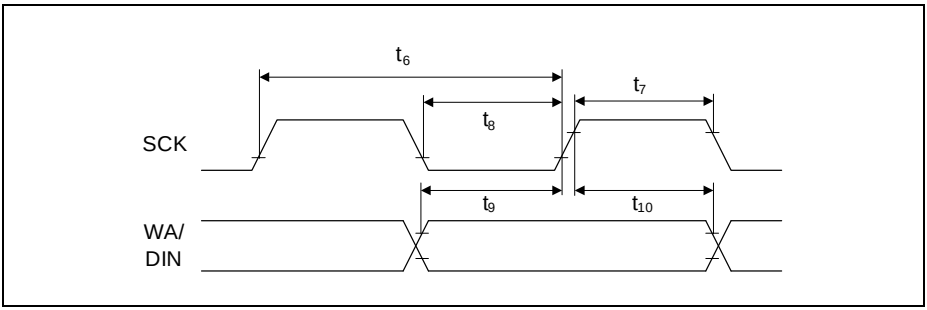

Figure 34 USIC IIS Slave Receiver Timing

5 Quality Declarations

The qualification of the XMC4[12]00 is executed according to the JEDEC standard JESD47H.

Note: For automotive applications refer to the Infineon automotive microcontrollers.

Table 58 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation lifetime	t_{OP} CC	20	–	–	a	$T_J \leq 109°C$, device permanent on
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	–	2 000	V	EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} SR	–	–	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	–	–	3	–	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	–	–	260	°C	Profile according to JEDEC J-STD-020D