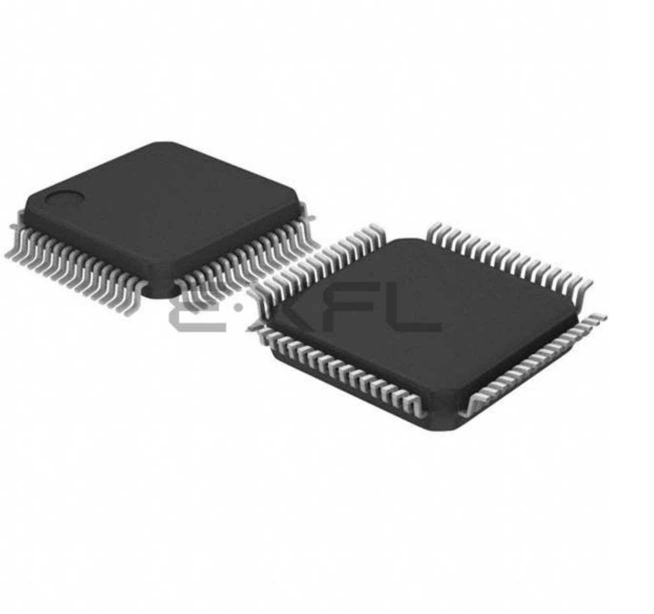

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Speed	80MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP Exposed Pad
Supplier Device Package	PG-TQFP-64-19
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4104f64f64baxqma1

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2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

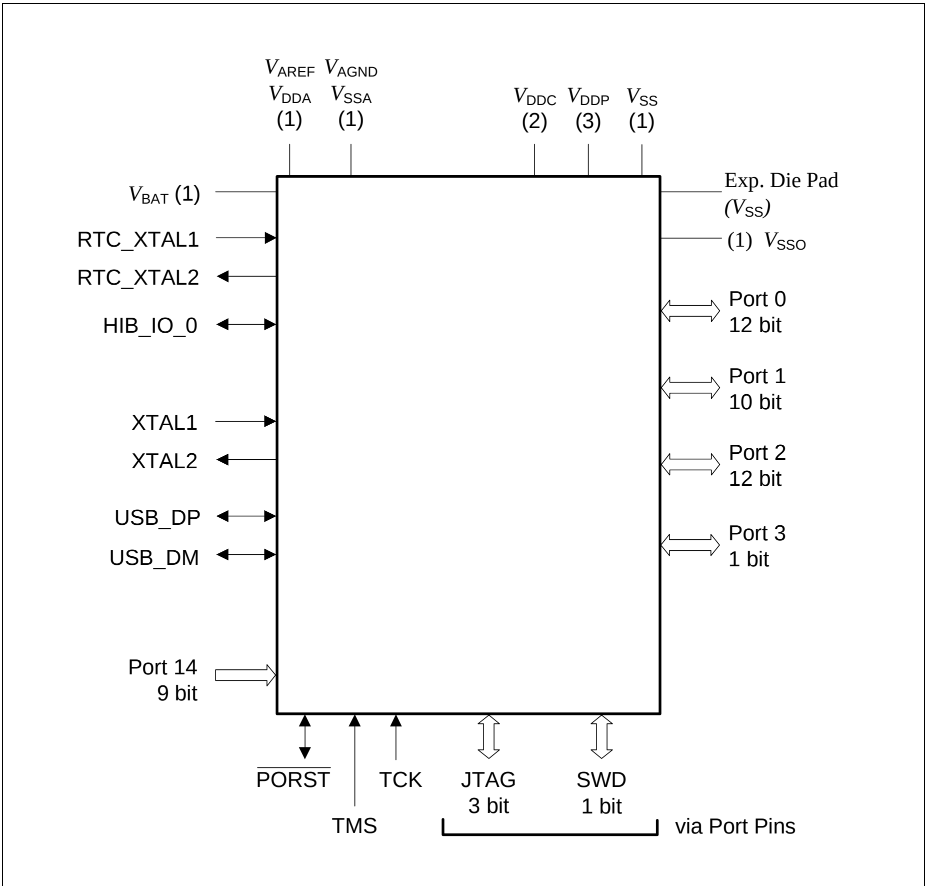

Figure 2 XMC4[12]00 Logic Symbol PG-LQFP-64 and PG-TQFP-64

Table 13 Port I/O Functions (cont'd)

Function	Output					Input								
	ALT1	**ALT2**	**ALT3**	**ALT4**	**HWO0**	**HWI0**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**
P1.8		U0C0.SELO1		U1C1.SCLKOUT										
P1.9	U0C0.SCLKOUT			U1C1.DOUT0										
P1.15	SCU.EXTCLK			U1C0.DOUT0						ERU1.1A0				
P2.0	CAN.N0_TXD			LEDTS0.COL1					ERU0.0B3		CCU40.IN1C			
P2.1				LEDTS0.COL0	DB.TDO/TRACESWO					ERU1.0B0	CCU40.IN0C			
P2.2	VADC.EMUX00		CCU41.OUT3	LEDTS0.LINE0	LEDTS0.EXTENDED0	LEDTS0.TSIN0A		U0C1.DX0A	ERU0.1B2		CCU41.IN3A			
P2.3	VADC.EMUX01	U0C1.SELO0	CCU41.OUT2	LEDTS0.LINE1	LEDTS0.EXTENDED1	LEDTS0.TSIN1A		U0C1.DX2A	ERU0.1A2		CCU41.IN2A			
P2.4	VADC.EMUX02	U0C1.SCLKOUT	CCU41.OUT1	LEDTS0.LINE2	LEDTS0.EXTENDED2	LEDTS0.TSIN2A		U0C1.DX1A	ERU0.0B2		CCU41.IN1A	HRPWM0.BL1A		
P2.5		U0C1.DOUT0	CCU41.OUT0	LEDTS0.LINE3	LEDTS0.EXTENDED3	LEDTS0.TSIN3A		U0C1.DX0B	ERU0.0A2		CCU41.IN0A	HRPWM0.BL2A		
P2.6			CCU80.OUT13	LEDTS0.COL3				CAN.N1_RXDA	ERU0.1B3		CCU40.IN3C			
P2.7		CAN.N1_TXD	CCU80.OUT03	LEDTS0.COL2						ERU1.1B0	CCU40.IN2C			
P2.8			CCU80.OUT32	LEDTS0.LINE4	LEDTS0.EXTENDED4	LEDTS0.TSIN4A	DAC.TRIGGER5				CCU40.IN0B	CCU40.IN1B	CCU40.IN2B	CCU40.IN3B
P2.9			CCU80.OUT22	LEDTS0.LINE5	LEDTS0.EXTENDED5	LEDTS0.TSIN5A	DAC.TRIGGER4				CCU41.IN0B	CCU41.IN1B	CCU41.IN2B	CCU41.IN3B
P2.14	VADC.EMUX11	U1C0.DOUT0	CCU80.OUT21					U1C0.DX0D						
P2.15	VADC.EMUX12		CCU80.OUT11	LEDTS0.LINE6	LEDTS0.EXTENDED6	LEDTS0.TSIN6A		U1C0.DX0C						
P3.0		U0C1.SCLKOUT					U0C1.DX1B				CCU80.IN2C			
P14.0							VADC.G0CH0							
P14.3							VADC.G0CH3	VADC.G1CH3			CAN.N0_RXDB			
P14.4							VADC.G0CH4							
P14.5							VADC.G0CH5				POSIF0.IN2B			
P14.6							VADC.G0CH6				POSIF0.IN1B		G0ORC6	
P14.7							VADC.G0CH7				POSIF0.IN0B			
P14.8					DAC.OUT_0			VADC.G1CH0						

3 Electrical Parameters

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the XMC4[12]00 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are a distinctive feature of the XMC4[12]00 and must be regarded for system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC4[12]00 is designed in.

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 14 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Con dition
			Min.	Typ.	Max.		
Storage temperature	T_{ST}	SR	-65	–	150	°C	–
Junction temperature	T_J	SR	-40	–	150	°C	–
Voltage at 3.3 V power supply pins with respect to V_{SS}	V_{DDP}	SR	–	–	4.3	V	–
Voltage on any Class A and dedicated input pin with respect to V_{SS}	V_{IN}	SR	-1.0	–	V_{DDP} + 1.0 or max. 4.3	V	whichever is lower
Voltage on any analog input pin with respect to V_{AGND}	V_{AIN} V_{AREF}	SR	-1.0	–	V_{DDP} + 1.0 or max. 4.3	V	whichever is lower
Input current on any pin during overload condition	I_{IN}	SR	-10	–	+10	mA	
Absolute maximum sum of all input circuit currents for one port group during overload condition[1)]	ΣI_{IN}	SR	-25	–	+25	mA	
Absolute maximum sum of all input circuit currents during overload condition	ΣI_{IN}	SR	-100	–	+100	mA	

1) The port groups are defined in **Table 18**.

Figure 8 explains the input voltage ranges of V_{IN} and V_{AIN} and its dependency to the supply level of V_{DDP}.The input voltage must not exceed 4.3 V, and it must not be more than 1.0 V above V_{DDP}. For the range up to V_{DDP} + 1.0 V also see the definition of the overload conditions in **Section 3.1.3**.

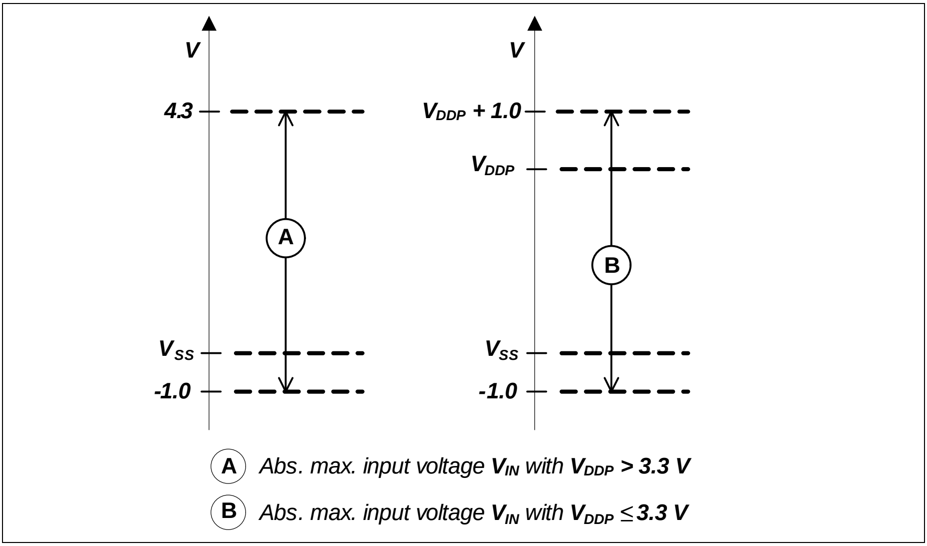

Figure 8 Absolute Maximum Input Voltage Ranges

3.1.5 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC4[12]00. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 20 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A SR	-40	–	85	°C	Temp. Range F
		-40	–	125	°C	Temp. Range K
Digital supply voltage	V_{DDP} SR	3.13[1)]	3.3	3.63[2)]	V	
Core Supply Voltage	V_{DDC} CC	–[1)]	1.3	–	V	Generated internally
Digital ground voltage	V_{SS} SR	0	–	–	V	
ADC analog supply voltage	V_{DDA} SR	3.0	3.3	3.6[2)]	V	
Analog ground voltage for V_{DDA}	V_{SSA} SR	-0.1	0	0.1	V	
Battery Supply Voltage for Hibernate Domain[3)]	V_{BAT} SR	1.95[4)]	–	3.63	V	When V_{DDP} is supplied V_{BAT} has to be supplied as well.
System Frequency	f_{SYS} SR	–	–	80	MHz	
Short circuit current of digital outputs	I_{SC} SR	-5	–	5	mA	
Absolute sum of short circuit currents per pin group[5)]	ΣI_{SC_PG} SR	–	–	20	mA	
Absolute sum of short circuit currents of the device	ΣI_{SC_D} SR	–	–	100	mA	

1) See also the Supply Monitoring thresholds, **Section 3.3.2**.

2) Voltage overshoot to 4.0 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h over lifetime.

3) Different limits apply for LPAC operation, **Section 3.2.6**

4) To start the hibernate domain it is required that $V_{BAT} \geq 2.1$ V, for a reliable start of the oscillation of RTC_XTAL in crystal mode it is required that $V_{BAT} \geq 3.0$ V.

5) The port groups are defined in **Table 18**.

The power-up calibration of the ADC requires a maximum number of 4 352 f_{ADCI} cycles.

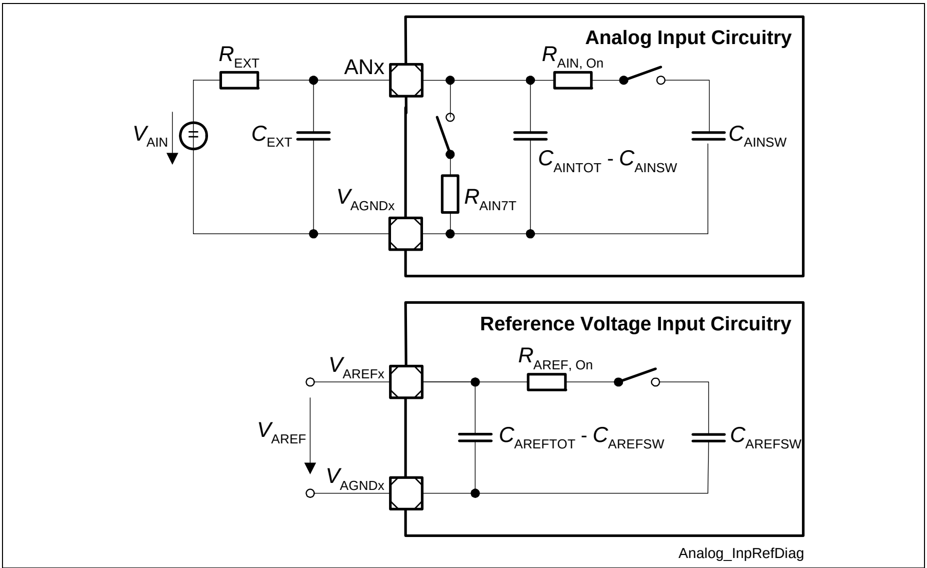

Figure 13 ADCx Input Circuits

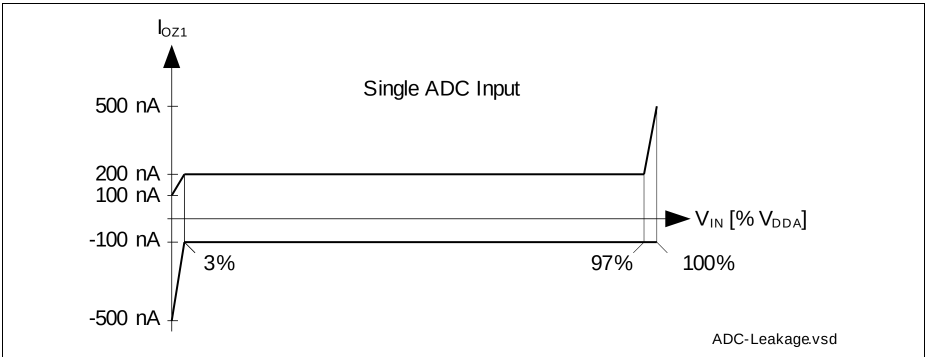

Figure 14 ADCx Analog Input Leakage Current

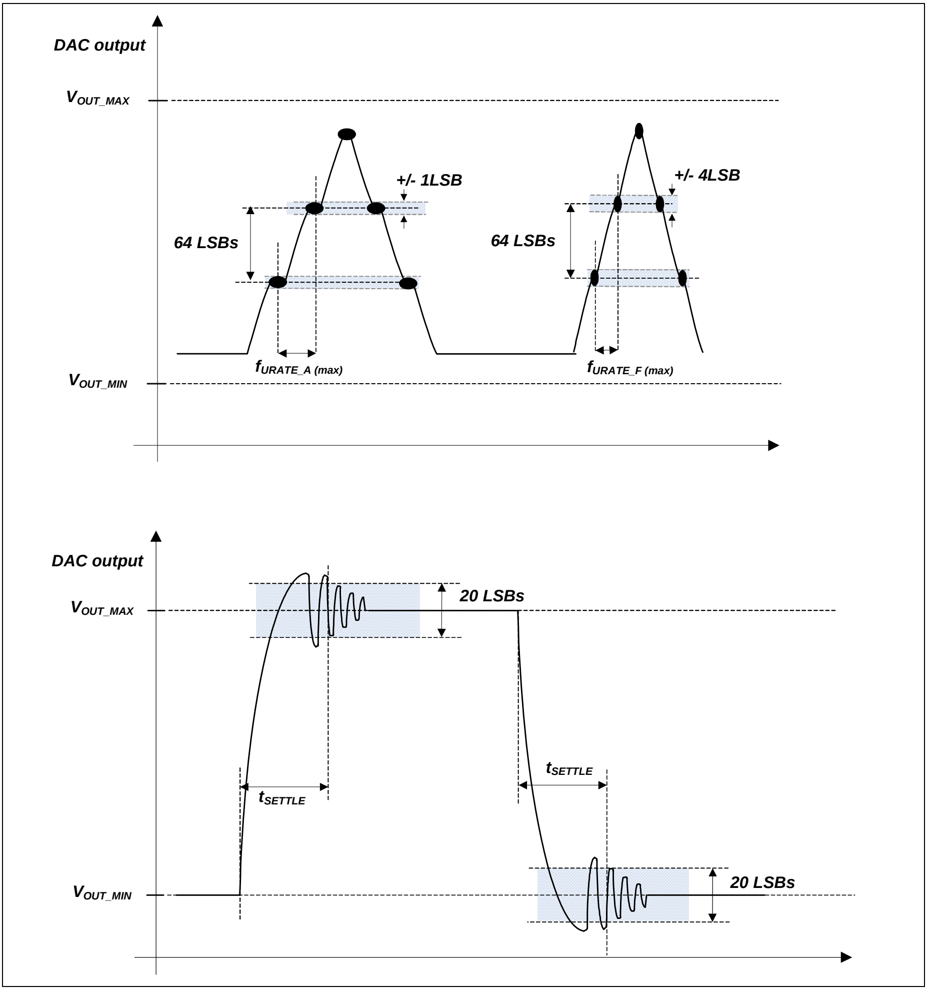

Figure 15 DAC Conversion Examples

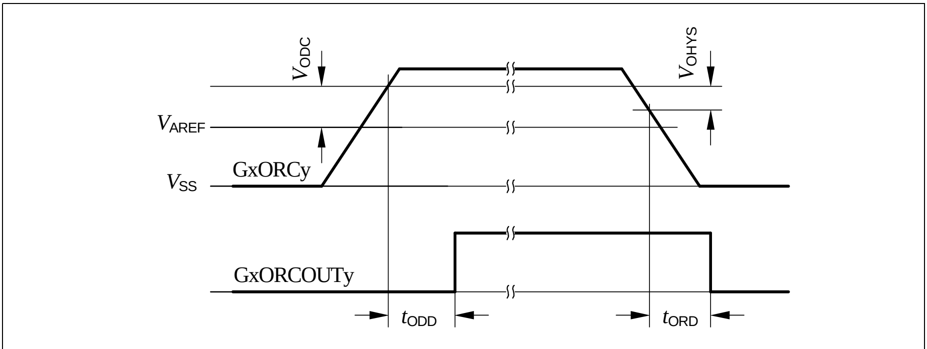

Figure 16 GxORCOUTy Trigger Generation

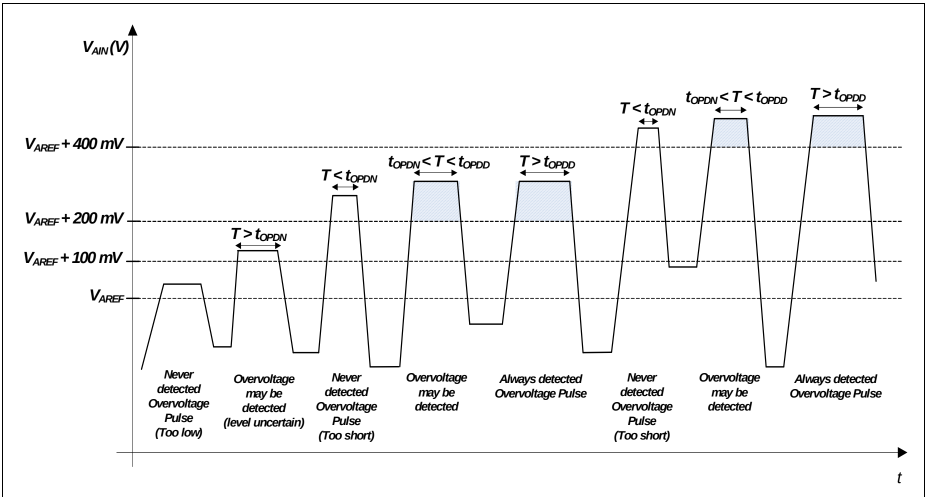

Figure 17 ORC Detection Ranges

3.2.9 Oscillator Pins

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The oscillator pins can be operated with an external crystal (see **Figure 21**) or in direct input mode (see **Figure 22**).

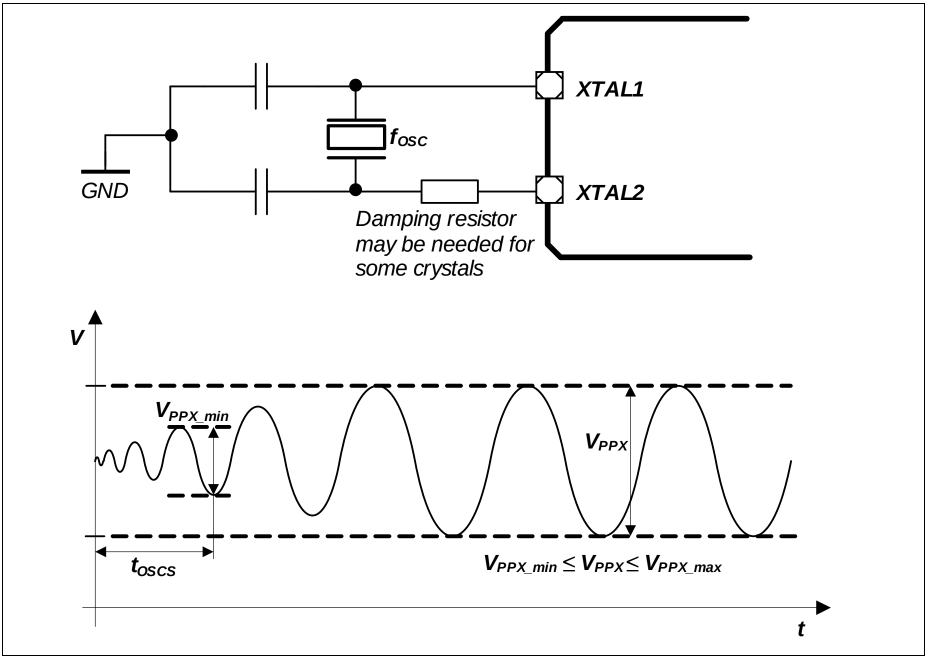

Figure 21 Oscillator in Crystal Mode

Table 36 OSC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	4	–	40	MHz	Direct Input Mode selected
		4	–	25	MHz	External Crystal Mode selected
Oscillator start-up time[1)2)]	t_{OSCS} CC	–	–	10	ms	
Input voltage at XTAL1	V_{IX} SR	-0.5	–	V_{DDP} + 0.5	V	
Input amplitude (peak-to-peak) at XTAL1[2)3)]	V_{PPX} SR	0.4 × V_{DDP}	–	V_{DDP} + 1.0	V	
Input high voltage at XTAL1[4)]	V_{IHBX} SR	1.0	–	V_{DDP} + 0.5	V	
Input low voltage at XTAL1[4)]	V_{ILBX} SR	-0.5	–	0.4	V	
Input leakage current at XTAL1	I_{ILX1} CC	-100	–	100	nA	Oscillator power down $0\ V \leq V_{IX} \leq V_{DDP}$

1) t_{OSCS} is defined from the moment the oscillator is enabled wih SCU_OSCHPCTRL.MODE until the oscillations reach an amplitude at XTAL1 of 0.4 * V_{DDP}.

2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.

3) If the shaper unit is enabled and not bypassed.

4) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.

Table 37 RTC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	–	32.768	–	kHz	
Oscillator start-up time[1][2][3]	t_{OSCS} CC	–	–	5	s	
Input voltage at RTC_XTAL1	V_{IX} SR	-0.3	–	V_{BAT} + 0.3	V	
Input amplitude (peak-to-peak) at RTC_XTAL1[2][4]	V_{PPX} SR	0.4	–	–	V	
Input high voltage at RTC_XTAL1[5]	V_{IHBX}SR	$0.6 \times V_{BAT}$	–	V_{BAT} + 0.3	V	
Input low voltage at RTC_XTAL1[5]	V_{ILBX} SR	-0.3	–	$0.36 \times V_{BAT}$	V	
Input Hysteresis for RTC_XTAL1[5][6]	V_{HYSX} CC	$0.1 \times V_{BAT}$		–	V	$3.0\ V \leq V_{BAT} < 3.6\ V$
		$0.03 \times V_{BAT}$		–	V	$V_{BAT} < 3.0\ V$
Input leakage current at RTC_XTAL1	I_{ILX1} CC	-100	–	100	nA	Oscillator power down $0\ V \leq V_{IX} \leq V_{BAT}$

1) t_{OSCS} is defined from the moment the oscillator is enabled by the user with SCU_OSCULCTRL.MODE until the oscillations reach an amplitude at RTC_XTAL1 of 400 mV.

2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.

3) For a reliable start of the oscillation in crystal mode it is required that $V_{BAT} \geq 3.0$ V. A running oscillation is maintained across the full V_{BAT} voltage range.

4) If the shaper unit is enabled and not bypassed.

5) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.

6) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

Table 38 Power Supply Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sleep supply current[3)] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS} CC	–	76	–	mA	80 / 80 / 80
		–	73	–		80 / 40 / 40
		–	70	–		40 / 40 / 80
		–	56	–		24 / 24 / 24
		–	47	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	46	–		100 / 100 / 100
Sleep supply current[4)] Peripherals disabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS} CC	–	59	–	mA	80 / 80 / 80
		–	58	–		80 / 40 / 40
		–	57	–		40 / 40 / 80
		–	51	–		24 / 24 / 24
		–	46	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	46	–		100 / 100 / 100
Deep Sleep supply current[5)] Flash in Sleep mode Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPD} CC	–	6.9	–	mA	24 / 24 / 24
		–	4.3	–		4 / 4 / 4
		–	3.8	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	4.5	–		100 / 100 / 100 [6)]
Hibernate supply current RTC on[7)]	I_{DDPH} CC	–	10.8	–	µA	V_{BAT} = 3.3 V
		–	8.0	–		V_{BAT} = 2.4 V
		–	6.8	–		V_{BAT} = 2.0 V
Hibernate supply current RTC off[8)]	I_{DDPH} CC	–	10.3	–	µA	V_{BAT} = 3.3 V
		–	7.5	–		V_{BAT} = 2.4 V
		–	6.3	–		V_{BAT} = 2.0 V
Worst case active supply current[9)]	I_{DDPA} CC	–	–	140 [10)]	mA	V_{DDP} = 3.6 V, T_J = 150 °C
V_{DDA} power supply current	I_{DDA} CC	–	–	–[11)]	mA	
I_{DDP} current at $\overline{PORST}$ Low	I_{DDP_PORST} CC	–	–	24	mA	V_{DDP} = 3.6 V, T_J = 150 °C

Table 42 Power Sequencing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Positive Load Step Current	ΔI_{PLS} SR	-	–	50	mA	Load increase on V_{DDP} $\Delta t \leq 10$ ns
Negative Load Step Current	ΔI_{NLS} SR	-	–	150	mA	Load decrease on V_{DDP} $\Delta t \leq 10$ ns
V_{DDC} Voltage Over- / Undershoot from Load Step	ΔV_{LS} CC	-	–	±100	mV	For maximum positive or negative load step
Positive Load Step Settling Time	t_{PLSS} SR	50	–	-	µs	
Negative Load Step Settling Time	t_{NLSS} SR	100	–	-	µs	
External Buffer Capacitor on V_{DDC}	C_{EXT} SR	3	4.7	6	µF	In addition C = 100 nF capacitor on each V_{DDC} pin

Positive Load Step Examples

System assumptions:
$f_{CPU} = f_{SYS}$, target frequency f_{CPU} = 80 MHz, main PLL f_{VCO} = 480 MHz, stepping done by K2 divider, t_{PLSS} between individual steps:

24 MHz - 48 MHz - 80 MHz (K2 steps 20 - 10 - 6)
24 MHz - 60 MHz - 80 MHz (K2 steps 20 - 8 - 6)

3.3.8 Peripheral Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

3.3.8.1 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: Operating Conditions apply.

Table 48 USIC SSC Master Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SCLKOUT master clock period	t_{CLK}	CC	40	–	–	ns	
Slave select output SELO active to first SCLKOUT transmit edge	t_1	CC	t_{SYS} - 6.5[1)]	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2	CC	t_{SYS} - 8.5[1)]	–	–	ns	
Data output DOUT[3:0] valid time	t_3	CC	-6	–	8	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4	SR	23	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5	SR	1	–	–	ns	

1) $t_{SYS} = 1 / f_{PB}$

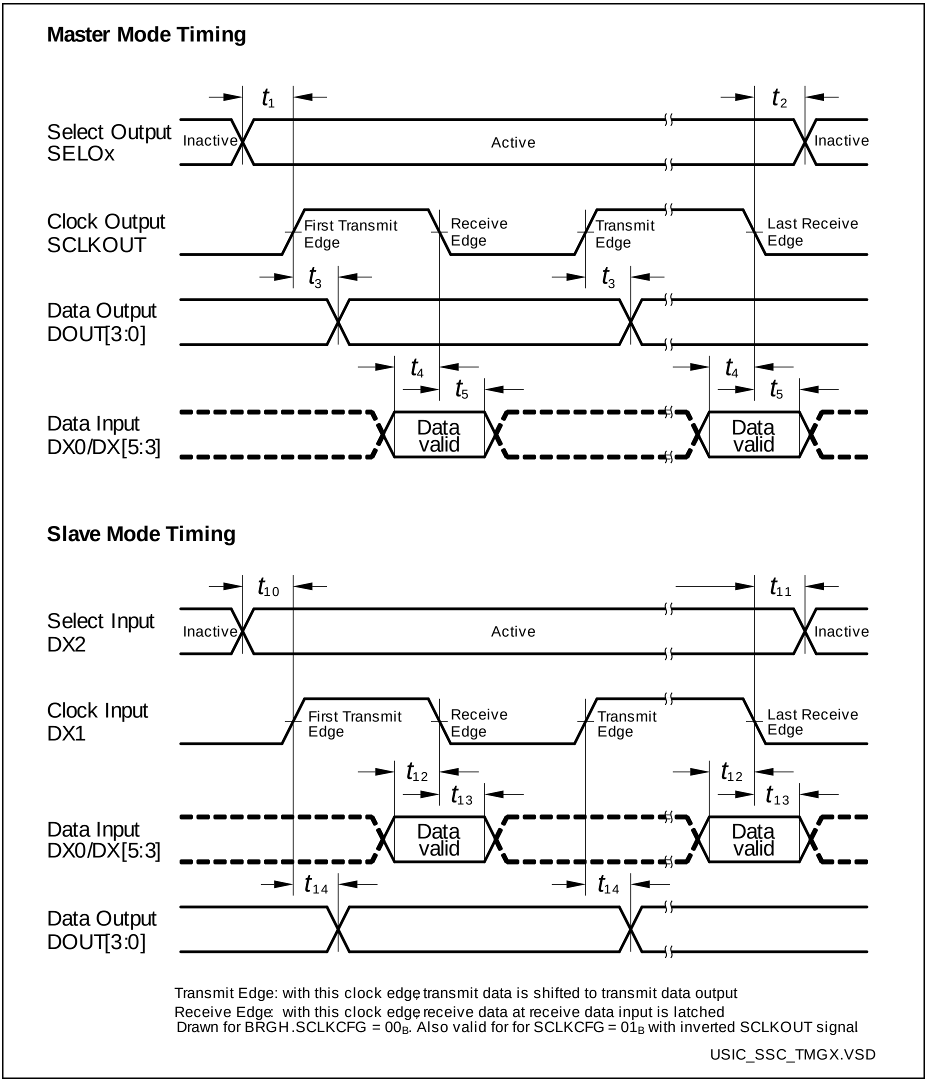

Figure 31 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.

4 Package and Reliability

The XMC4[12]00 is a member of the XMC4000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the Exposed Die Pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 55 provides the thermal characteristics of the packages used in XMC4[12]00. The availability of different packages for different markings is listed in **Table 2**.

Table 55 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad Dimensions	Ex × Ey CC	-	5.8 × 5.8	mm	PG-LQFP-64-19
		-	5.7 × 5.7	mm	PG-TQFP-64-19
		-	5.2 × 5.2	mm	PG-VQFN-48-53
		-	5.2 × 5.2	mm	PG-VQFN-48-71
Thermal resistance Junction-Ambient	$R_{\Theta JA}$ CC	-	30	K/W	PG-LQFP-64-19[1)]
		-	23.4	K/W	PG-TQFP-64-19[1)]
		-	34.8	K/W	PG-VQFN-48-53[1)] PG-VQFN-48-71[1)]

1) Device mounted on a 4-layer JEDEC board (JESD 51-7) with thermal vias; exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SS}, independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMC4[12]00 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The

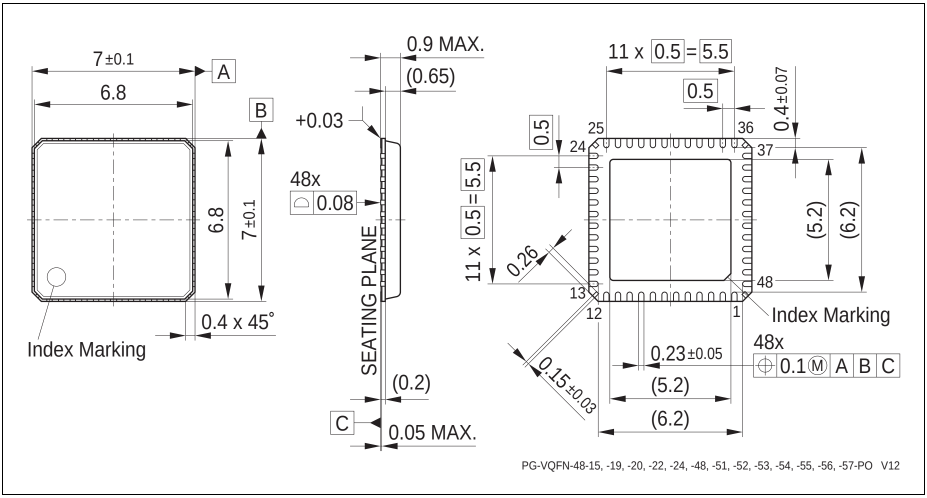

Figure 38 **PG-VQFN-48-53** (Plastic Green Very Thin Profile Flat Non Leaded Package)

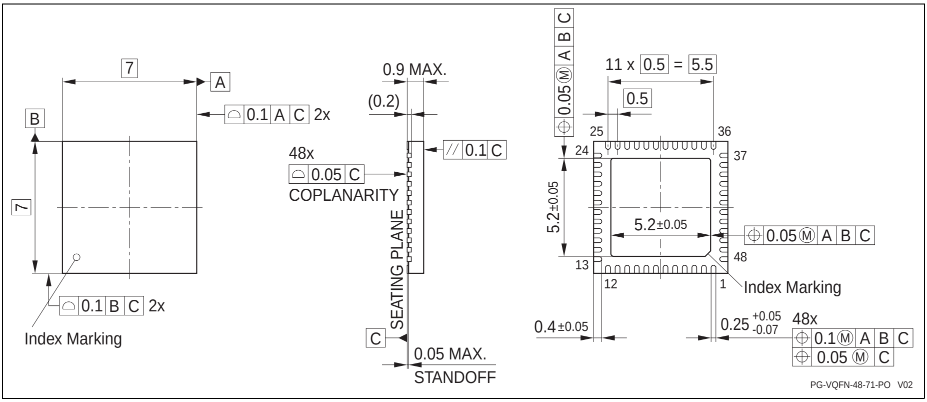

Figure 39 **PG-VQFN-48-71** (Plastic Green Very Thin Profile Flat Non Leaded Package)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page "Packages": **http://www.infineon.com/packages**