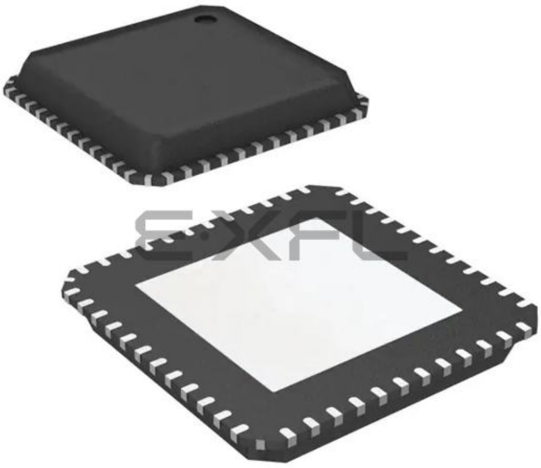

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 9x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-53
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4104q48f128baxuma1

XMC4[12]00 Data Sheet

Revision History: V1.3 2015-10

Previous Versions:
V1.2 2014-06
V1.1 2014-03
V1.0 2013-10
V0.6 2012-11

Page	Subjects
12	Added a section listing the packages of the different markings.
14	Added BA marking variant.
14	Corrected SCU_IDCHIP value of XMC4100 EES-AA/ES-AA.
36	Added footnote explaining minimum V_{BAT} requirements to start the hibernate domain and/or oscillation of a crystal on RTC_XTAL.
37	Changed pull device definition to System Requirement (SR) to reflect that the specified currents are defined by the characteristics of the external load/driver.
37	Added information that $\overline{\text{PORST}}$ Pull-up is identical to the pull-up on standard I/O pins.
42	Updated C_{AINSW}, C_{AINTOT} and R_{AIN} parameters with improved values.
56	Added footnote on test configuration for LPAC measurement.
58	Corrected parameter name of of USB pull device (upstream port receiving) definition according to USB standard (referenced to DM instead of DP)
62	Relaxed RTC_XTAL V_{PPX} parameter value and changed it to a system requirement.
66	Added footnote on current consumption by enabling of f_{CCU}.
67	Added Flash endurance parameter for 64 Kbytes Physical Sector PS4 N_{EPS4} for devices with BA marking.
many	Added PG-TQFP-64-19 and PG-VQFN-48-71 package information.
89, **91**	Added tables describing the differences between PG-LQFP-64-19 to PG-TQFP-64-19 as well as PG-VQFN-48-53 to PG-VQFN-48-71 packages.
93	Updated to JEDEC standard J-STD-020D for the moisture sensitivity level and added solder temperature parameter according to the same standard.

About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC4[12]00 series devices.

The document describes the characteristics of a superset of the XMC4[12]00 series devices. For simplicity, the various device types are referred to by the collective term XMC4[12]00 throughout this manual.

XMC4000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  - decribes the functionality of the superset of devices.
- **Data Sheets**
  - list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  - list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to **http://www.infineon.com/xmc4000** to get access to the latest versions of those documents.

1 Summary of Features

The XMC4[12]00 devices are members of the XMC4000 Family of microcontrollers based on the ARM Cortex-M4 processor core. The XMC4000 is a family of high performance and energy efficient microcontrollers optimized for Industrial Connectivity, Industrial Control, Power Conversion, Sense & Control.

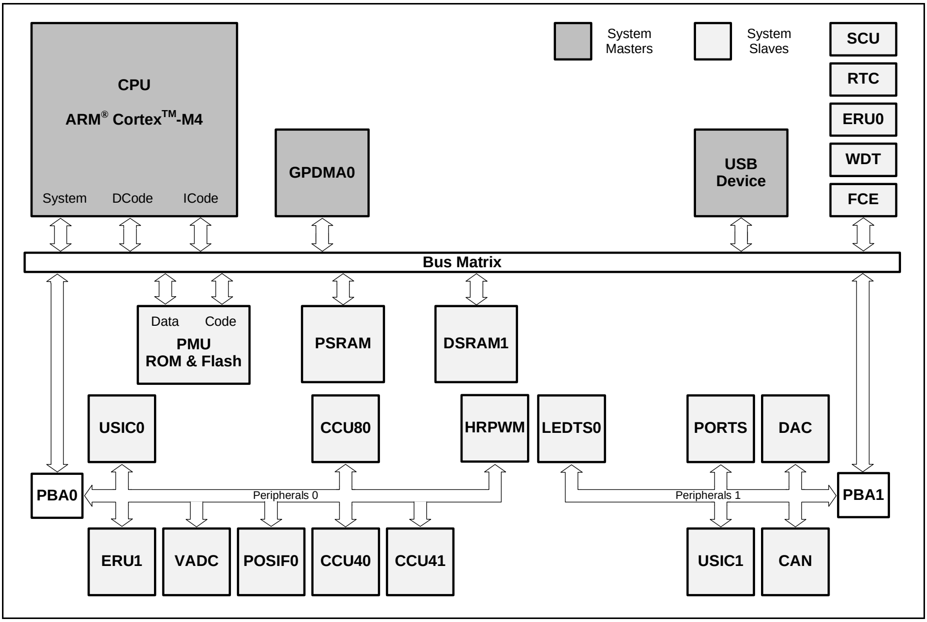

Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
  - High Performance 32-bit ARM Cortex-M4 CPU
  - 16-bit and 32-bit Thumb2 instruction set
  - DSP/MAC instructions
  - System timer (SysTick) for Operating System support
- Floating Point Unit
- Memory Protection Unit
- Nested Vectored Interrupt Controller
- One General Purpose DMA with up-to 8 channels
- Event Request Unit (ERU) for programmable processing of external and internal service requests
- Flexible CRC Engine (FCE) for multiple bit error detection

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC4<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set
- <Z> the package variant
  - E: LFBGA
  - F: LQFP, TQFP
  - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
  - F: -40°C to 85°C
  - K: -40°C to 125°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC4[12]00 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC4100 and XMC4200 series, some descriptions may not apply to a specific product. Please see **Table 1**.

For simplicity the term **XMC4[12]00** is used for all derivatives throughout this document.

1.2 Device Types

These device types are available and can be ordered through Infineon’s direct and/or distribution channels.

Table 1 Synopsis of XMC4[12]00 Device Types

Derivative[1]	Package	Flash Kbytes	SRAM Kbytes
XMC4200-F64x256	PG-yQFP-64[2]	256	40
XMC4200-Q48x256	PG-VQFN-48	256	40
XMC4100-F64x128	PG-yQFP-64[2]	128	20
XMC4100-Q48x128	PG-VQFN-48	128	20
XMC4104-F64x64	PG-yQFP-64[2]	64	20
XMC4104-Q48x64	PG-VQFN-48	64	20
XMC4104-F64x128	PG-yQFP-64[2]	128	20
XMC4104-Q48x128	PG-VQFN-48	128	20
XMC4108-F64x64	PG-yQFP-64[2]	64	20
XMC4108-Q48x64	PG-VQFN-48	64	20

1) x is a placeholder for the supported temperature range.

2) y is a placeholder for the QFP package variant, LQFP or TQFP depending on the stepping, see **Section 1.3**.

Table 4 Features of XMC4[12]00 Device Types

Derivative[1)]	ADC Chan.	DAC Chan.	CCU4 Slice	CCU8 Slice	POSIF Intf.	HRPWM Intf.
XMC4200-F64x256	10	2	2 x 4	1 x 4	1	1
XMC4200-Q48x256	9	2	2 x 4	1 x 4	1	1
XMC4100-F64x128	10	2	2 x 4	1 x 4	1	1
XMC4100-Q48x128	9	2	2 x 4	1 x 4	1	1
XMC4104-F64x64	10	2	2 x 4	1 x 4	1	1
XMC4104-Q48x64	9	2	2 x 4	1 x 4	1	1
XMC4104-F64x128	10	2	2 x 4	1 x 4	1	1
XMC4104-Q48x128	9	2	2 x 4	1 x 4	1	1
XMC4108-F64x64	10	2	2 x 4	1 x 4	1	–
XMC4108-Q48x64	9	2	2 x 4	1 x 4	1	–

1) x is a placeholder for the supported temperature range.

1.5 Definition of Feature Variants

The XMC4[12]00 types are offered with several memory sizes and number of available VADC channels. **Table 5** describes the location of the available Flash memory, **Table 6** describes the location of the available SRAMs, **Table 7** the available VADC channels.

Table 5 Flash Memory Ranges

Total Flash Size	Cached Range	Uncached Range
256 Kbytes	$0800\ 0000_H$ – $0803\ FFFF_H$	$0C00\ 0000_H$ – $0C03\ FFFF_H$
128 Kbytes	$0800\ 0000_H$ – $0801\ FFFF_H$	$0C00\ 0000_H$ – $0C01\ FFFF_H$
64 Kbytes	$0800\ 0000_H$ – $0800\ FFFF_H$	$0C00\ 0000_H$ – $0C00\ FFFF_H$

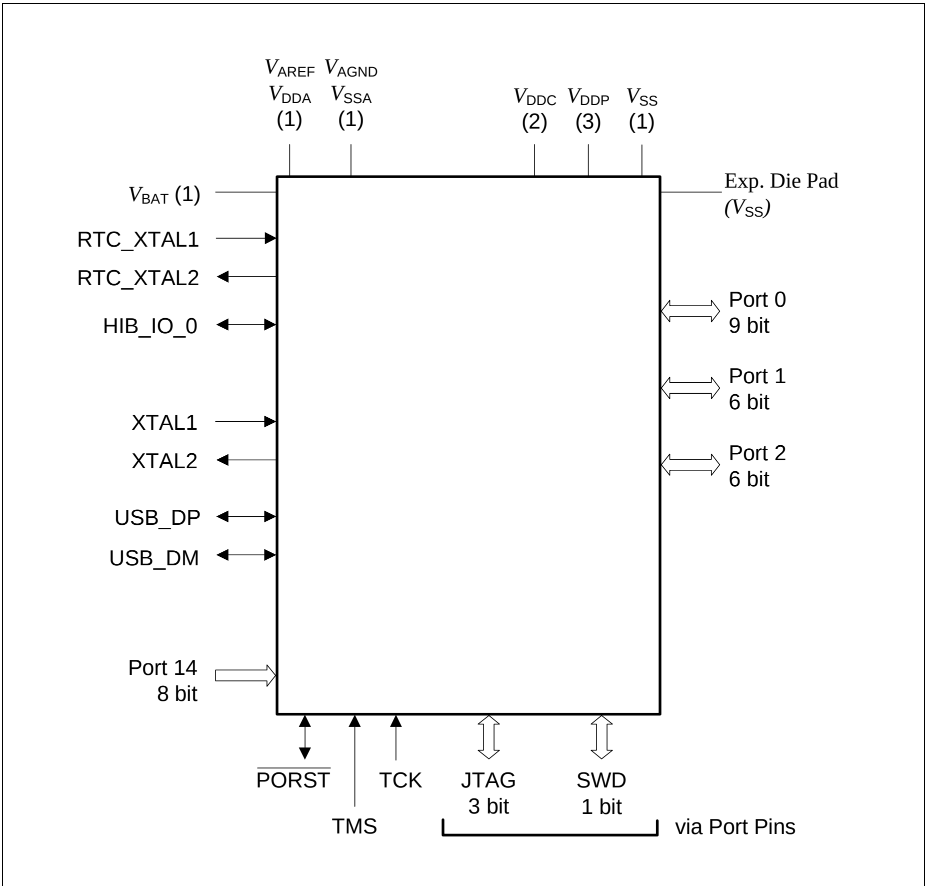

Figure 3 XMC4[12]00 Logic Symbol PG-VQFN-48

Table 11 Package Pin Mapping (cont'd)

Function	**LQFP-64 TQFP-64**	**VQFN-48**	**Pad Type**	**Notes**
P0.11	59	-	A1+	
P1.0	52	40	A1+	
P1.1	51	39	A1+	
P1.2	50	38	A1+	
P1.3	49	37	A1+	
P1.4	48	36	A1+	
P1.5	47	35	A1+	
P1.7	55	-	A1+	
P1.8	54	-	A1+	
P1.9	53	-	A1+	
P1.15	46	-	A1+	
P2.0	34	26	A1+	
P2.1	33	25	A1+	After a system reset, via HWSEL this pin selects the DB.TDO function.
P2.2	32	24	A1+	
P2.3	31	23	A1+	
P2.4	30	22	A1+	
P2.5	29	21	A1+	
P2.6	36	-	A1+	
P2.7	35	-	A1+	
P2.8	28	-	A1+	
P2.9	27	-	A1+	
P2.14	26	-	A1+	
P2.15	25	-	A1+	
P3.0	5	-	A1+	
P14.0	20	16	AN/DIG_IN	
P14.3	19	15	AN/DIG_IN	
P14.4	18	14	AN/DIG_IN	
P14.5	17	13	AN/DIG_IN	
P14.6	16	12	AN/DIG_IN	
P14.7	15	11	AN/DIG_IN	
P14.8	24	20	AN/DAC/DIG_IN	

Table 11 Package Pin Mapping (cont'd)

Function	LQFP-64 TQFP-64	VQFN-48	Pad Type	Notes
VSSO	41	-	Power	
VSS	Exp. Pad	Exp. Pad	Power	**Exposed Die Pad** The exposed die pad is connected internally to VSS. For proper operation, it is mandatory to connect the exposed pad directly to the common ground on the board. For thermal aspects, please refer to the Data Sheet. Board layout examples are given in an application note.

3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 15 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
  – pad supply levels (V_{DDP} or V_{DDA})
  – temperature

If a pin current is outside of the **Operating Conditions** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

Table 15 Overload Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Input current on any port pin during overload condition	I_{OV}	SR	-5	–	5	mA	
Absolute sum of all input circuit currents for one port group during overload condition[1]	I_{OVG}	SR	–	–	20	mA	$\Sigma\|I_{OVx}\|$, for all $I_{OVx} < 0$ mA
			–	–	20	mA	$\Sigma\|I_{OVx}\|$, for all $I_{OVx} > 0$ mA
Absolute sum of all input circuit currents during overload condition	I_{OVS}	SR	–	–	80	mA	ΣI_{OVG}

1) The port groups are defined in **Table 18**.

Figure 9 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

3.1.5 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC4[12]00. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 20 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A SR	-40	–	85	°C	Temp. Range F
		-40	–	125	°C	Temp. Range K
Digital supply voltage	V_{DDP} SR	3.13[1]	3.3	3.63[2]	V	
Core Supply Voltage	V_{DDC} CC	–[1]	1.3	–	V	Generated internally
Digital ground voltage	V_{SS} SR	0	–	–	V	
ADC analog supply voltage	V_{DDA} SR	3.0	3.3	3.6[2]	V	
Analog ground voltage for V_{DDA}	V_{SSA} SR	-0.1	0	0.1	V	
Battery Supply Voltage for Hibernate Domain[3]	V_{BAT} SR	1.95[4]	–	3.63	V	When V_{DDP} is supplied V_{BAT} has to be supplied as well.
System Frequency	f_{SYS} SR	–	–	80	MHz	
Short circuit current of digital outputs	I_{SC} SR	-5	–	5	mA	
Absolute sum of short circuit currents per pin group[5]	ΣI_{SC_PG} SR	–	–	20	mA	
Absolute sum of short circuit currents of the device	ΣI_{SC_D} SR	–	–	100	mA	

1) See also the Supply Monitoring thresholds, **Section 3.3.2**.

2) Voltage overshoot to 4.0 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h over lifetime.

3) Different limits apply for LPAC operation, **Section 3.2.6**

4) To start the hibernate domain it is required that $V_{BAT} \geq 2.1$ V, for a reliable start of the oscillation of RTC_XTAL in crystal mode it is required that $V_{BAT} \geq 3.0$ V.

5) The port groups are defined in **Table 18**.

Conversion Time

Table 26 Conversion Time (Operating Conditions apply)

Parameter	Symbol		Values	Unit	Note
Conversion time	t_C	CC	$2 \times T_{ADC}$ + (2 + N + STC + PC +DM) $\times$ T_{ADCI}	µs	N = 8, 10, 12 for N-bit conversion $T_{ADC} = 1 / f_{PERIPH}$ $T_{ADCI} = 1 / f_{ADCI}$

- STC defines additional clock cycles to extend the sample time
- PC adds two cycles if post-calibration is enabled
- DM adds one cycle for an extended conversion time of the MSB

Conversion Time Examples

System assumptions (max. f_{ADC}):
f_{ADC} = 80 MHz i.e. t_{ADC} = 12.5 ns, DIVA = 2, f_{ADCI} = 26.7 MHz i.e. t_{ADCI} = 37.5 ns

According to the given formulas the following minimum conversion times can be achieved (STC = 0, DM = 0):

12-bit post-calibrated conversion (PC = 2):
$t_{CN12C} = (2 + 12 + 2) \times t_{ADCI} + 2 \times t_{ADC} = 16 \times 37.5\text{ ns} + 2 \times 12.5\text{ ns} = 625\text{ ns}$

12-bit uncalibrated conversion:
$t_{CN12} = (2 + 12) \times t_{ADCI} + 2 \times t_{ADC} = 14 \times 37.5\text{ ns} + 2 \times 12.5\text{ ns} = 550\text{ ns}$

10-bit uncalibrated conversion:
$t_{CN10} = (2 + 10) \times t_{ADCI} + 2 \times t_{ADC} = 12 \times 37.5\text{ ns} + 2 \times 12.5\text{ ns} = 475\text{ ns}$

8-bit uncalibrated:
$t_{CN8} = (2 + 8) \times t_{ADCI} + 2 \times t_{ADC} = 10 \times 37.5\text{ ns} + 2 \times 12.5\text{ ns} = 400\text{ ns}$

System assumptions (max. f_{ADCI}):
f_{ADC} = 60 MHz i.e. t_{ADC} = 16.67 ns, DIVA = 1, f_{ADCI} = 30 MHz i.e. t_{ADCI} = 33.33 ns

12-bit post-calibrated conversion (PC = 2):
$t_{CN12C} = (2 + 12 + 2) \times t_{ADCI} + 2 \times t_{ADC} = 16 \times 33.33\text{ ns} + 2 \times 16.67\text{ ns} = 566\text{ ns}$

3.2.3 Digital to Analog Converters (DACx)

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 27 DAC Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
RMS supply current	I_{DD}	CC	–	2.5	4	mA	per active DAC channel, without load currents of DAC outputs
Resolution	RES	CC	–	12	–	Bit	
Update rate	f_{URATE_A}	CC	–		2	Msample/s	data rate, where DAC can follow 64 LSB code jumps to ± 1LSB accuracy
Update rate	f_{URATE_F}	CC	–		5	Msample/s	data rate, where DAC can follow 64 LSB code jumps to ± 4 LSB accuracy
Settling time	t_{SETTLE}	CC	–	1	2	µs	at full scale jump, output voltage reaches target value ± 20 LSB
Slew rate	SR	CC	2	5	–	V/µs	
Minimum output voltage	V_{OUT_MIN}	CC	–	0.3	–	V	code value unsigned: 000_H; signed: 800_H
Maximum output voltage	V_{OUT_MAX}	CC	–	2.5	–	V	code value unsigned: FFF_H; signed: $7FF_H$
Integral non-linearity[1)]	INL	CC	-5.5	±2.5	5.5	LSB	$R_L \geq 5$ kOhm, $C_L \leq 50$ pF
Differential non-linearity	DNL	CC	-2	±1	2	LSB	$R_L \geq 5$ kOhm, $C_L \leq 50$ pF

Table 27 DAC Parameters (Operating Conditions apply) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Offset error	ED_{OFF} CC		±20		mV	
Gain error	ED_{G_IN} CC	-5	0	5	%	
Startup time	$t_{STARTUP}$ CC	–	15	30	µs	time from output enabling till code valid ±16 LSB
3dB Bandwidth of Output Buffer	f_{C1} CC	2.5	5	–	MHz	verified by design
Output sourcing current	I_{OUT_SOURCE} CC	–	-30	–	mA	
Output sinking current	I_{OUT_SINK} CC	–	0.6	–	mA	
Output resistance	R_{OUT} CC	–	50	–	Ohm	
Load resistance	R_L SR	5	–	–	kOhm	
Load capacitance	C_L SR	–	–	50	pF	
Signal-to-Noise Ratio	*SNR* CC	–	70	–	dB	examination bandwidth < 25 kHz
Total Harmonic Distortion	*THD* CC	–	70	–	dB	examination bandwidth < 25 kHz
Power Supply Rejection Ratio	*PSRR* CC	–	56	–	dB	to V_{DDA} verified by design

1) According to best straight line method.

Conversion Calculation

Unsigned:
DACxDATA = 4095 × (V_{OUT} - V_{OUT_MIN}) / (V_{OUT_MAX} - V_{OUT_MIN})

Signed:
DACxDATA = 4095 × (V_{OUT} - V_{OUT_MIN}) / (V_{OUT_MAX} - V_{OUT_MIN}) - 2048

3.2.8 USB Device Interface DC Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification. High-Speed Mode is not supported.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 35 USB Device Data Line (USB_DP, USB_DM) Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Input low voltage	V_{IL}	SR	–	–	0.8	V	
Input high voltage (driven)	V_{IH}	SR	2.0	–	–	V	
Input high voltage (floating) [1)]	V_{IHZ}	SR	2.7	–	3.6	V	
Differential input sensitivity	V_{DIS}	CC	0.2	–	–	V	
Differential common mode range	V_{CM}	CC	0.8	–	2.5	V	
Output low voltage	V_{OL}	CC	0.0	–	0.3	V	1.5 kOhm pull-up to 3.6 V
Output high voltage	V_{OH}	CC	2.8	–	3.6	V	15 kOhm pull-down to 0 V
DP pull-up resistor (idle bus)	R_{PUI}	CC	900	–	1 575	Ohm	
DP pull-up resistor (upstream port receiving)	R_{PUA}	CC	1 425	–	3 090	Ohm	
Input impedance DP, DM	Z_{INP}	CC	300	–	–	kOhm	$0\ V \leq V_{IN} \leq V_{DDP}$
Driver output resistance DP, DM	Z_{DRV}	CC	28	–	44	Ohm	

1) Measured at A-connector with 1.5 kOhm ± 5% to 3.3 V ± 0.3 V connected to USB_DP or USB_DM and at B-connector with 15 kOhm ± 5% to ground connected to USB_DP and USB_DM.

3.2.9 Oscillator Pins

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The oscillator pins can be operated with an external crystal (see **Figure 21**) or in direct input mode (see **Figure 22**).

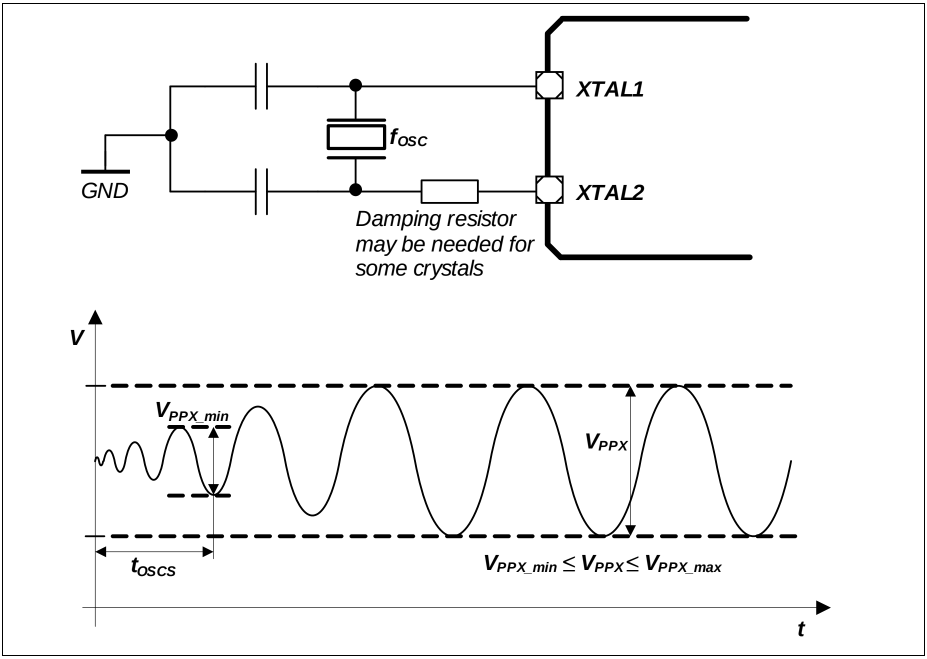

Figure 21 Oscillator in Crystal Mode

3.2.10 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

If not stated otherwise, the operating conditions for the parameters in the following table are:
V_{DDP} = 3.3 V, T_A = 25 °C

Table 38 Power Supply Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Active supply current[1)] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPA}	CC	–	80	–	mA	80 / 80 / 80
			–	75	–		80 / 40 / 40
			–	73	–		40 / 40 / 80
			–	59	–		24 / 24 / 24
			–	50	–		1 / 1 / 1
Active supply current Code execution from RAM Flash in Sleep mode Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPA}	CC	–	24	–	mA	80 / 80 / 80
			–	19	–		80 / 40 / 40
Active supply current[2)] Peripherals disabled Frequency: f_{CPU} / f_{PERIPH} in MHz	I_{DDPA}	CC	–	63	–	mA	80 / 80 / 80
			–	62	–		80 / 40 / 40
			–	60	–		40 / 40 / 80
			–	54	–		24 / 24 / 24
			–	50	–		1 / 1 / 1

3.3.4 Phase Locked Loop (PLL) Characteristics

Main and USB PLL

Table 43 PLL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated Jitter	D_P CC	–	–	±5	ns	accumulated over 300 cycles f_{SYS} = 80 MHz
Duty Cycle[1)]	D_{DC} CC	46	50	54	%	Low pulse to total period, assuming an ideal input clock source
PLL base frequency	$f_{PLLBASE}$ CC	30	–	140	MHz	
VCO input frequency	f_{REF} CC	4	–	16	MHz	
VCO frequency range	f_{VCO} CC	260	–	520	MHz	
PLL lock-in time	t_L CC	–	–	400	µs	

1) 50% for even K2 divider values, 50±(10/K2) for odd K2 divider values.

3.3.5 Internal Clock Source Characteristics

Fast Internal Clock Source

Table 44 Fast Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal frequency	f_{OFINC} CC	–	36.5	–	MHz	not calibrated
		–	24	–	MHz	calibrated
Accuracy	Δf_{OFI} CC	-0.5	–	0.5	%	automatic calibration[1)2)]
		-15	–	15	%	factory calibration, V_{DDP} = 3.3 V
		-25	–	25	%	no calibration, V_{DDP} = 3.3 V
		-7	–	7	%	Variation over voltage range[3)] 3.13 V ≤ V_{DDP} ≤ 3.63 V
Start-up time	t_{OFIS} CC	–	50	–	µs	

1) Error in addition to the accuracy of the reference clock.

2) Automatic calibration compensates variations of the temperature and in the V_{DDP} supply voltage.

3) Deviations from the nominal V_{DDP} voltage induce an additional error to the uncalibrated and/or factory calibrated oscillator frequency.

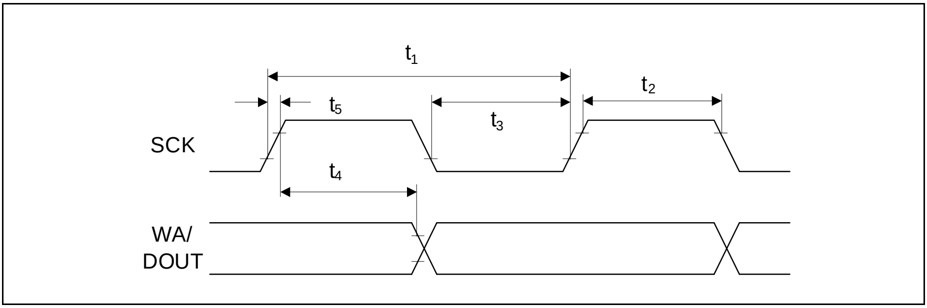

Figure 33 USIC IIS Master Transmitter Timing

Table 53 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	66.6	–	–	ns	
Clock high time	t_7 SR	0.35 x t_{6min}	–	–	ns	
Clock low time	t_8 SR	0.35 x t_{6min}	–	–	ns	
Set-up time	t_9 SR	0.2 x t_{6min}	–	–	ns	
Hold time	t_{10} SR	0	–	–	ns	

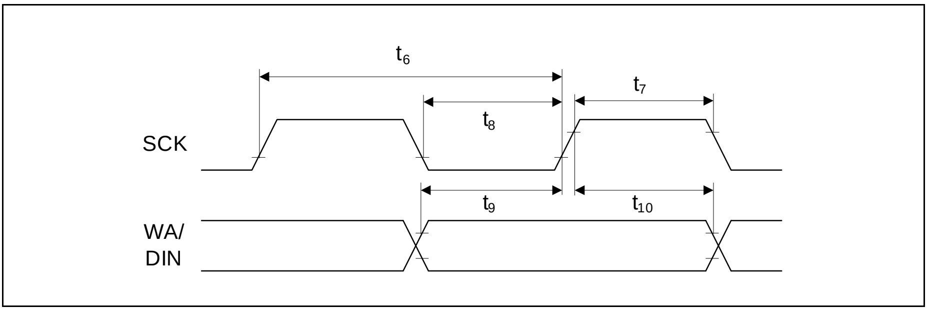

Figure 34 USIC IIS Slave Receiver Timing

4 Package and Reliability

The XMC4[12]00 is a member of the XMC4000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the Exposed Die Pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 55 provides the thermal characteristics of the packages used in XMC4[12]00. The availability of different packages for different markings is listed in **Table 2**.

Table 55 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad Dimensions	Ex × Ey CC	-	5.8 × 5.8	mm	PG-LQFP-64-19
		-	5.7 × 5.7	mm	PG-TQFP-64-19
		-	5.2 × 5.2	mm	PG-VQFN-48-53
		-	5.2 × 5.2	mm	PG-VQFN-48-71
Thermal resistance Junction-Ambient	$R_{\Theta JA}$ CC	-	30	K/W	PG-LQFP-64-19[1)]
		-	23.4	K/W	PG-TQFP-64-19[1)]
		-	34.8	K/W	PG-VQFN-48-53[1)] PG-VQFN-48-71[1)]

1) Device mounted on a 4-layer JEDEC board (JESD 51-7) with thermal vias; exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SS}, independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMC4[12]00 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The "Thermal resistance $R_{\Theta JA}$" quantifies these parameters. The