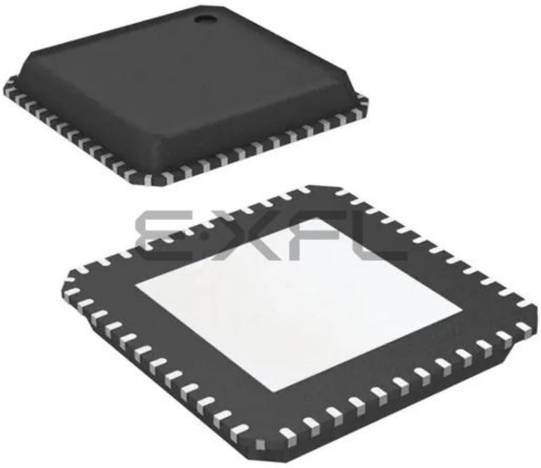

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 9x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-53
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4104q48f64abxuma1

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2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

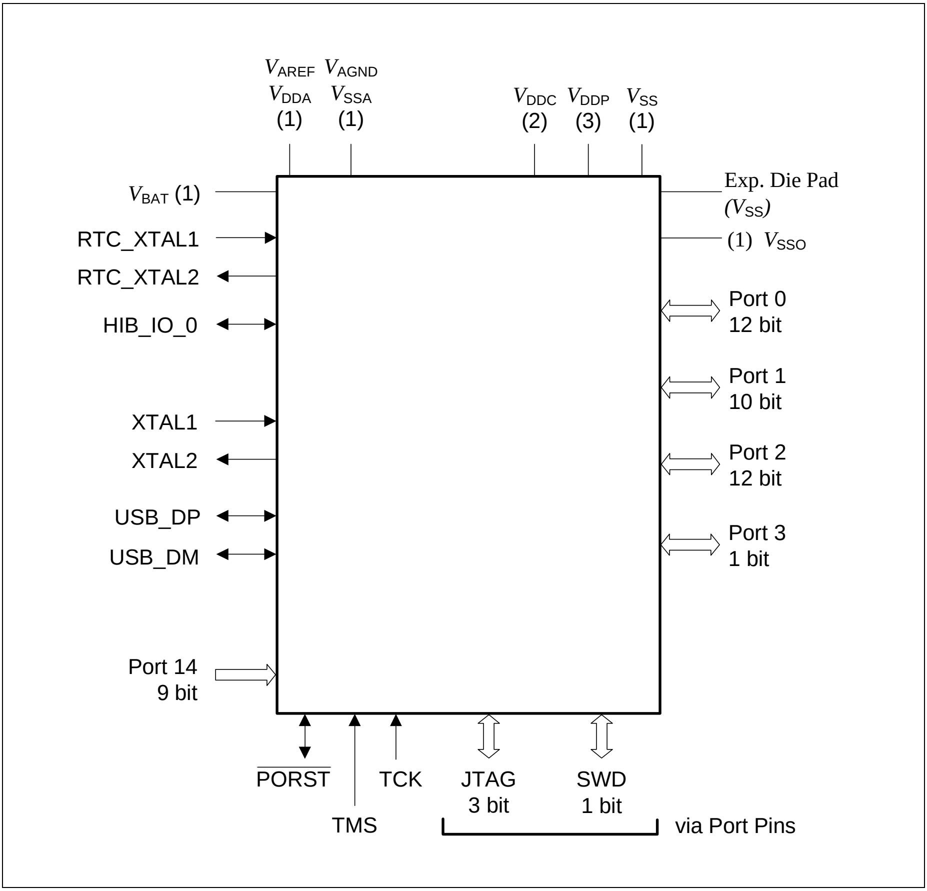

Figure 2 XMC4[12]00 Logic Symbol PG-LQFP-64 and PG-TQFP-64

2.2.2.1 Port I/O Function Table

Table 13 Port I/O Functions

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO0	HWI0	Input	Input	Input	Input	Input	Input	Input	Input
P0.0		CAN.N0_TXD	CCU80.OUT21	LEDTS0.COL2			U1C1.DX0D		ERU0.0B0	USB.VBUSDETECTA		HRPWM0.C1INB		
P0.1		U1C1.DOUT0	CCU80.OUT11	LEDTS0.COL3					ERU0.0A0			HRPWM0.C2INB		
P0.2		U1C1.SELO1	CCU80.OUT01	HRPWM0.HROUT01	U1C0.DOUT3	U1C0.HWIN3			ERU0.3B3					
P0.3			CCU80.OUT20	HRPWM0.HROUT20	U1C0.DOUT2	U1C0.HWIN2				ERU1.3B0				
P0.4			CCU80.OUT10	HRPWM0.HROUT21	U1C0.DOUT1	U1C0.HWIN1		U1C0.DX0A	ERU0.2B3					
P0.5		U1C0.DOUT0	CCU80.OUT00	HRPWM0.HROUT00	U1C0.DOUT0	U1C0.HWIN0		U1C0.DX0B		ERU1.3A0				
P0.6		U1C0.SELO0	CCU80.OUT30	HRPWM0.HROUT30				U1C0.DX2A	ERU0.3B2		CCU80.IN2B			
P0.7	WWDT.SERVICE_OUT	U0C0.SELO0		HRPWM0.HROUT11		DB.TDI	U0C0.DX2B		ERU0.2B1		CCU80.IN0A	CCU80.IN1A	CCU80.IN2A	CCU80.IN3A
P0.8	SCU.EXTCLK	U0C0.SCLKOUT		HRPWM0.HROUT10		DB.$\overline{\text{TRST}}$	U0C0.DX1B		ERU0.2A1		CCU80.IN1B			
P0.9	HRPWM0.HROUT31	U1C1.SELO0	CCU80.OUT12	LEDTS0.COL0			U1C1.DX2A		ERU0.1B0					
P0.10		U1C1.SCLKOUT	CCU80.OUT02	LEDTS0.COL1			U1C1.DX1A		ERU0.1A0					
P0.11		U1C0.SCLKOUT	CCU80.OUT31					U1C0.DX1A	ERU0.3A2					
P1.0		U0C0.SELO0	CCU40.OUT3	ERU1.PDOUT3			U0C0.DX2A		ERU0.3B0		CCU40.IN3A	HRPWM0.C0INA		
P1.1		U0C0.SCLKOUT	CCU40.OUT2	ERU1.PDOUT2			U0C0.DX1A	POSIF0.IN2A	ERU0.3A0		CCU40.IN2A	HRPWM0.C1INA		
P1.2			CCU40.OUT1	ERU1.PDOUT1	U0C0.DOUT3	U0C0.HWIN3		POSIF0.IN1A		ERU1.2B0	CCU40.IN1A	HRPWM0.C2INA		
P1.3		U0C0.MCLKOUT	CCU40.OUT0	ERU1.PDOUT0	U0C0.DOUT2	U0C0.HWIN2		POSIF0.IN0A		ERU1.2A0	CCU40.IN0A	HRPWM0.C0INB		
P1.4	WWDT.SERVICE_OUT	CAN.N0_TXD	CCU80.OUT33		U0C0.DOUT1	U0C0.HWIN1	U0C0.DX0B	CAN.N1_RXDD	ERU0.2B0		CCU41.IN0C	HRPWM0.BL0A		
P1.5	CAN.N1_TXD	U0C0.DOUT0	CCU80.OUT23		U0C0.DOUT0	U0C0.HWIN0	U0C0.DX0A	CAN.N0_RXDA	ERU0.2A0	ERU1.0A0	CCU41.IN1C			
P1.7		U0C0.DOUT0		U1C1.SELO2						USB.VBUSDETECTB				

Table 13 Port I/O Functions (cont'd)

Function	Output					Input								
	ALT1	**ALT2**	**ALT3**	**ALT4**	**HWO0**	**HWI0**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**
P1.8		U0C0. SELO1		U1C1. SCLKOUT										
P1.9	U0C0. SCLKOUT			U1C1. DOUT0										
P1.15	SCU. EXTCLK			U1C0. DOUT0						ERU1. 1A0				
P2.0	CAN. N0_TXD			LEDTS0. COL1					ERU0. 0B3		CCU40. IN1C			
P2.1				LEDTS0. COL0	DB.TDO/ TRACESWO					ERU1. 0B0	CCU40. IN0C			
P2.2	VADC. EMUX00		CCU41. OUT3	LEDTS0. LINE0	LEDTS0. EXTENDED0	LEDTS0. TSIN0A		U0C1. DX0A	ERU0. 1B2		CCU41. IN3A			
P2.3	VADC. EMUX01	U0C1. SELO0	CCU41. OUT2	LEDTS0. LINE1	LEDTS0. EXTENDED1	LEDTS0. TSIN1A		U0C1. DX2A	ERU0. 1A2		CCU41. IN2A			
P2.4	VADC. EMUX02	U0C1. SCLKOUT	CCU41. OUT1	LEDTS0. LINE2	LEDTS0. EXTENDED2	LEDTS0. TSIN2A		U0C1. DX1A	ERU0. 0B2		CCU41. IN1A	HRPWM0. BL1A		
P2.5		U0C1. DOUT0	CCU41. OUT0	LEDTS0. LINE3	LEDTS0. EXTENDED3	LEDTS0. TSIN3A		U0C1. DX0B	ERU0. 0A2		CCU41. IN0A	HRPWM0. BL2A		
P2.6			CCU80. OUT13	LEDTS0. COL3				CAN. N1_RXDA	ERU0. 1B3		CCU40. IN3C			
P2.7		CAN. N1_TXD	CCU80. OUT03	LEDTS0. COL2						ERU1. 1B0	CCU40. IN2C			
P2.8			CCU80. OUT32	LEDTS0. LINE4	LEDTS0. EXTENDED4	LEDTS0. TSIN4A	DAC. TRIGGER5				CCU40. IN0B	CCU40. IN1B	CCU40. IN2B	CCU40. IN3B
P2.9			CCU80. OUT22	LEDTS0. LINE5	LEDTS0. EXTENDED5	LEDTS0. TSIN5A	DAC. TRIGGER4				CCU41. IN0B	CCU41. IN1B	CCU41. IN2B	CCU41. IN3B
P2.14	VADC. EMUX11	U1C0. DOUT0	CCU80. OUT21					U1C0. DX0D						
P2.15	VADC. EMUX12		CCU80. OUT11	LEDTS0. LINE6	LEDTS0. EXTENDED6	LEDTS0. TSIN6A		U1C0. DX0C						
P3.0		U0C1. SCLKOUT					U0C1. DX1B				CCU80. IN2C			
P14.0							VADC. G0CH0							
P14.3							VADC. G0CH3	VADC. G1CH3			CAN. N0_RXDB			
P14.4							VADC. G0CH4							
P14.5							VADC. G0CH5				POSIF0. IN2B			
P14.6							VADC. G0CH6				POSIF0. IN1B		G0ORC6	
P14.7							VADC. G0CH7				POSIF0. IN0B			
P14.8					DAC. OUT_0			VADC. G1CH0						

2.3 Power Connection Scheme

Figure 7. shows a reference power connection scheme for the XMC4[12]00.

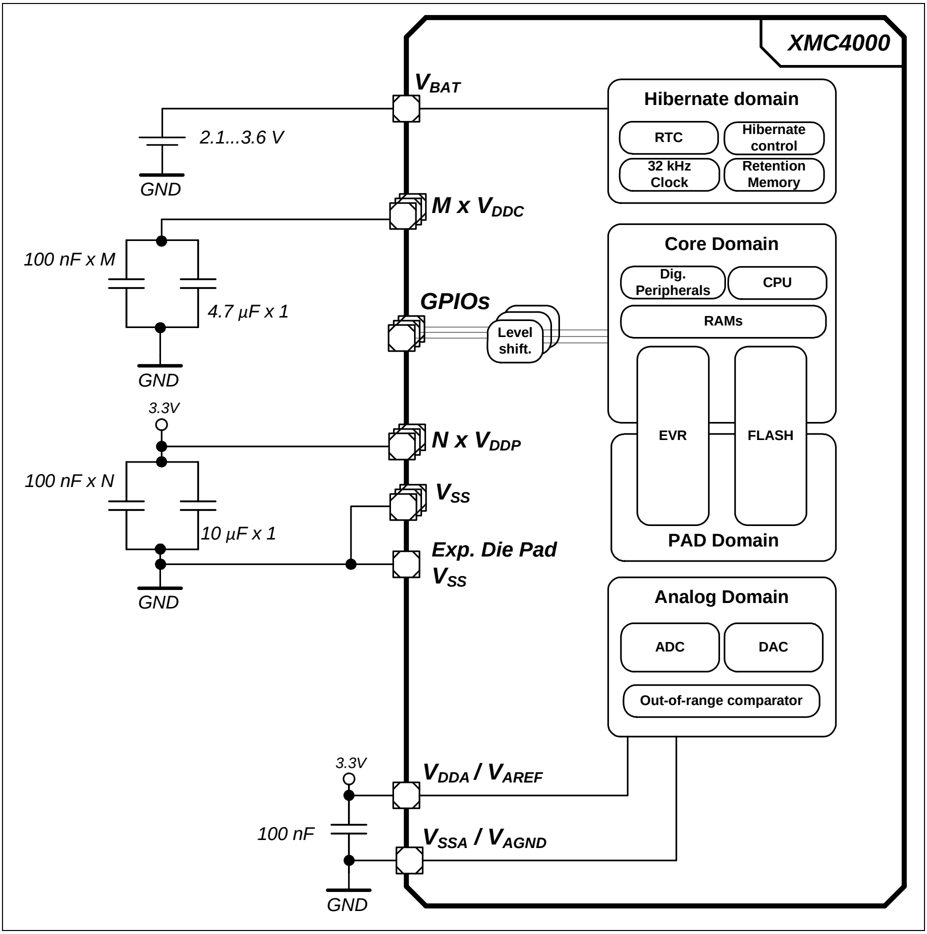

Figure 7 Power Connection Scheme

Every power supply pin needs to be connected. Different pins of the same supply need also to be externally connected. As example, all V_{DDP} pins must be connected externally to one V_{DDP} net. In this reference scheme one 100 nF capacitor is connected at each supply pin against V_{SS}. An additional 10 µF capacitor is connected to the V_{DDP} nets and an additional 4.7uF capacitor to the V_{DDC} nets.

Figure 8 explains the input voltage ranges of V_{IN} and V_{AIN} and its dependency to the supply level of V_{DDP}.The input voltage must not exceed 4.3 V, and it must not be more than 1.0 V above V_{DDP}. For the range up to V_{DDP} + 1.0 V also see the definition of the overload conditions in **Section 3.1.3**.

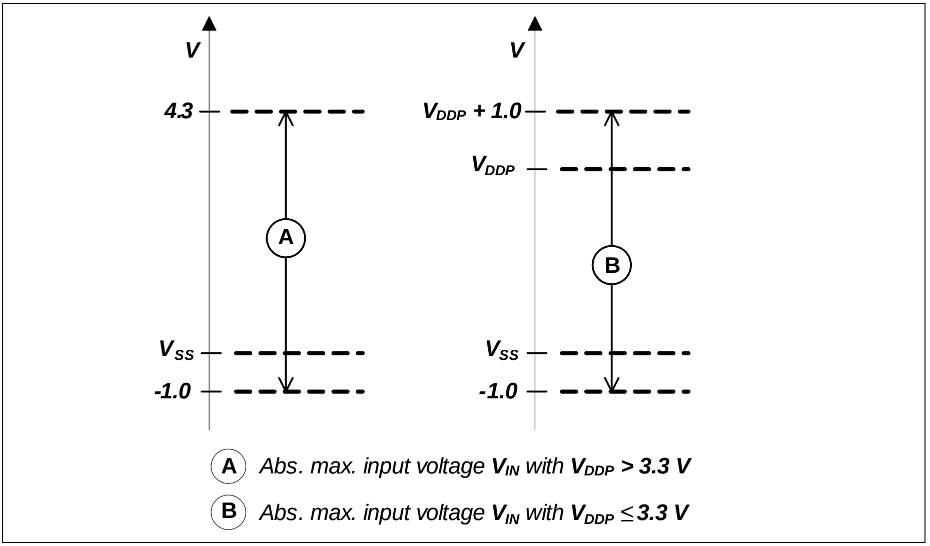

Figure 8 Absolute Maximum Input Voltage Ranges

3.2.2 Analog to Digital Converters (ADCx)

Table 25 ADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog reference voltage	V_{AREF} SR	–	–	–	V	$V_{AREF} = V_{DDA}$ shared analog supply and reference input pin
Alternate reference voltage[5)]	V_{AREF} SR	$V_{AGND} + 1$	–	$V_{DDA} + 0.05$[1)]	V	
Analog reference ground	V_{AGND} SR	–	–	–	V	$V_{AGND} = V_{SSA}$ shared analog supply and reference input pin
Alternate reference voltage range[2)5)]	V_{AREF} - V_{AGND} SR	1	–	$V_{DDA} + 0.1$	V	
Analog input voltage	V_{AIN} SR	V_{AGND}	–	V_{DDA}	V	
Input leakage at analog inputs[3)]	I_{OZ1} CC	-100	–	200	nA	$0.03 \times V_{DDA} < V_{AIN} < 0.97 \times V_{DDA}$
		-500	–	100	nA	$0\ V \leq V_{AIN} \leq 0.03 \times V_{DDA}$
		-100	–	500	nA	$0.97 \times V_{DDA} \leq V_{AIN} \leq V_{DDA}$
Internal ADC clock	f_{ADCI} CC	2	–	30	MHz	$V_{DDA} = 3.3\ V$
Switched capacitance at the analog voltage inputs[4)]	C_{AINSW} CC	–	4	6.5	pF	
Total capacitance of an analog input	C_{AINTOT} CC	–	12	20	pF	
Switched capacitance at the alternate reference voltage input[5)6)]	C_{AREFSW} CC	–	15	30	pF	

9) The resulting current for a conversion can be calculated with $I_{AREF} = Q_{CONV} / t_c$.
The fastest 12-bit post-calibrated conversion of t_c = 566 ns results in a typical average current of I_{AREF} = 53 µA.

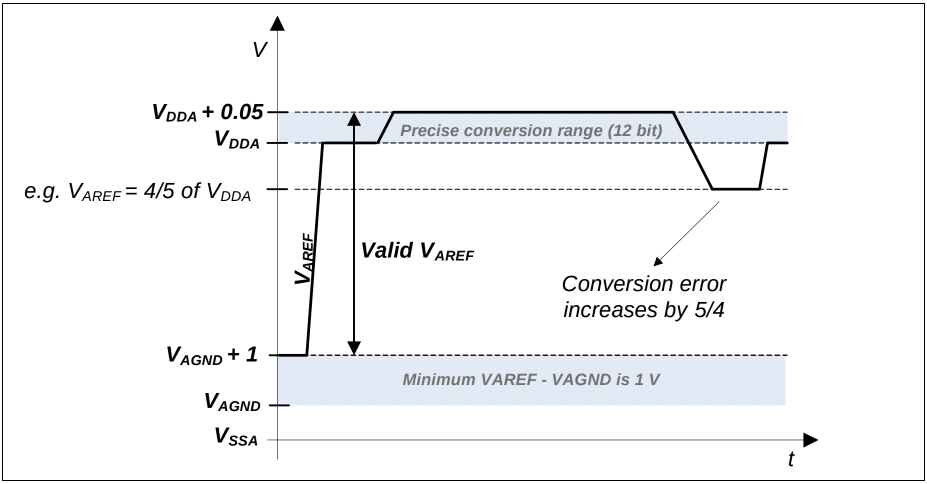

Figure 12 VADC Reference Voltage Range

3.2.3 Digital to Analog Converters (DACx)

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 27 DAC Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
RMS supply current	I_{DD}	CC	–	2.5	4	mA	per active DAC channel, without load currents of DAC outputs
Resolution	RES	CC	–	12	–	Bit	
Update rate	f_{URATE_A}	CC	–		2	Msample/s	data rate, where DAC can follow 64 LSB code jumps to ± 1LSB accuracy
Update rate	f_{URATE_F}	CC	–		5	Msample/s	data rate, where DAC can follow 64 LSB code jumps to ± 4 LSB accuracy
Settling time	t_{SETTLE}	CC	–	1	2	µs	at full scale jump, output voltage reaches target value ± 20 LSB
Slew rate	SR	CC	2	5	–	V/µs	
Minimum output voltage	V_{OUT_MIN}	CC	–	0.3	–	V	code value unsigned: 000_H; signed: 800_H
Maximum output voltage	V_{OUT_MAX}	CC	–	2.5	–	V	code value unsigned: FFF_H; signed: $7FF_H$
Integral non-linearity[1]	INL	CC	-5.5	±2.5	5.5	LSB	$R_L \geq 5$ kOhm, $C_L \leq 50$ pF
Differential non-linearity	DNL	CC	-2	±1	2	LSB	$R_L \geq 5$ kOhm, $C_L \leq 50$ pF

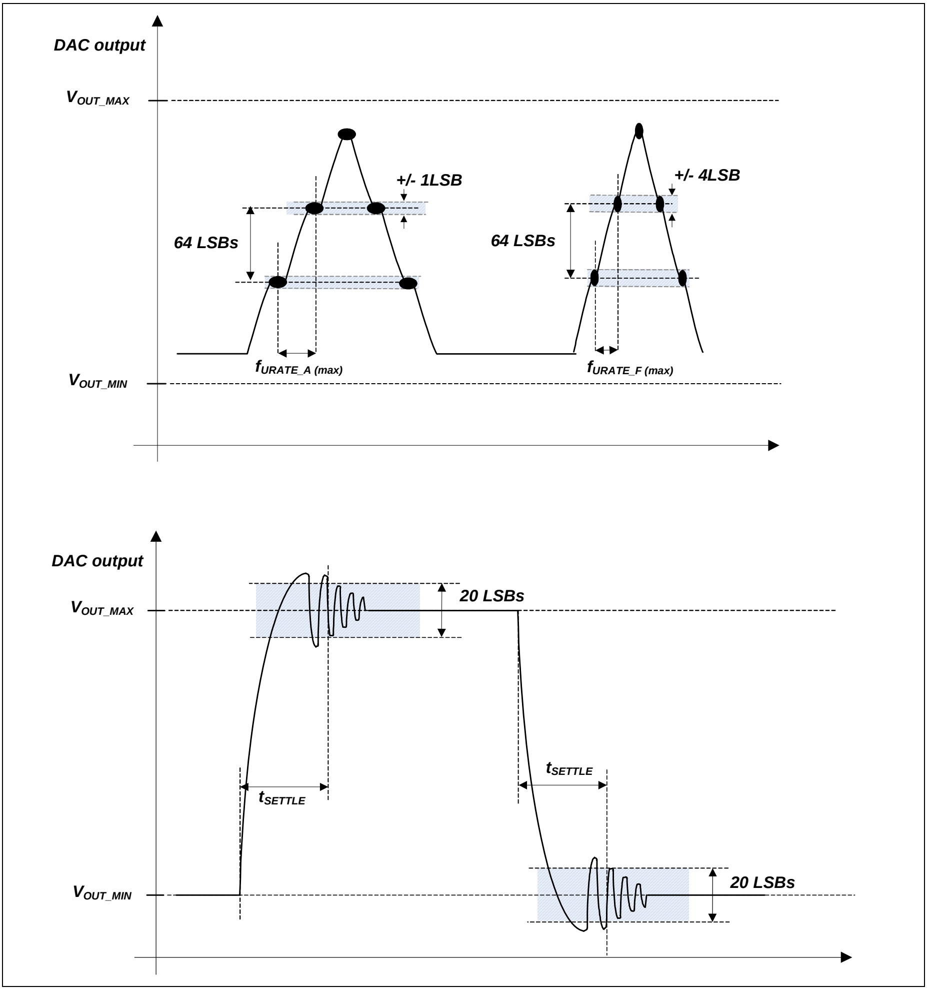

Figure 15 DAC Conversion Examples

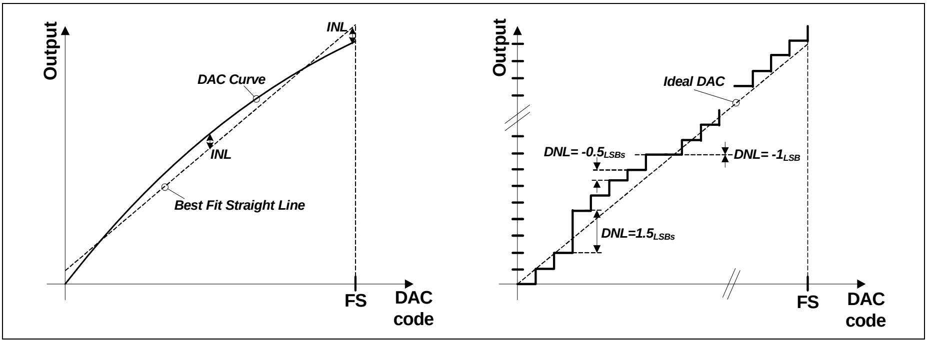

Figure 18 CSG DAC INL and DNL example

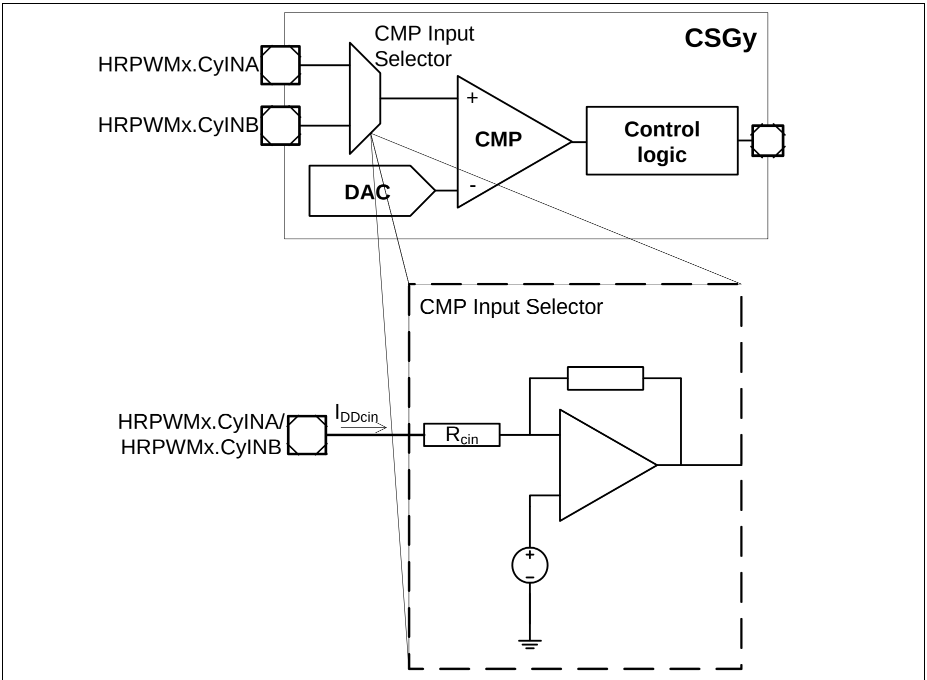

Figure 19 Input operation current

3.2.11 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 40 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase Time per 256 Kbyte Sector	t_{ERP} CC	–	5	5.5	s	
Erase Time per 64 Kbyte Sector	t_{ERP} CC	–	1.2	1.4	s	
Erase Time per 16 Kbyte Logical Sector	t_{ERP} CC	–	0.3	0.4	s	
Program time per page[1]	t_{PRP} CC	–	5.5	11	ms	
Erase suspend delay	t_{FL_ErSusp} CC	–	–	15	ms	
Wait time after margin change	$t_{FL\_MarginDel}$ CC	10	–	–	µs	
Wake-up time	t_{WU} CC	–	–	270	µs	
Read access time	t_a CC	20	–	–	ns	For operation with $1 / f_{CPU} < t_a$ wait states must be configured[2]
Data Retention Time, Physical Sector[3)4)]	t_{RET} CC	20	–	–	years	Max. 1000 erase/program cycles
Data Retention Time, Logical Sector[3)4)]	t_{RETL} CC	20	–	–	years	Max. 100 erase/program cycles

3.3.2 Power-Up and Supply Monitoring

$\overline{\text{PORST}}$ is always asserted when V_{DDP} and/or V_{DDC} violate the respective thresholds.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

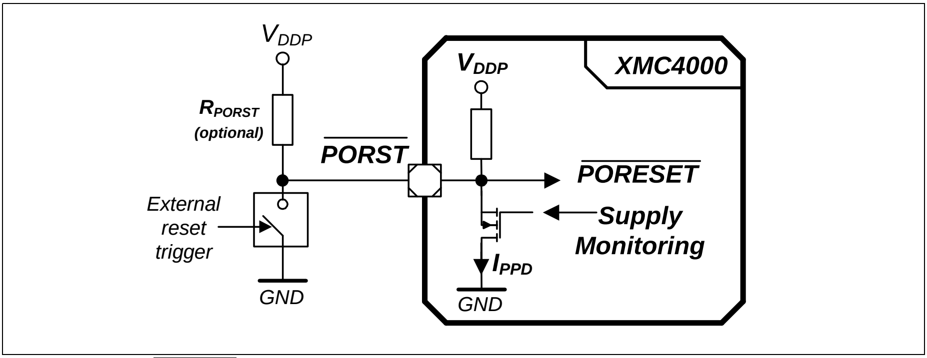

Figure 26 $\overline{\text{PORST}}$ Circuit

Table 41 Supply Monitoring Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage reset threshold	V_{POR} CC	2.79[1]	–	3.05[2]	V	[3]
Core supply voltage reset threshold	V_{PV} CC	–	–	1.17	V	
V_{DDP} voltage to ensure defined pad states	V_{DDPPA} CC	–	1.0	–	V	
$\overline{\text{PORST}}$ rise time	t_{PR} SR	–	–	2	µs	
Startup time from power-on reset with code execution from Flash	t_{SSW} CC	–	2.5	3.5	ms	Time to the first user code instruction
V_{DDC} ramp up time	t_{VCR} CC	–	550	–	µs	Ramp up after power-on or after a reset triggered by a violation of V_{POR} or V_{PV}

1) Minimum threshold for reset assertion.

2) Maximum threshold for reset deassertion.
3) The V_{DDP} monitoring has a typical hysteresis of V_{PORHYS} = 180 mV.

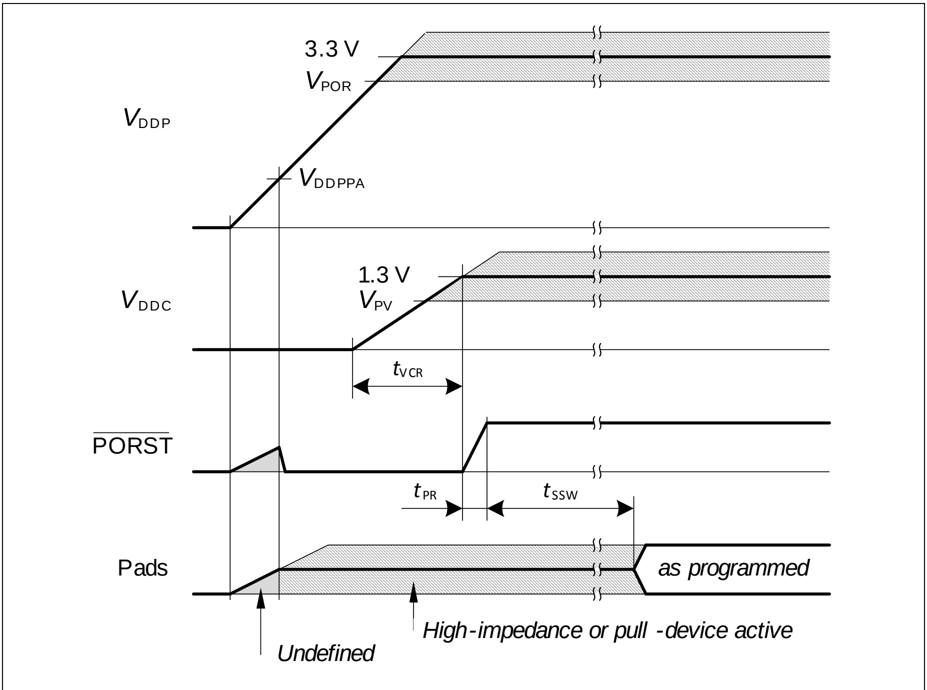

Figure 27 Power-Up Behavior

3.3.3 Power Sequencing

While starting up and shutting down as well as when switching power modes of the system it is important to limit the current load steps. A typical cause for such load steps is changing the CPU frequency f_{CPU}. Load steps exceeding the below defined values may cause a power on reset triggered by the supply monitor.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 42 Power Sequencing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Positive Load Step Current	ΔI_{PLS} SR	-	–	50	mA	Load increase on V_{DDP} $\Delta t \leq 10$ ns
Negative Load Step Current	ΔI_{NLS} SR	-	–	150	mA	Load decrease on V_{DDP} $\Delta t \leq 10$ ns
V_{DDC} Voltage Over- / Undershoot from Load Step	ΔV_{LS} CC	-	–	±100	mV	For maximum positive or negative load step
Positive Load Step Settling Time	t_{PLSS} SR	50	–	-	µs	
Negative Load Step Settling Time	t_{NLSS} SR	100	–	-	µs	
External Buffer Capacitor on V_{DDC}	C_{EXT} SR	3	4.7	6	µF	In addition C = 100 nF capacitor on each V_{DDC} pin

Positive Load Step Examples

System assumptions:
$f_{CPU} = f_{SYS}$, target frequency f_{CPU} = 80 MHz, main PLL f_{VCO} = 480 MHz, stepping done by K2 divider, t_{PLSS} between individual steps:

24 MHz - 48 MHz - 80 MHz (K2 steps 20 - 10 - 6)
24 MHz - 60 MHz - 80 MHz (K2 steps 20 - 8 - 6)

Table 49 USIC SSC Slave Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DX1 slave clock period	t_{CLK}	SR	66.6	–	–	ns	
Select input DX2 setup to first clock input DX1 transmit edge[1]	t_{10}	SR	3	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1]	t_{11}	SR	4	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1]	t_{12}	SR	6	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1]	t_{13}	SR	4	–	–	ns	
Data output DOUT[3:0] valid time	t_{14}	CC	0	–	24	ns	

1) These input timing are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

power dissipation must be limited so that the average junction temperature does not exceed 150 °C.

The difference between junction temperature and ambient temperature is determined by
$\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

4.2 Package Outlines

The availability of different packages for different devices types is listed in **Table 1**, specific packages for different device markings are listed in **Table 2**.

The exposed die pad dimensions are listed in **Table 55**.

Table 56 Differences PG-LQFP-64-19 to PG-TQFP-64-19

Change	PG-LQFP-64-19	PG-TQFP-64-19
Thermal Resistance Junction Ambient ($R_{\Theta JA}$)	30 K/W	23.4 K/W
Package thickness	$1.4^{\pm 0.05}$ mm	$1.0^{\pm 0.05}$ mm
	1.6 mm MAX	1.2 mm MAX
Exposed Die Pad size	5.8 mm × 5.8 mm	5.7 mm × 5.7 mm

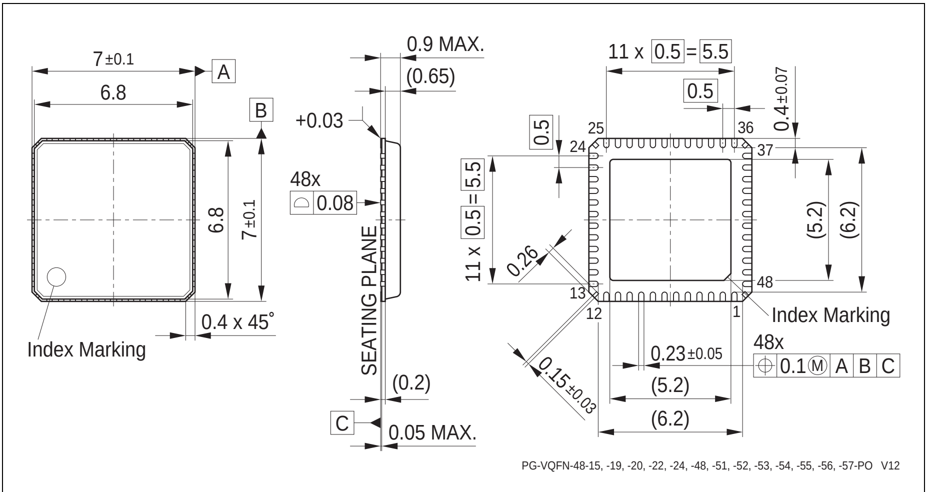

Figure 38 **PG-VQFN-48-53** (Plastic Green Very Thin Profile Flat Non Leaded Package)

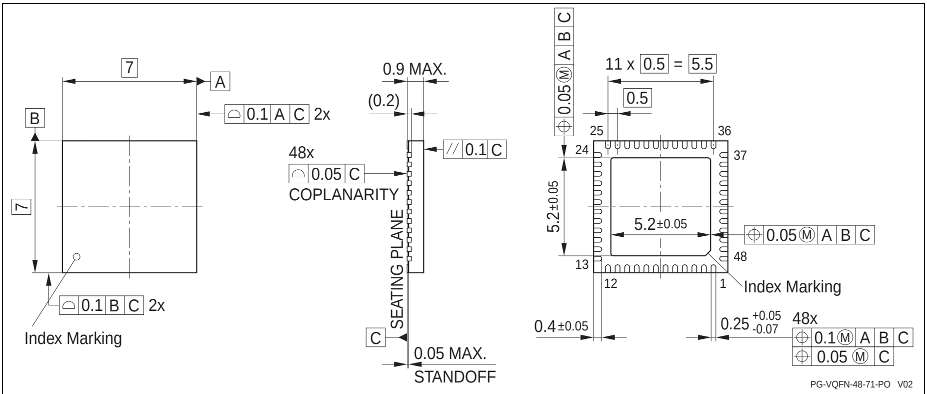

Figure 39 **PG-VQFN-48-71** (Plastic Green Very Thin Profile Flat Non Leaded Package)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page “Packages”: **http://www.infineon.com/packages**

5 Quality Declarations

The qualification of the XMC4[12]00 is executed according to the JEDEC standard JESD47H.

Note: For automotive applications refer to the Infineon automotive microcontrollers.

Table 58 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation lifetime	t_{OP} CC	20	–	–	a	$T_J \leq 109°C$, device permanent on
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	–	2 000	V	EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} SR	–	–	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	–	–	3	–	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	–	–	260	°C	Profile according to JEDEC J-STD-020D