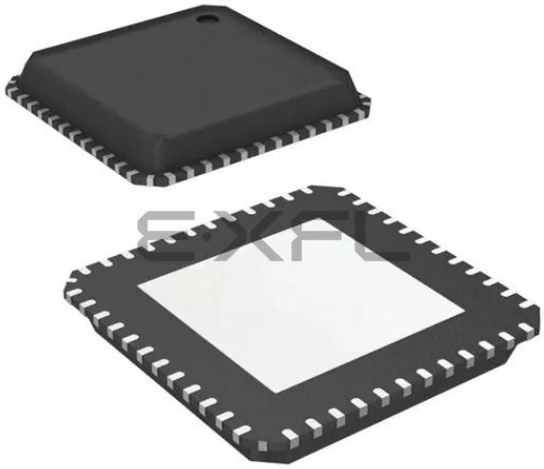
Infineon Technologies - XMC4104Q48K128ABXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 9x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-53
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4104q48k128abxuma1

XMC4[12]00 Data Sheet

Revision History: V1.3 2015-10

Previous Versions:
V1.2 2014-06
V1.1 2014-03
V1.0 2013-10
V0.6 2012-11

Page	Subjects
12	Added a section listing the packages of the different markings.
14	Added BA marking variant.
14	Corrected SCU_IDCHIP value of XMC4100 EES-AA/ES-AA.
36	Added footnote explaining minimum V_{BAT} requirements to start the hibernate domain and/or oscillation of a crystal on RTC_XTAL.
37	Changed pull device definition to System Requirement (SR) to reflect that the specified currents are defined by the characteristics of the external load/driver.
37	Added information that $\overline{\text{PORST}}$ Pull-up is identical to the pull-up on standard I/O pins.
42	Updated C_{AINSW}, C_{AINTOT} and R_{AIN} parameters with improved values.
56	Added footnote on test configuration for LPAC measurement.
58	Corrected parameter name of of USB pull device (upstream port receiving) definition according to USB standard (referenced to DM instead of DP)
62	Relaxed RTC_XTAL V_{PPX} parameter value and changed it to a system requirement.
66	Added footnote on current consumption by enabling of f_{CCU}.
67	Added Flash endurance parameter for 64 Kbytes Physical Sector PS4 N_{EPS4} for devices with BA marking.
many	Added PG-TQFP-64-19 and PG-VQFN-48-71 package information.
89, 91	Added tables describing the differences between PG-LQFP-64-19 to PG-TQFP-64-19 as well as PG-VQFN-48-53 to PG-VQFN-48-71 packages.
93	Updated to JEDEC standard J-STD-020D for the moisture sensitivity level and added solder temperature parameter according to the same standard.

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1 Summary of Features

The XMC4[12]00 devices are members of the XMC4000 Family of microcontrollers based on the ARM Cortex-M4 processor core. The XMC4000 is a family of high performance and energy efficient microcontrollers optimized for Industrial Connectivity, Industrial Control, Power Conversion, Sense & Control.

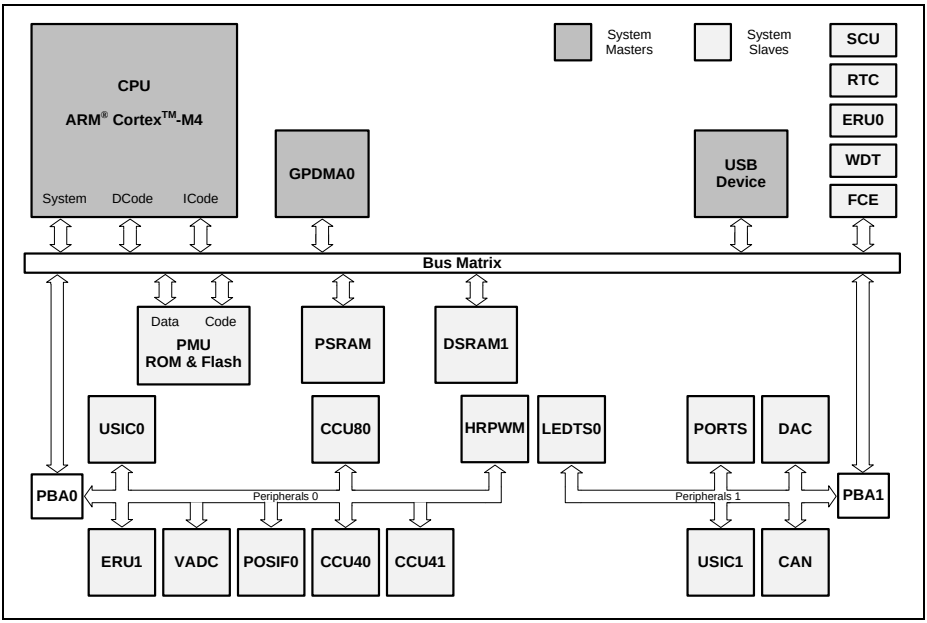

Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
  - High Performance 32-bit ARM Cortex-M4 CPU
  - 16-bit and 32-bit Thumb2 instruction set
  - DSP/MAC instructions
  - System timer (SysTick) for Operating System support
- Floating Point Unit
- Memory Protection Unit
- Nested Vectored Interrupt Controller
- One General Purpose DMA with up-to 8 channels
- Event Request Unit (ERU) for programmable processing of external and internal service requests
- Flexible CRC Engine (FCE) for multiple bit error detection

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Table 6 SRAM Memory Ranges

Total SRAM Size	Program SRAM	System Data SRAM
40 Kbytes	1FFF C000$_H$ – 1FFF FFFF$_H$	2000 0000$_H$ – 2000 5FFF$_H$
20 Kbytes	1FFF E000$_H$ – 1FFF FFFF$_H$	2000 0000$_H$ – 2000 2FFF$_H$

Table 7 ADC Channels[1)]

Package	VADC G0	VADC G1
LQFP-64, TQFP-64	CH0, CH3..CH7	CH0, CH1, CH3, CH6
PG-VQFN-48	CH0, CH3..CH7	CH0, CH1, CH3

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

1.6 Identification Registers

The identification registers allow software to identify the marking.

Table 8 XMC4200 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	0004 2001$_H$	EES-AA, ES-AA
SCU_IDCHIP	0004 2002$_H$	ES-AB, AB
SCU_IDCHIP	0004 2003$_H$	BA
JTAG IDCODE	101D D083$_H$	EES-AA, ES-AA
JTAG IDCODE	201D D083$_H$	ES-AB, AB
JTAG IDCODE	301D D083$_H$	BA

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Table 9 XMC4100 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	0004 2001$_H$	EES-AA, ES-AA
SCU_IDCHIP	0004 2002$_H$	ES-AB, AB
SCU_IDCHIP	0004 1003$_H$	BA
JTAG IDCODE	101D D083$_H$	EES-AA, ES-AA
JTAG IDCODE	201D D083$_H$	ES-AB, AB
JTAG IDCODE	301D D083$_H$	BA

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2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

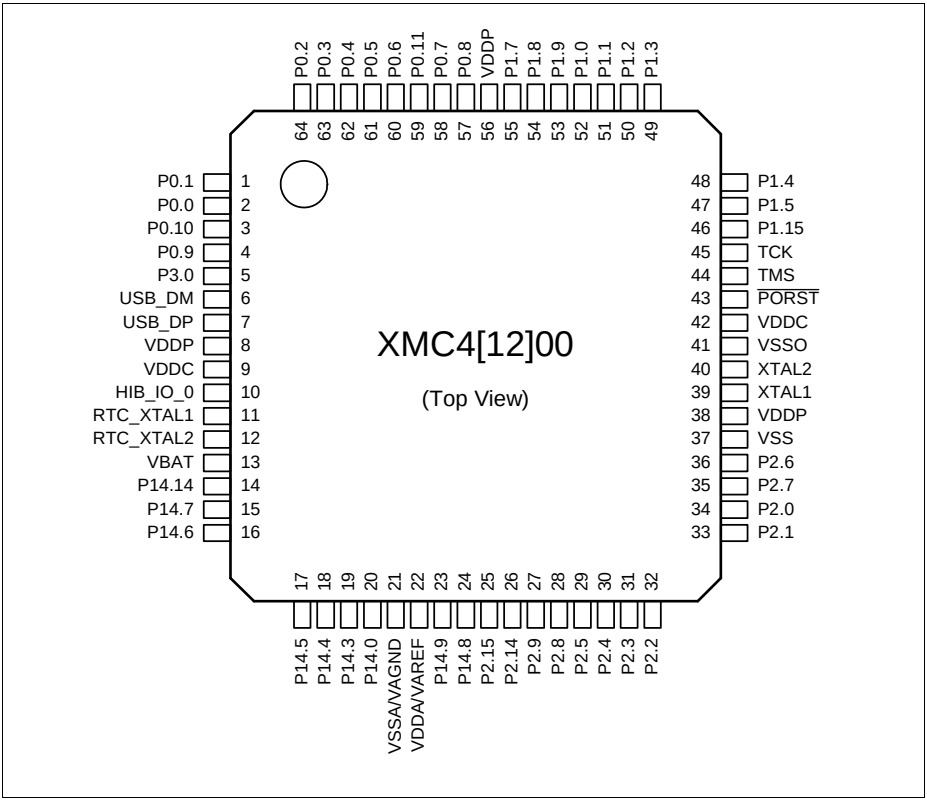

Figure 4 XMC4[12]00 PG-LQFP-64 and PG-TQFP-64 Pin Configuration (top view)

Table 11 Package Pin Mapping (cont'd)

Function	LQFP-64 TQFP-64	VQFN-48	Pad Type	Notes
P14.9	23	19	AN/DAC/DIG_IN	
P14.14	14	-	AN/DIG_IN	
USB_DP	7	4	special	
USB_DM	6	3	special	
HIB_IO_0	10	7	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as open-drain output and drives "0". As output the medium driver mode is active.
TCK	45	34	A1	Weak pull-down active.
TMS	44	33	A1+	Weak pull-up active. As output the strong-soft driver mode is active.
$\overline{\text{PORST}}$	43	32	special	Strong pull-down controlled by EVR. Weak pull-up active while strong pull-down is not active.
XTAL1	39	29	clock_IN	
XTAL2	40	30	clock_O	
RTC_XTAL1	11	8	clock_IN	
RTC_XTAL2	12	9	clock_O	
VBAT	13	10	Power	When VDDP is supplied VBAT has to be supplied as well.
VDDA/VAREF	22	18	AN_Power/AN_ Ref	Shared analog supply and reference voltage pin.
VSSA/VAGND	21	17	AN_Power/AN_ Ref	Shared analog supply and reference ground pin.
VDDC	9	6	Power	
VDDC	42	31	Power	
VDDP	8	5	Power	
VDDP	38	28	Power	
VDDP	56	41	Power	
VSS	37	27	Power	

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Table 13 Port I/O Functions (cont'd)

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO0	HWI0	Input	Input	Input	Input	Input	Input	Input	Input
P1.8		U0C0. SELO1		U1C1. SCLKOUT										
P1.9	U0C0. SCLKOUT			U1C1. DOUT0										
P1.15	SCU. EXTCLK			U1C0. DOUT0						ERU1. 1A0				
P2.0	CAN. N0_TXD			LEDTS0. COL1					ERU0. 0B3		CCU40. IN1C			
P2.1				LEDTS0. COL0	DB.TDO/ TRACESWO					ERU1. 0B0	CCU40. IN0C			
P2.2	VADC. EMUX00		CCU41. OUT3	LEDTS0. LINE0	LEDTS0. EXTENDED0	LEDTS0. TSIN0A		U0C1. DX0A	ERU0. 1B2		CCU41. IN3A			
P2.3	VADC. EMUX01	U0C1. SELO0	CCU41. OUT2	LEDTS0. LINE1	LEDTS0. EXTENDED1	LEDTS0. TSIN1A		U0C1. DX2A	ERU0. 1A2		CCU41. IN2A			
P2.4	VADC. EMUX02	U0C1. SCLKOUT	CCU41. OUT1	LEDTS0. LINE2	LEDTS0. EXTENDED2	LEDTS0. TSIN2A		U0C1. DX1A	ERU0. 0B2		CCU41. IN1A	HRPWM0. BL1A		
P2.5		U0C1. DOUT0	CCU41. OUT0	LEDTS0. LINE3	LEDTS0. EXTENDED3	LEDTS0. TSIN3A		U0C1. DX0B	ERU0. 0A2		CCU41. IN0A	HRPWM0. BL2A		
P2.6			CCU80. OUT13	LEDTS0. COL3				CAN. N1_RXDA	ERU0. 1B3		CCU40. IN3C			
P2.7		CAN. N1_TXD	CCU80. OUT03	LEDTS0. COL2						ERU1. 1B0	CCU40. IN2C			
P2.8			CCU80. OUT32	LEDTS0. LINE4	LEDTS0. EXTENDED4	LEDTS0. TSIN4A	DAC. TRIGGER5				CCU40. IN0B	CCU40. IN1B	CCU40. IN2B	CCU40. IN3B
P2.9			CCU80. OUT22	LEDTS0. LINE5	LEDTS0. EXTENDED5	LEDTS0. TSIN5A	DAC. TRIGGER4				CCU41. IN0B	CCU41. IN1B	CCU41. IN2B	CCU41. IN3B
P2.14	VADC. EMUX11	U1C0. DOUT0	CCU80. OUT21					U1C0. DX0D						
P2.15	VADC. EMUX12		CCU80. OUT11	LEDTS0. LINE6	LEDTS0. EXTENDED6	LEDTS0. TSIN6A		U1C0. DX0C						
P3.0		U0C1. SCLKOUT					U0C1. DX1B				CCU80. IN2C			
P14.0							VADC. G0CH0							
P14.3							VADC. G0CH3	VADC. G1CH3			CAN. N0_RXDB			
P14.4							VADC. G0CH4							
P14.5							VADC. G0CH5				POSIF0. IN2B			
P14.6							VADC. G0CH6				POSIF0. IN1B		G0ORC6	
P14.7							VADC. G0CH7				POSIF0. IN0B			
P14.8					DAC. OUT_0			VADC. G1CH0						

3 Electrical Parameters

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the XMC4[12]00 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are a distinctive feature of the XMC4[12]00 and must be regarded for system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC4[12]00 is designed in.

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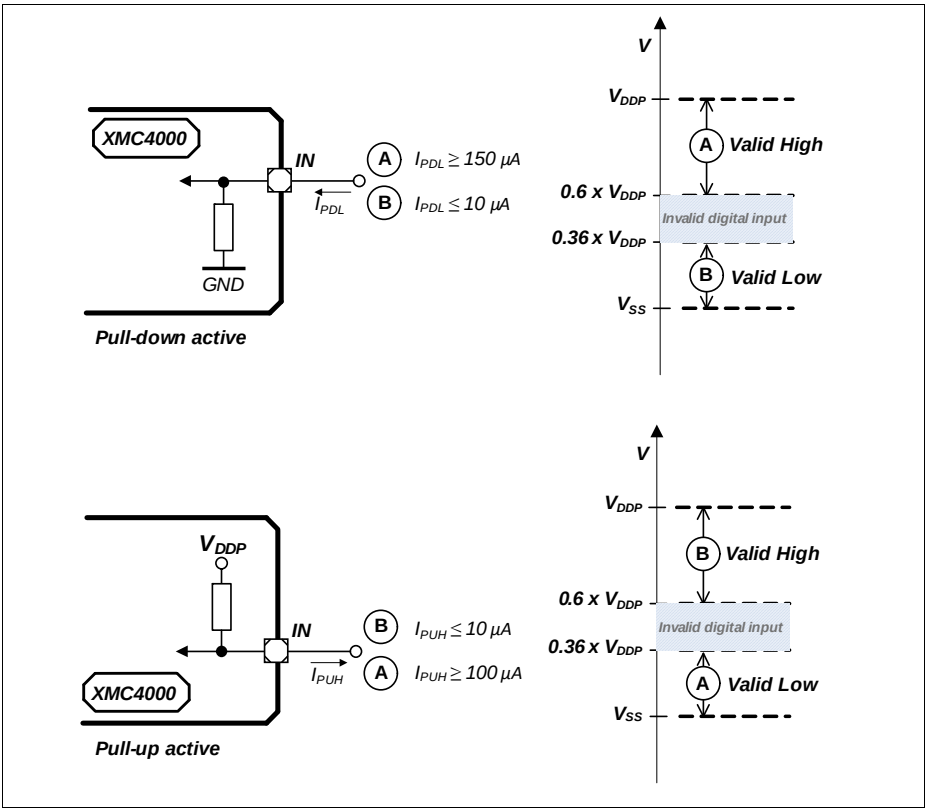

Figure 11 Pull Device Input Characteristics

Figure 11 visualizes the input characteristics with an active internal pull device:

- in the cases “A” the internal pull device is overridden by a strong external driver;
- in the cases “B” the internal pull device defines the input logical state against a weak external load.

Table 23 Standard Pads Class_A1+

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Output high voltage, POD[1] = weak	V_{OHA1+} CC	V_{DDP} - 0.4		–	V	$I_{OH} \geq$ -400 µA
		2.4		–	V	$I_{OH} \geq$ -500 µA
Output high voltage, POD[1] = medium		V_{DDP} - 0.4		–	V	$I_{OH} \geq$ -1.4 mA
		2.4		–	V	$I_{OH} \geq$ -2 mA
Output high voltage, POD[1] = strong		V_{DDP} - 0.4		–	V	$I_{OH} \geq$ -1.4 mA
		2.4		–	V	$I_{OH} \geq$ -2 mA
Output low voltage	V_{OLA1+} CC	–		0.4	V	$I_{OL} \leq$ 500 µA; POD[1] = weak
		–		0.4	V	$I_{OL} \leq$ 2 mA; POD[1] = medium
		–		0.4	V	$I_{OL} \leq$ 2 mA; POD[1] = strong
Fall time	t_{FA1+} CC	–		150	ns	C_L = 20 pF; POD[1] = weak
		–		50	ns	C_L = 50 pF; POD[1] = medium
		–		28	ns	C_L = 50 pF; POD[1] = strong; edge = slow
		–		16	ns	C_L = 50 pF; POD[1] = strong; edge = soft;
Rise time	t_{RA1+} CC	–		150	ns	C_L = 20 pF; POD[1] = weak
		–		50	ns	C_L = 50 pF; POD[1] = medium
		–		28	ns	C_L = 50 pF; POD[1] = strong; edge = slow
		–		16	ns	C_L = 50 pF; POD[1] = strong; edge = soft

1) POD = Pin Out Driver

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3.2.2 Analog to Digital Converters (ADCx)

Table 25 ADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog reference voltage	V_{AREF} SR	–	–	–	V	$V_{AREF} = V_{DDA}$ shared analog supply and reference input pin
Alternate reference voltage[5]	V_{AREF} SR	V_{AGND} + 1	–	V_{DDA} + 0.05[1]	V	
Analog reference ground	V_{AGND} SR	–	–	–	V	$V_{AGND} = V_{SSA}$ shared analog supply and reference input pin
Alternate reference voltage range[2][5]	V_{AREF} - V_{AGND} SR	1	–	V_{DDA} + 0.1	V	
Analog input voltage	V_{AIN} SR	V_{AGND}	–	V_{DDA}	V	
Input leakage at analog inputs[3]	I_{OZ1} CC	-100	–	200	nA	$0.03 \times V_{DDA} < V_{AIN} < 0.97 \times V_{DDA}$
		-500	–	100	nA	$0\ V \le V_{AIN} \le 0.03 \times V_{DDA}$
		-100	–	500	nA	$0.97 \times V_{DDA} \le V_{AIN} \le V_{DDA}$
Internal ADC clock	f_{ADCI} CC	2	–	30	MHz	V_{DDA} = 3.3 V
Switched capacitance at the analog voltage inputs[4]	C_{AINSW} CC	–	4	6.5	pF	
Total capacitance of an analog input	C_{AINTOT} CC	–	12	20	pF	
Switched capacitance at the alternate reference voltage input[5][6]	C_{AREFSW} CC	–	15	30	pF	

The power-up calibration of the ADC requires a maximum number of 4 352 f_{ADCI} cycles.

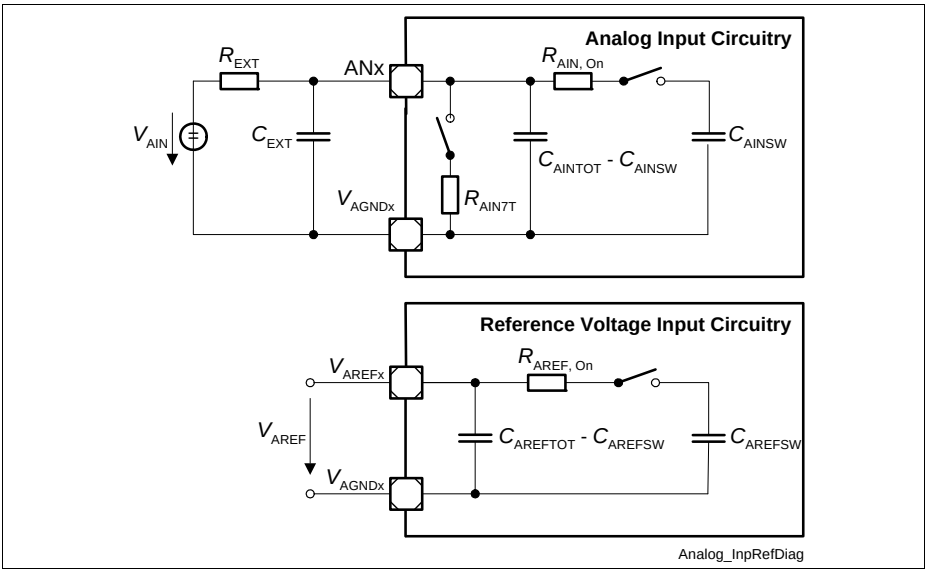

Figure 13 ADCx Input Circuits

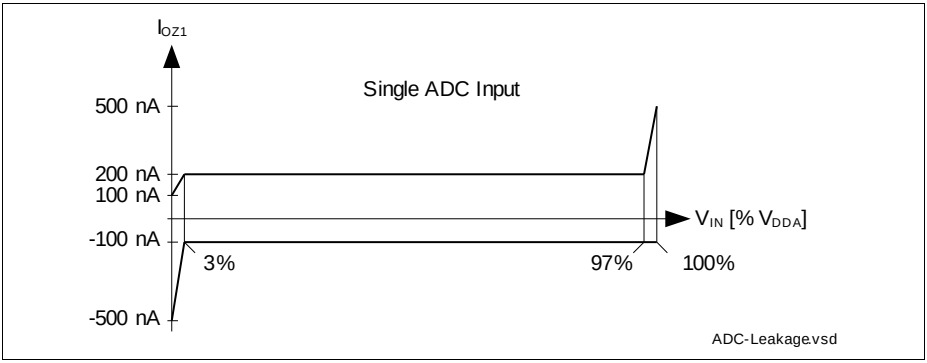

Figure 14 ADCx Analog Input Leakage Current

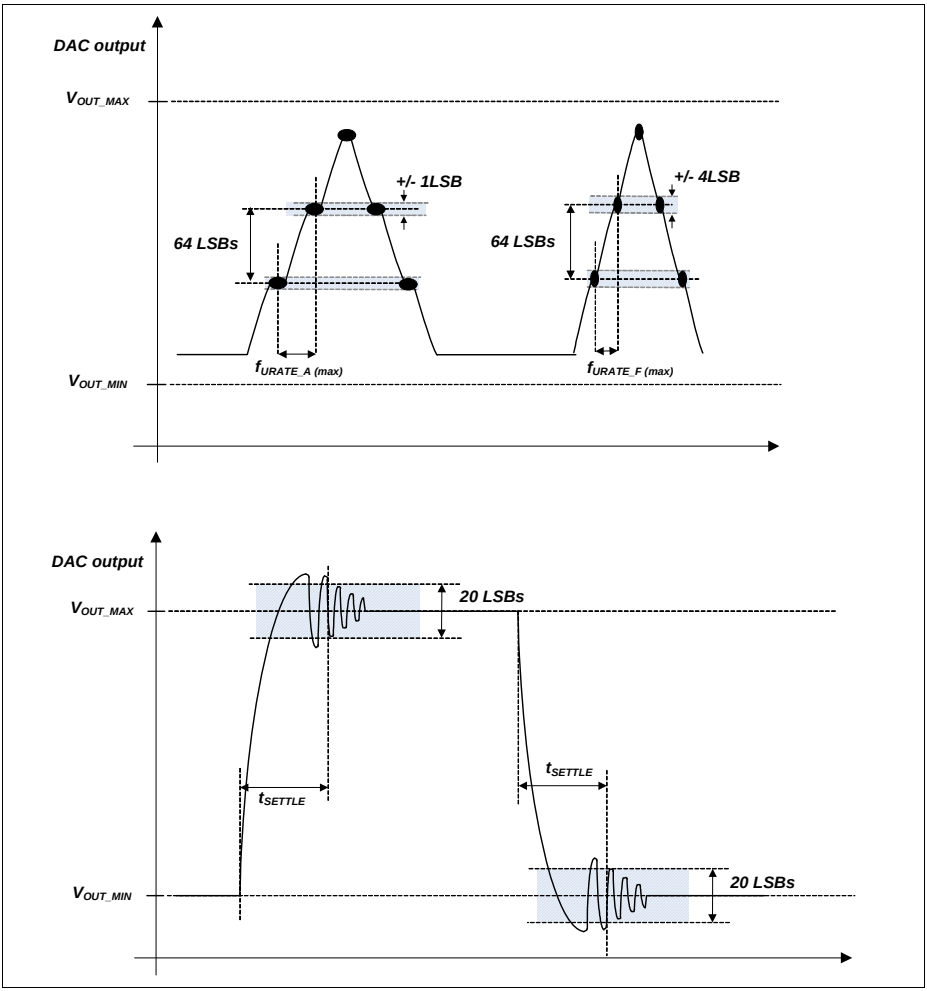

Figure 15 DAC Conversion Examples

3.2.5 High Resolution PWM (HRPWM)

The following chapters describe the operating conditions, characteristics and timing requirements, for all the components inside the HRPWM module. Each description is given for just one sub unit, e.g., one CSG or one HRC.

All the timing information is related to the module clock, f_{hrpwm}.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.2.5.1 HRC characteristics

Table 29 summarizes the characteristics of the HRC units.

Table 29 HRC characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
High resolution step size[1)2)]	t_{HRS} CC	–	150	–	ps	
Startup time (after reset release)	t_{start} CC	–	–	2	µs	

1) The step size for clock frequencies equal to 180, 120 and 80 MHz is 150 ps.

2) The step size for clock frequencies different from 180, 120 and 80 MHz but within the range from 180 to 64 MHz can be between 118 to 180 ps (fixed over process and operating conditions)

3.2.5.2 CMP and 10-bit DAC characteristics

The **Table 30** summarizes the characteristics of the CSG unit.

The specified characteristics require that the setup of the HRPWM follows the initialization sequence as documented in the Reference Manual.

Table 30 CMP and 10-bit DAC characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAC Resolution	*RES* CC		10		bits	
DAC differential nonlinearity	*DNL CC*	-1	–	1.5	LSB	Monotonic behavior, See **Figure 18**
DAC integral nonlinearity	*INL* CC	-3	–	3	LSB	See **Figure 18**

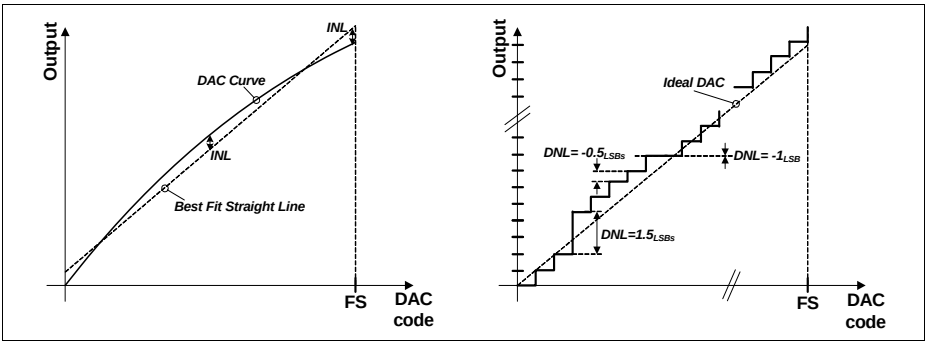

Figure 18 CSG DAC INL and DNL example

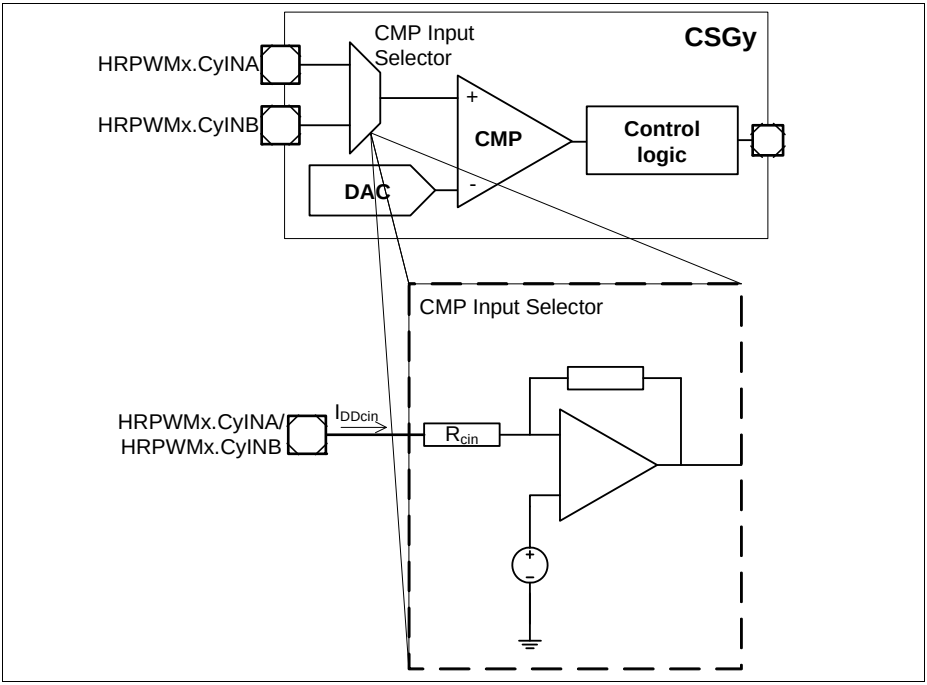

Figure 19 Input operation current

3.2.7 Die Temperature Sensor

The Die Temperature Sensor (DTS) measures the junction temperature T_J.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 34 Die Temperature Sensor Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Temperature sensor range	T_{SR}	SR	-40	–	150	°C	
Linearity Error (to the below defined formula)	ΔT_{LE}	CC	–	±1	–	°C	per $\Delta T_J \leq 30$ °C
Offset Error	ΔT_{OE}	CC	–	±6	–	°C	$\Delta T_{OE} = T_J - T_{DTS}$ $V_{DDP} \leq 3.3$ V[1]
Measurement time	t_M	CC	–	–	100	µs	
Start-up time after reset inactive	t_{TSST}	SR	–	–	10	µs	

1) At V_{DDP_max} = 3.63 V the typical offset error increases by an additional ΔT_{OE} = ±1 °C.

The following formula calculates the temperature measured by the DTS in [°C] from the RESULT bit field of the DTSSTAT register.

Temperature T_{DTS} = (RESULT - 605) / 2.05 [°C]

This formula and the values defined in **Table 34** apply with the following calibration values:

- DTSCON.BGTRIM = 8_H
- DTSCON.REFTRIM = 4_H

3.3.4 Phase Locked Loop (PLL) Characteristics

Main and USB PLL

Table 43 PLL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated Jitter	D_P CC	–	–	±5	ns	accumulated over 300 cycles f_{SYS} = 80 MHz
Duty Cycle[1)]	D_{DC} CC	46	50	54	%	Low pulse to total period, assuming an ideal input clock source
PLL base frequency	$f_{PLLBASE}$ CC	30	–	140	MHz	
VCO input frequency	f_{REF} CC	4	–	16	MHz	
VCO frequency range	f_{VCO} CC	260	–	520	MHz	
PLL lock-in time	t_L CC	–	–	400	µs	

1) 50% for even K2 divider values, 50±(10/K2) for odd K2 divider values.

3.3.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

Table 46 JTAG Interface Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TCK clock period	t_1	SR	30	–	–	ns	For C_L = 20 pF on TDO
TCK clock period	t_1	SR	40	–	–	ns	For C_L = 50 pF on TDO
TCK high time	t_2	SR	10	–	–	ns	
TCK low time	t_3	SR	10	–	–	ns	
TCK clock rise time	t_4	SR	–	–	4	ns	
TCK clock fall time	t_5	SR	–	–	4	ns	
TDI/TMS setup to TCK rising edge	t_6	SR	6	–	–	ns	
TDI/TMS hold after TCK rising edge	t_7	SR	6	–	–	ns	
TDO valid after TCK falling edge[1] (propagation delay)	t_8	CC	–	–	17	ns	C_L = 50 pF
			3	–	–	ns	C_L = 20 pF
TDO hold after TCK falling edge[1]	t_{18}	CC	2	–	–	ns	
TDO high imped. to valid from TCK falling edge[1)2)]	t_9	CC	–	–	14	ns	C_L = 50 pF
TDO valid to high imped. from TCK falling edge[1]	t_{10}	CC	–	–	13.5	ns	C_L = 50 pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

3.3.7 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

Table 47 SWD Interface Timing Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SWDCLK clock period	t_{SC}	SR	25	–	–	ns	C_L = 30 pF
			40	–	–	ns	C_L = 50 pF
SWDCLK high time	t_1	SR	10	–	500000	ns	
SWDCLK low time	t_2	SR	10	–	500000	ns	
SWDIO input setup to SWDCLK rising edge	t_3	SR	6	–	–	ns	
SWDIO input hold after SWDCLK rising edge	t_4	SR	6	–	–	ns	
SWDIO output valid time after SWDCLK rising edge	t_5	CC	–	–	17	ns	C_L = 50 pF
			–	–	13	ns	C_L = 30 pF
SWDIO output hold time from SWDCLK rising edge	t_6	CC	3	–	–	ns	

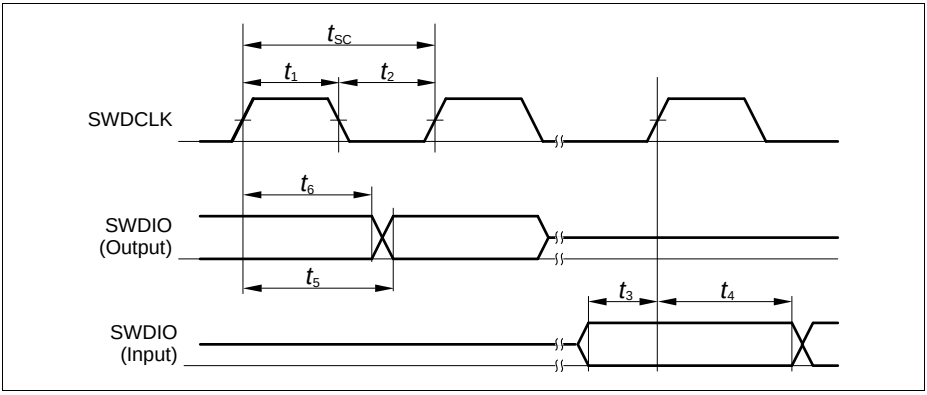

Figure 30 SWD Timing

4.2 Package Outlines

The availability of different packages for different devices types is listed in **Table 1**, specific packages for different device markings are listed in **Table 2**.

The exposed die pad dimensions are listed in **Table 55**.

Table 56 Differences PG-LQFP-64-19 to PG-TQFP-64-19

Change	PG-LQFP-64-19	PG-TQFP-64-19
Thermal Resistance Junction Ambient ($R_{\Theta JA}$)	30 K/W	23.4 K/W
Package thickness	$1.4^{\pm 0.05}$ mm	$1.0^{\pm 0.05}$ mm
	1.6 mm MAX	1.2 mm MAX
Exposed Die Pad size	5.8 mm × 5.8 mm	5.7 mm × 5.7 mm