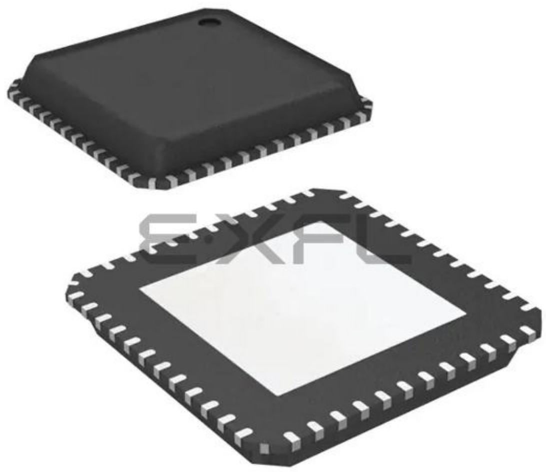
# Infineon Technologies - XMC4104Q48K128BAXUMA1 Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | CANbus, I²C, LINbus, SPI, UART/USART, USB |
| Peripherals | DMA, I²S, LED, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 20K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.13V ~ 3.63V |
| Data Converters | A/D 9x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-VFQFN Exposed Pad |
| Supplier Device Package | PG-VQFN-48-53 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xmc4104q48k128baxuma1 |

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**Table 6 SRAM Memory Ranges**

| Total SRAM Size | Program SRAM | System Data SRAM |
|---|---|---|
| 40 Kbytes | $1FFF\ C000_H$ – $1FFF\ FFFF_H$ | $2000\ 0000_H$ – $2000\ 5FFF_H$ |
| 20 Kbytes | $1FFF\ E000_H$ – $1FFF\ FFFF_H$ | $2000\ 0000_H$ – $2000\ 2FFF_H$ |

**Table 7 ADC Channels[1)]**

| Package | VADC G0 | VADC G1 |
|---|---|---|
| LQFP-64, TQFP-64 | CH0, CH3..CH7 | CH0, CH1, CH3, CH6 |
| PG-VQFN-48 | CH0, CH3..CH7 | CH0, CH1, CH3 |

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

## 1.6 Identification Registers

The identification registers allow software to identify the marking.

**Table 8 XMC4200 Identification Registers**

| Register Name | Value | Marking |
|---|---|---|
| SCU_IDCHIP | $0004\ 2001_H$ | EES-AA, ES-AA |
| SCU_IDCHIP | $0004\ 2002_H$ | ES-AB, AB |
| SCU_IDCHIP | $0004\ 2003_H$ | BA |
| JTAG IDCODE | $101D\ D083_H$ | EES-AA, ES-AA |
| JTAG IDCODE | $201D\ D083_H$ | ES-AB, AB |
| JTAG IDCODE | $301D\ D083_H$ | BA |

## 2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

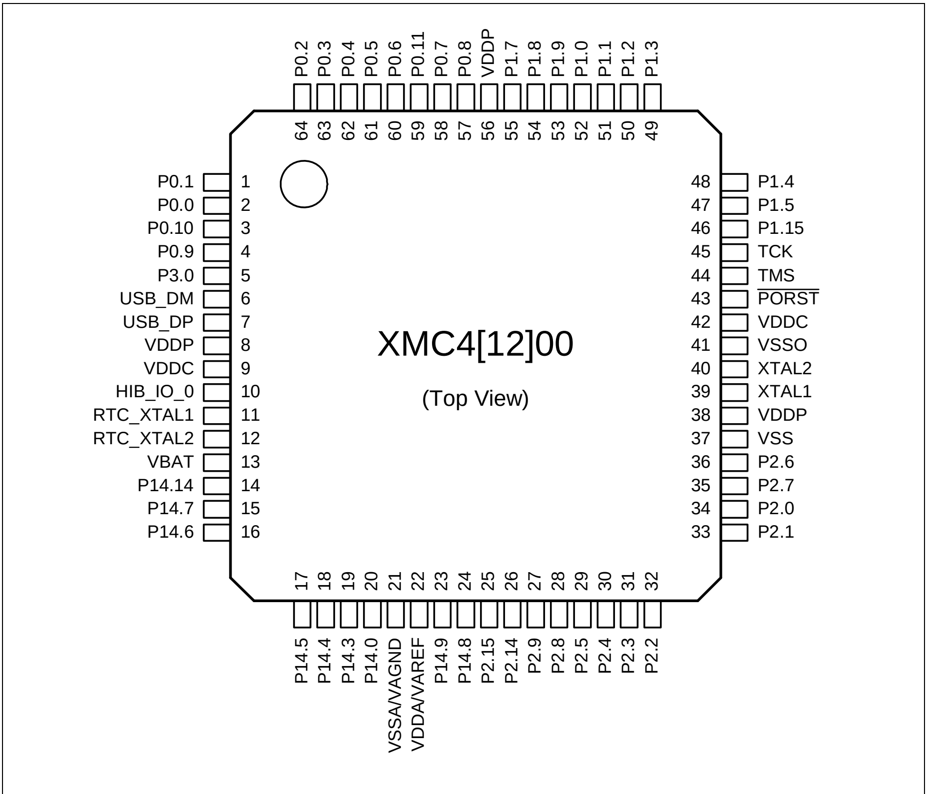


**Figure 4 XMC4[12]00 PG-LQFP-64 and PG-TQFP-64 Pin Configuration**
(top view)

**Table 11 Package Pin Mapping** (cont'd)

| Function | LQFP-64<br>TQFP-64 | VQFN-48 | Pad Type | Notes |
|---|---|---|---|---|
| P14.9 | 23 | 19 | AN/DAC/DIG_IN | |
| P14.14 | 14 | - | AN/DIG_IN | |
| USB_DP | 7 | 4 | special | |
| USB_DM | 6 | 3 | special | |
| HIB_IO_0 | 10 | 7 | A1 special | At the first power-up and with every reset of the hibernate domain this pin is configured as open-drain output and drives "0".<br>As output the medium driver mode is active. |
| TCK | 45 | 34 | A1 | Weak pull-down active. |
| TMS | 44 | 33 | A1+ | Weak pull-up active.<br>As output the strong-soft driver mode is active. |
| $\overline{\text{PORST}}$ | 43 | 32 | special | Strong pull-down controlled by EVR.<br>Weak pull-up active while strong pull-down is not active. |
| XTAL1 | 39 | 29 | clock_IN | |
| XTAL2 | 40 | 30 | clock_O | |
| RTC_XTAL1 | 11 | 8 | clock_IN | |
| RTC_XTAL2 | 12 | 9 | clock_O | |
| VBAT | 13 | 10 | Power | When VDDP is supplied VBAT has to be supplied as well. |
| VDDA/VAREF | 22 | 18 | AN_Power/AN_Ref | Shared analog supply and reference voltage pin. |
| VSSA/VAGND | 21 | 17 | AN_Power/AN_Ref | Shared analog supply and reference ground pin. |
| VDDC | 9 | 6 | Power | |
| VDDC | 42 | 31 | Power | |
| VDDP | 8 | 5 | Power | |
| VDDP | 38 | 28 | Power | |
| VDDP | 56 | 41 | Power | |
| VSS | 37 | 27 | Power | |

## 2.2.2 Port I/O Functions

The following general scheme is used to describe each PORT pin:

**Table 12 Port I/O Function Description**

| Function | Outputs | | | Inputs | | |
|---|---|---|---|---|---|---|
| | **ALT1** | **ALTn** | **HWO0** | **HWI0** | **Input** | **Input** |
| P0.0 | | MODA.OUT | MODB.OUT | MODB.INA | MODC.INA | |
| Pn.y | MODA.OUT | | | | MODA.INA | MODC.INB |

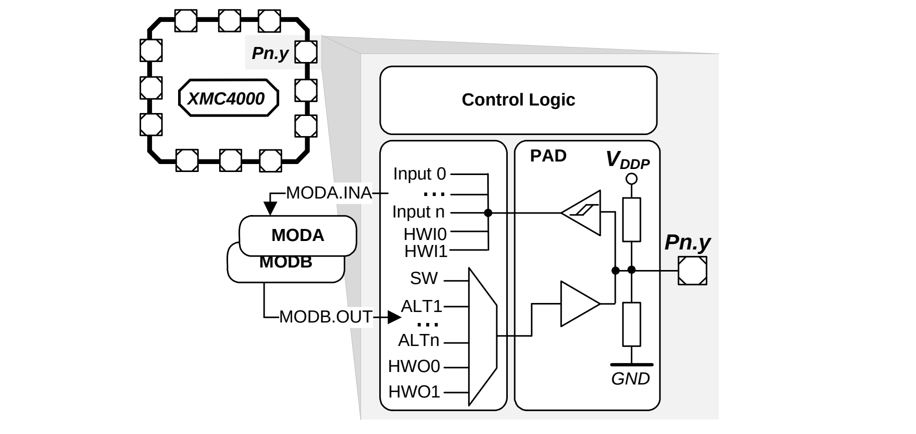


**Figure 6 Simplified Port Structure**

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to four alternate output functions (ALT1/2/3/4) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.
The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL it is possible to select between different hardware "masters" (HWO0/HWI0). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

#### 2.2.2.1 Port I/O Function Table

**Table 13 Port I/O Functions**

| Function | Output | | | | | Input | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | ALT1 | ALT2 | ALT3 | ALT4 | HWO0 | HWI0 | Input | Input | Input | Input | Input | Input | Input | Input |
| P0.0 | | CAN.N0_TXD | CCU80.OUT21 | LEDTS0.COL2 | | | U1C1.DX0D | | ERU0.0B0 | USB.VBUSDETECTA | | HRPWM0.C1INB | | |
| P0.1 | | U1C1.DOUT0 | CCU80.OUT11 | LEDTS0.COL3 | | | | | ERU0.0A0 | | | HRPWM0.C2INB | | |
| P0.2 | | U1C1.SELO1 | CCU80.OUT01 | HRPWM0.HROUT01 | U1C0.DOUT3 | U1C0.HWIN3 | | | ERU0.3B3 | | | | | |
| P0.3 | | | CCU80.OUT20 | HRPWM0.HROUT20 | U1C0.DOUT2 | U1C0.HWIN2 | | | | ERU1.3B0 | | | | |
| P0.4 | | | CCU80.OUT10 | HRPWM0.HROUT21 | U1C0.DOUT1 | U1C0.HWIN1 | | U1C0.DX0A | ERU0.2B3 | | | | | |
| P0.5 | | U1C0.DOUT0 | CCU80.OUT00 | HRPWM0.HROUT00 | U1C0.DOUT0 | U1C0.HWIN0 | | U1C0.DX0B | | ERU1.3A0 | | | | |
| P0.6 | | U1C0.SELO0 | CCU80.OUT30 | HRPWM0.HROUT30 | | | | U1C0.DX2A | ERU0.3B2 | | CCU80.IN2B | | | |
| P0.7 | WWDT.SERVICE_OUT | U0C0.SELO0 | | HRPWM0.HROUT11 | | DB.TDI | U0C0.DX2B | | ERU0.2B1 | | CCU80.IN0A | CCU80.IN1A | CCU80.IN2A | CCU80.IN3A |
| P0.8 | SCU.EXTCLK | U0C0.SCLKOUT | | HRPWM0.HROUT10 | | DB.$\overline{\text{TRST}}$ | U0C0.DX1B | | ERU0.2A1 | | CCU80.IN1B | | | |
| P0.9 | HRPWM0.HROUT31 | U1C1.SELO0 | CCU80.OUT12 | LEDTS0.COL0 | | | U1C1.DX2A | | ERU0.1B0 | | | | | |
| P0.10 | | U1C1.SCLKOUT | CCU80.OUT02 | LEDTS0.COL1 | | | U1C1.DX1A | | ERU0.1A0 | | | | | |
| P0.11 | | U1C0.SCLKOUT | CCU80.OUT31 | | | | | U1C0.DX1A | ERU0.3A2 | | | | | |
| P1.0 | | U0C0.SELO0 | CCU40.OUT3 | ERU1.PDOUT3 | | | U0C0.DX2A | | ERU0.3B0 | | CCU40.IN3A | HRPWM0.C0INA | | |
| P1.1 | | U0C0.SCLKOUT | CCU40.OUT2 | ERU1.PDOUT2 | | | U0C0.DX1A | POSIF0.IN2A | ERU0.3A0 | | CCU40.IN2A | HRPWM0.C1INA | | |
| P1.2 | | | CCU40.OUT1 | ERU1.PDOUT1 | U0C0.DOUT3 | U0C0.HWIN3 | | POSIF0.IN1A | | ERU1.2B0 | CCU40.IN1A | HRPWM0.C2INA | | |
| P1.3 | | U0C0.MCLKOUT | CCU40.OUT0 | ERU1.PDOUT0 | U0C0.DOUT2 | U0C0.HWIN2 | | POSIF0.IN0A | | ERU1.2A0 | CCU40.IN0A | HRPWM0.C0INB | | |
| P1.4 | WWDT.SERVICE_OUT | CAN.N0_TXD | CCU80.OUT33 | | U0C0.DOUT1 | U0C0.HWIN1 | U0C0.DX0B | CAN.N1_RXDD | ERU0.2B0 | | CCU41.IN0C | HRPWM0.BL0A | | |
| P1.5 | CAN.N1_TXD | U0C0.DOUT0 | CCU80.OUT23 | | U0C0.DOUT0 | U0C0.HWIN0 | U0C0.DX0A | CAN.N0_RXDA | ERU0.2A0 | ERU1.0A0 | CCU41.IN1C | | | |
| P1.7 | | U0C0.DOUT0 | | U1C1.SELO2 | | | | | | USB.VBUSDETECTB | | | | |

**Table 13 Port I/O Functions** (cont'd)

| Function | Output | | | | | Input | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | ALT1 | ALT2 | ALT3 | ALT4 | HWO0 | HWI0 | Input | Input | Input | Input | Input | Input | Input | Input |
| P14.9 | | | | | DAC.<br>OUT_1 | | | VADC.<br>G1CH1 | | | | | | |
| P14.14 | | | | | | | | VADC.<br>G1CH6 | | | | | G1ORC6 | |
| USB_DP | | | | | | | | | | | | | | |
| USB_DM | | | | | | | | | | | | | | |
| HIB_IO_0 | HIBOUT | WWDT.<br>SERVICE_OUT | | | | | WAKEUPA | | | USB.<br>VBUSDETECT<br>C | | | | |
| TCK | | | | | | DB.TCK/<br>SWCLK | | | | | | | | |
| TMS | | | | | DB.TMS/<br>SWDIO | | | | | | | | | |
| $\overline{\text{PORST}}$ | | | | | | | | | | | | | | |
| XTAL1 | | | | | | | U0C0.<br>DX0F | U0C1.<br>DX0F | U1C0.<br>DX0F | U1C1.<br>DX0F | | | | |
| XTAL2 | | | | | | | | | | | | | | |
| RTC_XTAL1 | | | | | | | | | ERU0.<br>1B1 | | | | | |
| RTC_XTAL2 | | | | | | | | | | | | | | |

The XMC4[12]00 has a common ground concept, all $V_{SS}$, $V_{SSA}$ and $V_{SSO}$ pins share the same ground potential. In packages with an exposed die pad it must be connected to the common ground as well.
There are no dedicated connections for the analog reference $V_{AREF}$ and $V_{AGND}$. Instead, they share the same pins as the analog supply pins $V_{DDA}$ and $V_{SSA}$.Some analog channels can optionally serve as “Alternate Reference”; further details on this operating mode are described in the Reference Manual.

When $V_{DDP}$ is supplied, $V_{BAT}$ must be supplied as well. If no other supply source (e.g. battery) is connected to $V_{BAT}$, the $V_{BAT}$ pin can also be connected directly to $V_{DDP}$.

### 3.1.5 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC4[12]00. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

**Table 20 Operating Conditions Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Ambient Temperature | $T_A$ SR | -40 | – | 85 | °C | Temp. Range F |
| | | -40 | – | 125 | °C | Temp. Range K |
| Digital supply voltage | $V_{DDP}$ SR | 3.13[1] | 3.3 | 3.63[2] | V | |
| Core Supply Voltage | $V_{DDC}$ CC | –[1] | 1.3 | – | V | Generated internally |
| Digital ground voltage | $V_{SS}$ SR | 0 | – | – | V | |
| ADC analog supply voltage | $V_{DDA}$ SR | 3.0 | 3.3 | 3.6[2] | V | |
| Analog ground voltage for $V_{DDA}$ | $V_{SSA}$ SR | -0.1 | 0 | 0.1 | V | |
| Battery Supply Voltage for Hibernate Domain[3] | $V_{BAT}$ SR | 1.95[4] | – | 3.63 | V | When $V_{DDP}$ is supplied $V_{BAT}$ has to be supplied as well. |
| System Frequency | $f_{SYS}$ SR | – | – | 80 | MHz | |
| Short circuit current of digital outputs | $I_{SC}$ SR | -5 | – | 5 | mA | |
| Absolute sum of short circuit currents per pin group[5] | $\Sigma I_{SC\_PG}$ SR | – | – | 20 | mA | |
| Absolute sum of short circuit currents of the device | $\Sigma I_{SC\_D}$ SR | – | – | 100 | mA | |

1) See also the Supply Monitoring thresholds, **Section 3.3.2**.
2) Voltage overshoot to 4.0 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h over lifetime.
3) Different limits apply for LPAC operation, **Section 3.2.6**
4) To start the hibernate domain it is required that $V_{BAT} \geq 2.1$ V, for a reliable start of the oscillation of RTC_XTAL in crystal mode it is required that $V_{BAT} \geq 3.0$ V.
5) The port groups are defined in **Table 18**.

**Table 24 HIB_IO Class_A1 special Pads**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | | Max. | | |
| Input leakage current | $I_{OZHIB}$ CC | -500 | | 500 | nA | $0\ V \leq V_{IN} \leq V_{BAT}$ |
| Input high voltage | $V_{IHHIB}$ SR | $0.6 \times V_{BAT}$ | | $V_{BAT} + 0.3$ | V | max. 3.6 V |
| Input low voltage | $V_{ILHIB}$ SR | -0.3 | | $0.36 \times V_{BAT}$ | V | |
| Input Hysteresis for HIB_IO pins[1)] | $HYSHIB$ CC | $0.1 \times V_{BAT}$ | | – | V | $V_{BAT} \geq 3.13\ V$ |
| | | $0.06 \times V_{BAT}$ | | – | V | $V_{BAT} < 3.13\ V$ |
| Output high voltage, POD[1)] = medium | $V_{OHHIB}$ CC | $V_{BAT}$ - 0.4 | | – | V | $I_{OH} \geq -1.4\ mA$ |
| Output low voltage | $V_{OLHIB}$ CC | – | | 0.4 | V | $I_{OL} \leq 2\ mA$ |
| Fall time | $t_{FHIB}$ CC | – | | 50 | ns | $V_{BAT} \geq 3.13\ V$ $C_L = 50\ pF$ |
| | | – | | 100 | ns | $V_{BAT} < 3.13\ V$ $C_L = 50\ pF$ |
| Rise time | $t_{RHIB}$ CC | – | | 50 | ns | $V_{BAT} \geq 3.13\ V$ $C_L = 50\ pF$ |
| | | – | | 100 | ns | $V_{BAT} < 3.13\ V$ $C_L = 50\ pF$ |

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

**Table 30 CMP and 10-bit DAC characteristics** (Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| CSG Output Jitter | $D_{CSG}$ CC | – | – | 1 | clk | |
| Bias startup time | $t_{start}$ CC | – | – | 98 | us | |
| Bias supply current | $I_{DDbias}$ CC | – | – | 400 | µA | |
| CSGy startup time | $t_{CSGS}$ CC | – | – | 2 | µs | |
| Input operation current[1)] | $I_{DDCIN}$ CC | -10 | – | 33 | µA | See **Figure 19** |
| High Speed Mode | | | | | | |
| DAC output voltage range | $V_{DOUT}$ CC | $V_{SS}$ | – | $V_{DDP}$ | V | |
| DAC propagation delay - Full scale | $t_{FShs}$ CC | – | – | 80 | ns | See **Figure 20** |
| Input Selector propagation delay - Full scale | $t_{Dhs}$ CC | – | – | 100 | ns | See **Figure 20** |
| Comparator bandwidth | $t_{Dhs}$ CC | 20 | – | – | ns | |
| DAC CLK frequency | $f_{clk}$ SR | – | – | 30 | MHz | |
| Supply current | $I_{DDhs}$ CC | – | – | 940 | µA | |
| Low Speed Mode | | | | | | |
| DAC output voltage range | $V_{DOUT}$ CC | $0.1 \times V_{DDP}$[2)] | – | $V_{DDP}$ | V | |
| DAC propagation delay - Full Scale | $t_{FSls}$ CC | – | – | 160 | ns | See **Figure 20** |
| Input Selector propagation delay - Full Scale | $t_{Dls}$ CC | – | – | 200 | ns | See **Figure 20** |
| Comparator bandwidth | $t_{Dls}$ CC | 20 | – | – | ns | |
| DAC CLK frequency | $f_{clk}$ SR | – | – | 30 | MHz | |
| Supply current | $I_{DDls}$ CC | – | – | 300 | µA | |

1) Typical input resistance $R_{CIN}$ = 100kOhm.

2) The INL error increases for DAC output voltages below this limit.

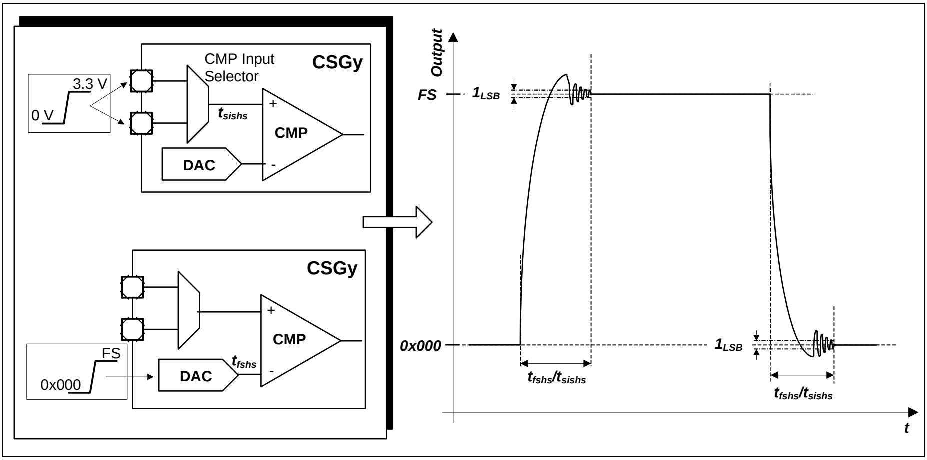


**Figure 20 DAC and Input Selector Propagation Delay**

### 3.2.5.3 Clocks

#### HRPWM DAC Conversion Clock

The DAC conversion clock can be generated internally or it can be controlled via a HRPWM module pin.

**Table 31 External DAC conversion trigger operating conditions**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Frequency | $f_{etrg}$ | SR | – | – | 30[2] | MHz | |
| ON time | $t_{onetrg}$ | SR | $2T_{ccu}$[1)2)] | – | – | ns | |
| OFF time | $t_{offetrg}$ | SR | $2T_{ccu}$[1)2)] | – | – | ns | |

1) 50% duty cycle is not obligatory

2) Only valid if the signal was not previously synchronized/generated with the fccu clock (or a synchronous clock)

#### CSG External Clock

It is possible to select an external source, that can be used as a clock for the slope generation, HRPWMx.ECLKy. This clock is synchronized internally with the module clock and therefore the external clock needs to meet the criterion described on **Table 32**.

**Table 38 Power Supply Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Power Dissipation | $P_{DISS}$ | CC | – | – | 1 | W | $V_{DDP}$ = 3.6 V, $T_J$ = 150 °C |
| Wake-up time from Sleep to Active mode | $t_{SSA}$ | CC | – | 6 | – | cycles | |
| Wake-up time from Deep Sleep to Active mode | | | – | – | – | ms | Defined by the wake-up of the Flash module, see **Section 3.2.11** |
| Wake-up time from Hibernate mode | | | – | – | – | ms | Wake-up via power-on reset event, see **Section 3.3.2** |

1) CPU executing code from Flash, all peripherals idle.
2) CPU executing code from Flash. USB and CCU clock off.
3) CPU in sleep, all peripherals idle, Flash in Active mode.
4) CPU in sleep, Flash in Active mode.
5) CPU in sleep, peripherals disabled, after wake-up code execution from RAM.
6) To wake-up the Flash from its Sleep mode, $f_{CPU} \geq 1$ MHz is required.
7) OSC_ULP operating with external crystal on RTC_XTAL
8) OSC_ULP off, Hibernate domain operating with OSC_SI clock
9) Test Power Loop: $f_{SYS}$ = 80 MHz, CPU executing benchmark code from Flash, all CCUs in 100kHz timer mode, all ADC groups in continuous conversion mode, USICs as SPI in internal loop-back mode, CAN in 500kHz internal loop-back mode, interrupt triggered DMA block transfers to parity protected RAMs and FCE, DTS measurements and FPU calculations.
The power consumption of each customer application will most probably be lower than this value, but must be evaluated separately.
10) $I_{DDP}$ decreases typically by 3.5 mA when $f_{SYS}$ decreases by 10 MHz, at constant $T_J$
11) Sum of currents of all active converters (ADC and DAC)

### 3.2.11 Flash Memory Parameters

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 40 Flash Memory Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Erase Time per 256 Kbyte Sector | $t_{ERP}$ CC | – | 5 | 5.5 | s | |
| Erase Time per 64 Kbyte Sector | $t_{ERP}$ CC | – | 1.2 | 1.4 | s | |
| Erase Time per 16 Kbyte Logical Sector | $t_{ERP}$ CC | – | 0.3 | 0.4 | s | |
| Program time per page[1] | $t_{PRP}$ CC | – | 5.5 | 11 | ms | |
| Erase suspend delay | $t_{FL\_ErSusp}$ CC | – | – | 15 | ms | |
| Wait time after margin change | $t_{FL\_MarginDel}$ CC | 10 | – | – | µs | |
| Wake-up time | $t_{WU}$ CC | – | – | 270 | µs | |
| Read access time | $t_a$ CC | 20 | – | – | ns | For operation with $1 / f_{CPU} < t_a$ wait states must be configured[2] |
| Data Retention Time, Physical Sector[3)4)] | $t_{RET}$ CC | 20 | – | – | years | Max. 1000 erase/program cycles |
| Data Retention Time, Logical Sector[3)4)] | $t_{RETL}$ CC | 20 | – | – | years | Max. 100 erase/program cycles |

## 3.3 AC Parameters

### 3.3.1 Testing Waveforms

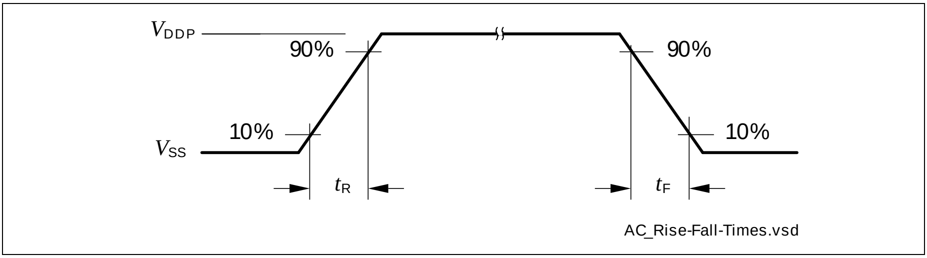


**Figure 23 Rise/Fall Time Parameters**

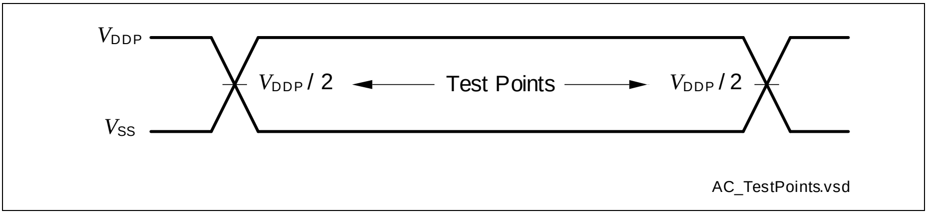


**Figure 24 Testing Waveform, Output Delay**

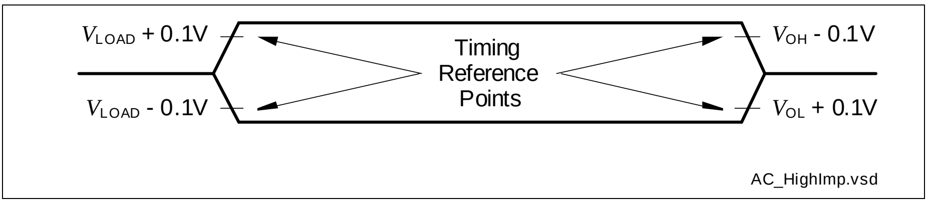


**Figure 25 Testing Waveform, Output High Impedance**

**Table 42 Power Sequencing Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Positive Load Step Current | $\Delta I_{PLS}$ SR | - | – | 50 | mA | Load increase on $V_{DDP}$ $\Delta t \leq 10$ ns |
| Negative Load Step Current | $\Delta I_{NLS}$ SR | - | – | 150 | mA | Load decrease on $V_{DDP}$ $\Delta t \leq 10$ ns |
| $V_{DDC}$ Voltage Over- / Undershoot from Load Step | $\Delta V_{LS}$ CC | - | – | ±100 | mV | For maximum positive or negative load step |
| Positive Load Step Settling Time | $t_{PLSS}$ SR | 50 | – | - | µs | |
| Negative Load Step Settling Time | $t_{NLSS}$ SR | 100 | – | - | µs | |
| External Buffer Capacitor on $V_{DDC}$ | $C_{EXT}$ SR | 3 | 4.7 | 6 | µF | In addition $C$ = 100 nF capacitor on each $V_{DDC}$ pin |

### Positive Load Step Examples

System assumptions:
$f_{CPU} = f_{SYS}$, target frequency $f_{CPU}$ = 80 MHz, main PLL $f_{VCO}$ = 480 MHz, stepping done by K2 divider, $t_{PLSS}$ between individual steps:

24 MHz - 48 MHz - 80 MHz (K2 steps 20 - 10 - 6)
24 MHz - 60 MHz - 80 MHz (K2 steps 20 - 8 - 6)

### 3.3.4 Phase Locked Loop (PLL) Characteristics

#### Main and USB PLL

**Table 43 PLL Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Accumulated Jitter | $D_P$ CC | – | – | ±5 | ns | accumulated over 300 cycles $f_{SYS}$ = 80 MHz |
| Duty Cycle[1)] | $D_{DC}$ CC | 46 | 50 | 54 | % | Low pulse to total period, assuming an ideal input clock source |
| PLL base frequency | $f_{PLLBASE}$ CC | 30 | – | 140 | MHz | |
| VCO input frequency | $f_{REF}$ CC | 4 | – | 16 | MHz | |
| VCO frequency range | $f_{VCO}$ CC | 260 | – | 520 | MHz | |
| PLL lock-in time | $t_L$ CC | – | – | 400 | µs | |

1) 50% for even K2 divider values, 50±(10/K2) for odd K2 divider values.

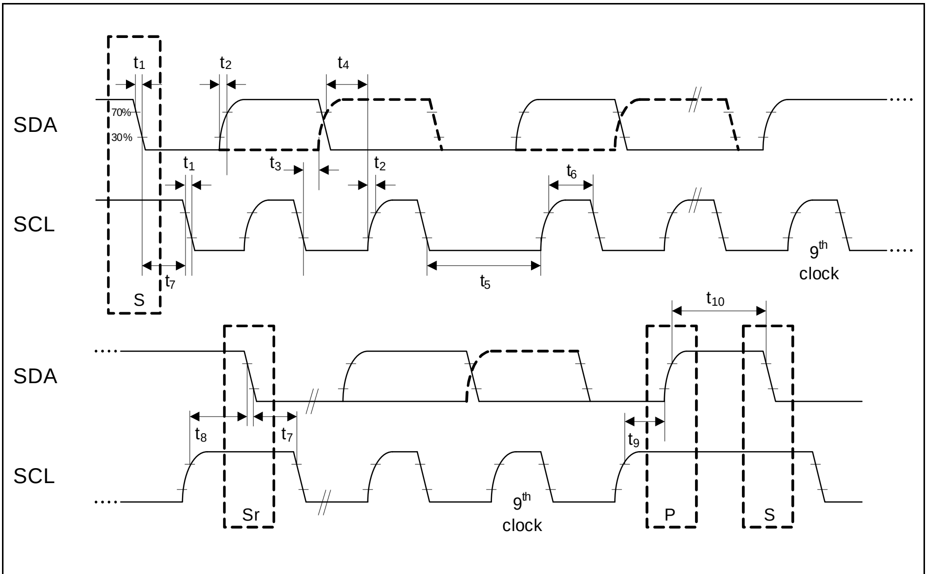


**Figure 32 USIC IIC Stand and Fast Mode Timing**

### 3.3.8.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

*Note: Operating Conditions apply.*

**Table 52 USIC IIS Master Transmitter Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Clock period | $t_1$ CC | 33.3 | – | – | ns | |
| Clock high time | $t_2$ CC | 0.35 x $t_{1min}$ | – | – | ns | |
| Clock low time | $t_3$ CC | 0.35 x $t_{1min}$ | – | – | ns | |
| Hold time | $t_4$ CC | 0 | – | – | ns | |
| Clock rise time | $t_5$ CC | – | – | 0.15 x $t_{1min}$ | ns | |

power dissipation must be limited so that the average junction temperature does not exceed 150 °C.

The difference between junction temperature and ambient temperature is determined by
$\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers ($P_{IODYN}$) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce $V_{DDP}$, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers