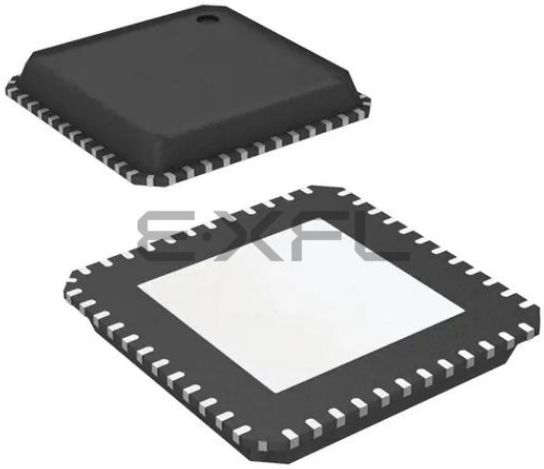
Infineon Technologies - XMC4104Q48K64ABXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 9x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-53
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4104q48k64abxuma1

Table of Contents

1 Summary of Features . . . 9
1.1 Ordering Information . . . 11
1.2 Device Types . . . 11
1.3 Package Variants . . . 12
1.4 Device Type Features . . . 12
1.5 Definition of Feature Variants . . . 13
1.6 Identification Registers . . . 14

2 General Device Information . . . 16
2.1 Logic Symbols . . . 16
2.2 Pin Configuration and Definition . . . 18
2.2.1 Package Pin Summary . . . 20
2.2.2 Port I/O Functions . . . 24
2.2.2.1 Port I/O Function Table . . . 25
2.3 Power Connection Scheme . . . 28

3 Electrical Parameters . . . 30
3.1 General Parameters . . . 30
3.1.1 Parameter Interpretation . . . 30
3.1.2 Absolute Maximum Ratings . . . 31
3.1.3 Pin Reliability in Overload . . . 33
3.1.4 Pad Driver and Pad Classes Summary . . . 35
3.1.5 Operating Conditions . . . 36
3.2 DC Parameters . . . 37
3.2.1 Input/Output Pins . . . 37
3.2.2 Analog to Digital Converters (ADCx) . . . 42
3.2.3 Digital to Analog Converters (DACx) . . . 47
3.2.4 Out-of-Range Comparator (ORC) . . . 50
3.2.5 High Resolution PWM (HRPWM) . . . 52
3.2.5.1 HRC characteristics . . . 52
3.2.5.2 CMP and 10-bit DAC characteristics . . . 52
3.2.5.3 Clocks . . . 55
3.2.6 Low Power Analog Comparator (LPAC) . . . 56
3.2.7 Die Temperature Sensor . . . 57
3.2.8 USB Device Interface DC Characteristics . . . 58
3.2.9 Oscillator Pins . . . 59
3.2.10 Power Supply Current . . . 63
3.2.11 Flash Memory Parameters . . . 67
3.3 AC Parameters . . . 69
3.3.1 Testing Waveforms . . . 69
3.3.2 Power-Up and Supply Monitoring . . . 70
3.3.3 Power Sequencing . . . 71

1 Summary of Features

The XMC4[12]00 devices are members of the XMC4000 Family of microcontrollers based on the ARM Cortex-M4 processor core. The XMC4000 is a family of high performance and energy efficient microcontrollers optimized for Industrial Connectivity, Industrial Control, Power Conversion, Sense & Control.

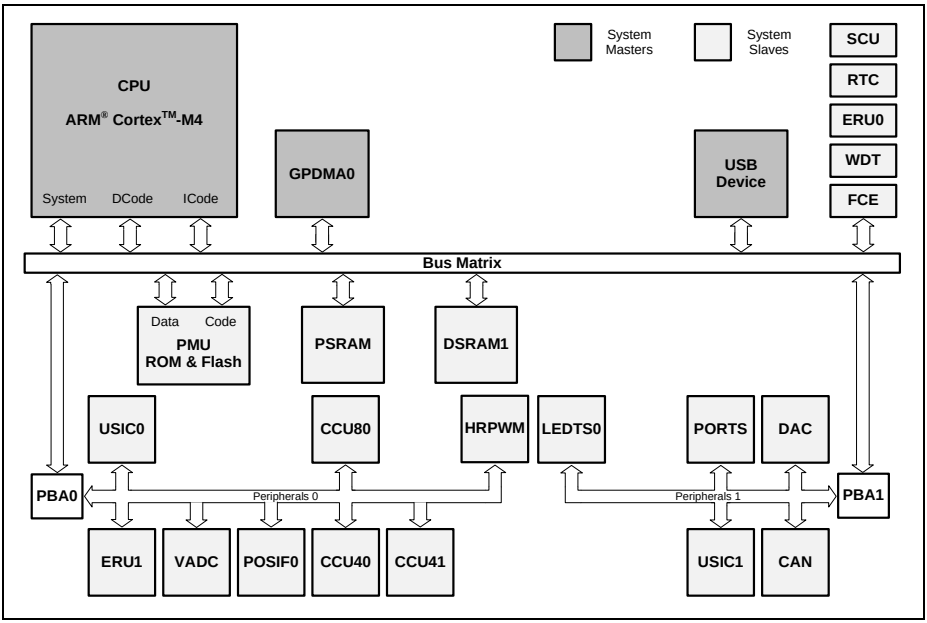

Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
  - High Performance 32-bit ARM Cortex-M4 CPU
  - 16-bit and 32-bit Thumb2 instruction set
  - DSP/MAC instructions
  - System timer (SysTick) for Operating System support
- Floating Point Unit
- Memory Protection Unit
- Nested Vectored Interrupt Controller
- One General Purpose DMA with up-to 8 channels
- Event Request Unit (ERU) for programmable processing of external and internal service requests
- Flexible CRC Engine (FCE) for multiple bit error detection

Table 6 SRAM Memory Ranges

Total SRAM Size	Program SRAM	System Data SRAM
40 Kbytes	1FFF C000$_H$ – 1FFF FFFF$_H$	2000 0000$_H$ – 2000 5FFF$_H$
20 Kbytes	1FFF E000$_H$ – 1FFF FFFF$_H$	2000 0000$_H$ – 2000 2FFF$_H$

Table 7 ADC Channels[1)]

Package	VADC G0	VADC G1
LQFP-64, TQFP-64	CH0, CH3..CH7	CH0, CH1, CH3, CH6
PG-VQFN-48	CH0, CH3..CH7	CH0, CH1, CH3

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

1.6 Identification Registers

The identification registers allow software to identify the marking.

Table 8 XMC4200 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	0004 2001$_H$	EES-AA, ES-AA
SCU_IDCHIP	0004 2002$_H$	ES-AB, AB
SCU_IDCHIP	0004 2003$_H$	BA
JTAG IDCODE	101D D083$_H$	EES-AA, ES-AA
JTAG IDCODE	201D D083$_H$	ES-AB, AB
JTAG IDCODE	301D D083$_H$	BA

Table 9 XMC4100 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	0004 2001$_H$	EES-AA, ES-AA
SCU_IDCHIP	0004 2002$_H$	ES-AB, AB
SCU_IDCHIP	0004 1003$_H$	BA
JTAG IDCODE	101D D083$_H$	EES-AA, ES-AA
JTAG IDCODE	201D D083$_H$	ES-AB, AB
JTAG IDCODE	301D D083$_H$	BA

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

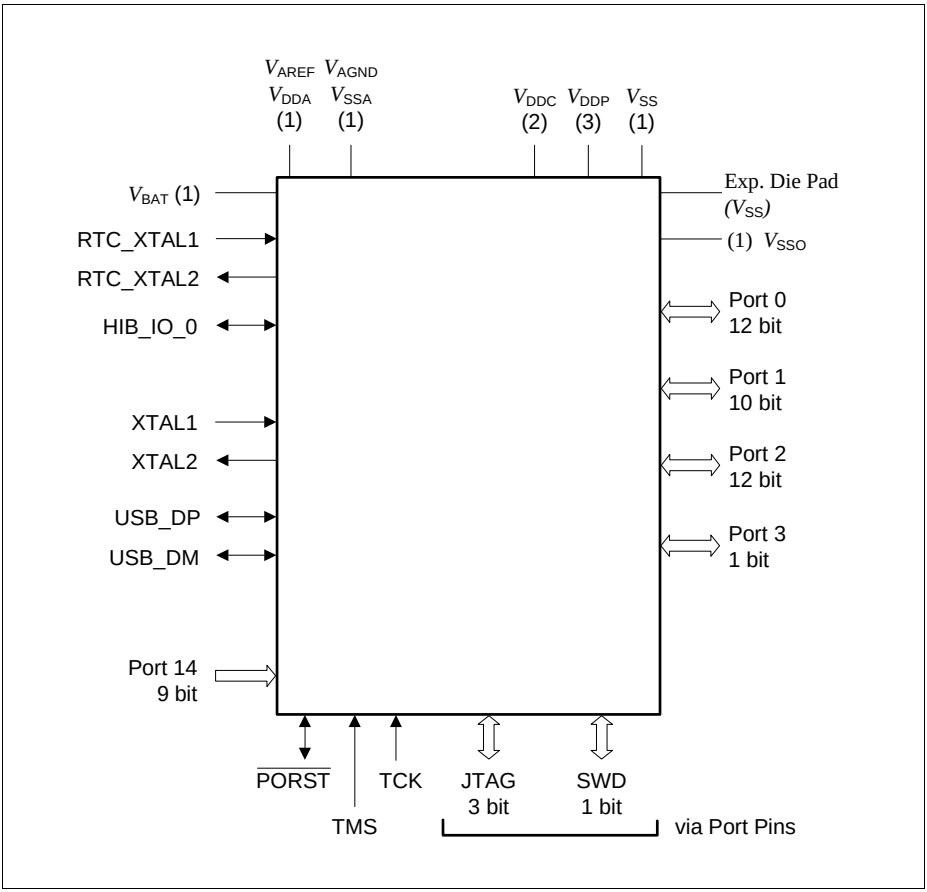

Figure 2 XMC4[12]00 Logic Symbol PG-LQFP-64 and PG-TQFP-64

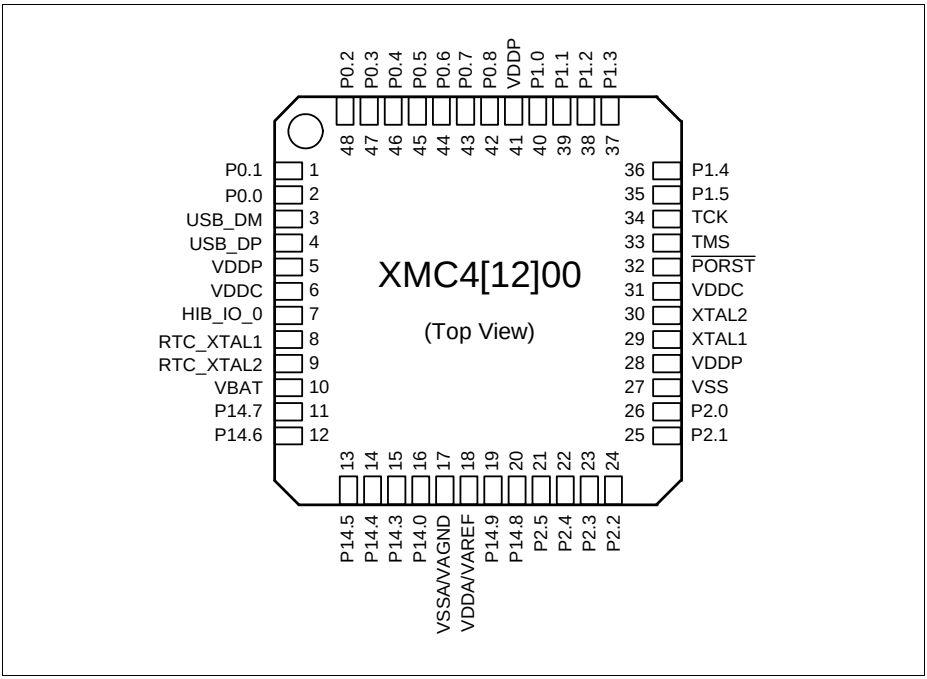

Figure 5 XMC4[12]00 PG-VQFN-48 Pin Configuration (top view)

Table 13 Port I/O Functions (cont'd)

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO0	HWI0	Input	Input	Input	Input	Input	Input	Input	Input
P14.9					DAC. OUT_1			VADC. G1CH1						
P14.14								VADC. G1CH6					G1ORC6	
USB_DP														
USB_DM														
HIB_IO_0	HIBOUT	WWDT. SERVICE_OUT					WAKEUPA			USB. VBUSDETECT C				
TCK						DB.TCK/ SWCLK								
TMS					DB.TMS/ SWDIO									
$\overline{\text{PORST}}$														
XTAL1							U0C0. DX0F	U0C1. DX0F	U1C0. DX0F	U1C1. DX0F				
XTAL2														
RTC_XTAL1									ERU0. 1B1					
RTC_XTAL2														

3.1.4 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in the **Section 3.2.1**.

Table 19 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub-Class	Speed Grade	Load	Termination
A	3.3 V	LVTTL I/O, LVTTL outputs	**A1** (e.g. GPIO)	6 MHz	100 pF	No
			A1+ (e.g. serial I/Os)	25 MHz	50 pF	Series termination recommended

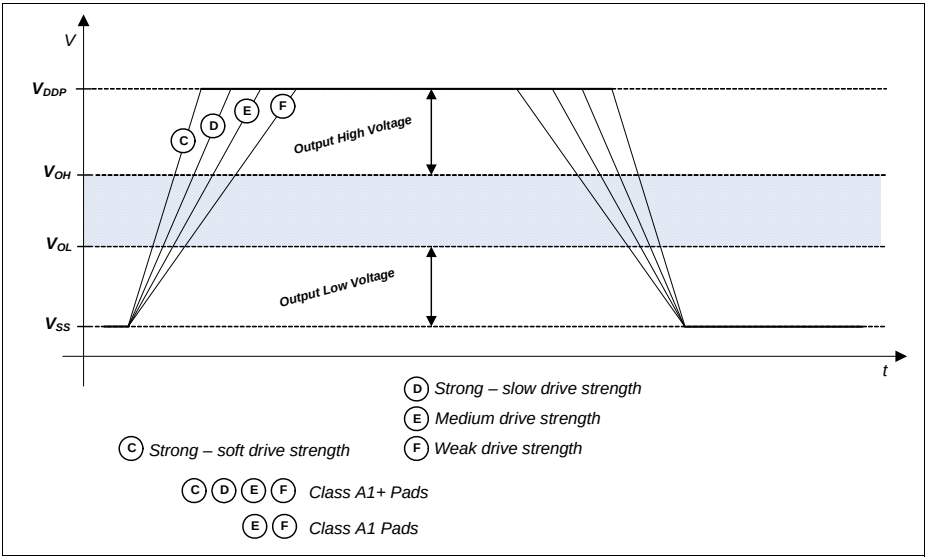

Figure 10 Output Slopes with different Pad Driver Modes

Figure 10 is a qualitative display of the resulting output slope performance with different output driver modes. The detailed input and output characteristics are listed in **Section 3.2.1**.

3.1.5 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC4[12]00. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 20 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A SR	-40	–	85	°C	Temp. Range F
		-40	–	125	°C	Temp. Range K
Digital supply voltage	V_{DDP} SR	3.13[1]	3.3	3.63[2]	V	
Core Supply Voltage	V_{DDC} CC	–[1]	1.3	–	V	Generated internally
Digital ground voltage	V_{SS} SR	0	–	–	V	
ADC analog supply voltage	V_{DDA} SR	3.0	3.3	3.6[2]	V	
Analog ground voltage for V_{DDA}	V_{SSA} SR	-0.1	0	0.1	V	
Battery Supply Voltage for Hibernate Domain[3]	V_{BAT} SR	1.95[4]	–	3.63	V	When V_{DDP} is supplied V_{BAT} has to be supplied as well.
System Frequency	f_{SYS} SR	–	–	80	MHz	
Short circuit current of digital outputs	I_{SC} SR	-5	–	5	mA	
Absolute sum of short circuit currents per pin group[5]	ΣI_{SC_PG} SR	–	–	20	mA	
Absolute sum of short circuit currents of the device	ΣI_{SC_D} SR	–	–	100	mA	

1) See also the Supply Monitoring thresholds, **Section 3.3.2**.

2) Voltage overshoot to 4.0 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h over lifetime.

3) Different limits apply for LPAC operation, **Section 3.2.6**

4) To start the hibernate domain it is required that $V_{BAT} \geq 2.1$ V, for a reliable start of the oscillation of RTC_XTAL in crystal mode it is required that $V_{BAT} \geq 3.0$ V.

5) The port groups are defined in **Table 18**.

3.2 DC Parameters

3.2.1 Input/Output Pins

The digital input stage of the shared analog/digital input pins is identical to the input stage of the standard digital input/output pins.
The pull-up characteristics (I_{PUH}) and the input high and low voltage levels (V_{IH} and V_{IL}) of the $\overline{\text{PORST}}$ pin are identical to the respective values of the standard digital input/output pins.

Table 21 Standard Pad Parameters

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Pin capacitance (digital inputs/outputs)	C_{IO} CC	–	10	pF	
Pull-down current	$\lvert I_{PDL}\rvert$ SR	150	–	µA	1) $V_{IN} \geq 0.6 \times V_{DDP}$
		–	10	µA	2) $V_{IN} \leq 0.36 \times V_{DDP}$
Pull-up current	$\lvert I_{PUH}\rvert$ SR	–	10	µA	2) $V_{IN} \geq 0.6 \times V_{DDP}$
		100	–	µA	1) $V_{IN} \leq 0.36 \times V_{DDP}$
Input Hysteresis for pads of all A classes[3]	$HYSA$ CC	$0.1 \times V_{DDP}$	–	V	
$\overline{\text{PORST}}$ spike filter always blocked pulse duration	t_{SF1} CC	–	10	ns	
$\overline{\text{PORST}}$ spike filter pass-through pulse duration	t_{SF2} CC	100	–	ns	
$\overline{\text{PORST}}$ pull-down current	$\lvert I_{PPD}\rvert$ CC	13	–	mA	$V_i = 1.0$ V

1) Current required to override the pull device with the opposite logic level (“force current”).
With active pull device, at load currents between force and keep current the input state is undefined.

2) Load current at which the pull device still maintains the valid logic level (“keep current”).
With active pull device, at load currents between force and keep current the input state is undefined.

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

Table 24 HIB_IO Class_A1 special Pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Input leakage current	I_{OZHIB} CC	-500		500	nA	$0\ V \le V_{IN} \le V_{BAT}$
Input high voltage	V_{IHHIB} SR	$0.6 \times V_{BAT}$		V_{BAT} + 0.3	V	max. 3.6 V
Input low voltage	V_{ILHIB} SR	-0.3		$0.36 \times V_{BAT}$	V	
Input Hysteresis for HIB_IO pins[1]	$HYSHIB$ CC	$0.1 \times V_{BAT}$		–	V	$V_{BAT} \ge 3.13$ V
		$0.06 \times V_{BAT}$		–	V	$V_{BAT} < 3.13$ V
Output high voltage, POD[1] = medium	V_{OHHIB} CC	V_{BAT} - 0.4		–	V	$I_{OH} \ge$ -1.4 mA
Output low voltage	V_{OLHIB} CC	–		0.4	V	$I_{OL} \le 2$ mA
Fall time	t_{FHIB} CC	–		50	ns	$V_{BAT} \ge 3.13$ V, $C_L = 50$ pF
		–		100	ns	$V_{BAT} < 3.13$ V, $C_L = 50$ pF
Rise time	t_{RHIB} CC	–		50	ns	$V_{BAT} \ge 3.13$ V, $C_L = 50$ pF
		–		100	ns	$V_{BAT} < 3.13$ V, $C_L = 50$ pF

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

3.2.2 Analog to Digital Converters (ADCx)

Table 25 ADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog reference voltage	V_{AREF} SR	–	–	–	V	$V_{AREF} = V_{DDA}$ shared analog supply and reference input pin
Alternate reference voltage[5]	V_{AREF} SR	V_{AGND} + 1	–	V_{DDA} + 0.05[1]	V	
Analog reference ground	V_{AGND} SR	–	–	–	V	$V_{AGND} = V_{SSA}$ shared analog supply and reference input pin
Alternate reference voltage range[2][5]	V_{AREF} - V_{AGND} SR	1	–	V_{DDA} + 0.1	V	
Analog input voltage	V_{AIN} SR	V_{AGND}	–	V_{DDA}	V	
Input leakage at analog inputs[3]	I_{OZ1} CC	-100	–	200	nA	$0.03 \times V_{DDA} < V_{AIN} < 0.97 \times V_{DDA}$
		-500	–	100	nA	$0\ V \le V_{AIN} \le 0.03 \times V_{DDA}$
		-100	–	500	nA	$0.97 \times V_{DDA} \le V_{AIN} \le V_{DDA}$
Internal ADC clock	f_{ADCI} CC	2	–	30	MHz	V_{DDA} = 3.3 V
Switched capacitance at the analog voltage inputs[4]	C_{AINSW} CC	–	4	6.5	pF	
Total capacitance of an analog input	C_{AINTOT} CC	–	12	20	pF	
Switched capacitance at the alternate reference voltage input[5][6]	C_{AREFSW} CC	–	15	30	pF	

Table 27 DAC Parameters (Operating Conditions apply) (cont'd)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Offset error	ED_{OFF}	CC		±20		mV	
Gain error	ED_{G_IN}	CC	-5	0	5	%	
Startup time	$t_{STARTUP}$	CC	–	15	30	µs	time from output enabling till code valid ±16 LSB
3dB Bandwidth of Output Buffer	f_{C1}	CC	2.5	5	–	MHz	verified by design
Output sourcing current	I_{OUT_SOURCE}	CC	–	-30	–	mA	
Output sinking current	I_{OUT_SINK}	CC	–	0.6	–	mA	
Output resistance	R_{OUT}	CC	–	50	–	Ohm	
Load resistance	R_L	SR	5	–	–	kOhm	
Load capacitance	C_L	SR	–	–	50	pF	
Signal-to-Noise Ratio	*SNR*	CC	–	70	–	dB	examination bandwidth < 25 kHz
Total Harmonic Distortion	*THD*	CC	–	70	–	dB	examination bandwidth < 25 kHz
Power Supply Rejection Ratio	*PSRR*	CC	–	56	–	dB	to V_{DDA} verified by design

1) According to best straight line method.

Conversion Calculation

Unsigned:
DACxDATA = 4095 × (V_{OUT} - V_{OUT_MIN}) / (V_{OUT_MAX} - V_{OUT_MIN})
Signed:
DACxDATA = 4095 × (V_{OUT} - V_{OUT_MIN}) / (V_{OUT_MAX} - V_{OUT_MIN}) - 2048

3.2.8 USB Device Interface DC Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification. High-Speed Mode is not supported.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 35 USB Device Data Line (USB_DP, USB_DM) Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Input low voltage	V_{IL}	SR	–	–	0.8	V	
Input high voltage (driven)	V_{IH}	SR	2.0	–	–	V	
Input high voltage (floating) [1]	V_{IHZ}	SR	2.7	–	3.6	V	
Differential input sensitivity	V_{DIS}	CC	0.2	–	–	V	
Differential common mode range	V_{CM}	CC	0.8	–	2.5	V	
Output low voltage	V_{OL}	CC	0.0	–	0.3	V	1.5 kOhm pull-up to 3.6 V
Output high voltage	V_{OH}	CC	2.8	–	3.6	V	15 kOhm pull-down to 0 V
DP pull-up resistor (idle bus)	R_{PUI}	CC	900	–	1 575	Ohm	
DP pull-up resistor (upstream port receiving)	R_{PUA}	CC	1 425	–	3 090	Ohm	
Input impedance DP, DM	Z_{INP}	CC	300	–	–	kOhm	$0\ V \le V_{IN} \le V_{DDP}$
Driver output resistance DP, DM	Z_{DRV}	CC	28	–	44	Ohm	

1) Measured at A-connector with 1.5 kOhm ± 5% to 3.3 V ± 0.3 V connected to USB_DP or USB_DM and at B-connector with 15 kOhm ± 5% to ground connected to USB_DP and USB_DM.

Table 36 OSC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	4	–	40	MHz	Direct Input Mode selected
		4	–	25	MHz	External Crystal Mode selected
Oscillator start-up time[1)2)]	t_{OSCS} CC	–	–	10	ms	
Input voltage at XTAL1	V_{IX} SR	-0.5	–	V_{DDP} + 0.5	V	
Input amplitude (peak-to-peak) at XTAL1[2)3)]	V_{PPX} SR	0.4 × V_{DDP}	–	V_{DDP} + 1.0	V	
Input high voltage at XTAL1[4)]	V_{IHBX}SR	1.0	–	V_{DDP} + 0.5	V	
Input low voltage at XTAL1[4)]	V_{ILBX} SR	-0.5	–	0.4	V	
Input leakage current at XTAL1	I_{ILX1} CC	-100	–	100	nA	Oscillator power down 0 V ≤ V_{IX} ≤ V_{DDP}

1) t_{OSCS} is defined from the moment the oscillator is enabled wih SCU_OSCHPCTRL.MODE until the oscillations reach an amplitude at XTAL1 of 0.4 * V_{DDP}.

2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.

3) If the shaper unit is enabled and not bypassed.

4) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.

Slow Internal Clock Source

Table 45 Slow Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal frequency	f_{OSI} CC	–	32.768	–	kHz	
Accuracy	Δf_{OSI} CC	-4	–	4	%	V_{BAT} = const. 0 °C ≤ T_A ≤ 85 °C
		-5	–	5	%	V_{BAT} = const. T_A < 0 °C or T_A > 85 °C
		-5	–	5	%	2.4 V ≤ V_{BAT}, T_A = 25 °C
		-10	–	10	%	1.95 V ≤ V_{BAT} < 2.4 V, T_A = 25 °C
Start-up time	t_{OSIS} CC	–	50	–	µs	

3.3.8 Peripheral Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

3.3.8.1 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: Operating Conditions apply.

Table 48 USIC SSC Master Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SCLKOUT master clock period	t_{CLK}	CC	40	–	–	ns	
Slave select output SELO active to first SCLKOUT transmit edge	t_1	CC	t_{SYS} - 6.5[1]	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2	CC	t_{SYS} - 8.5[1]	–	–	ns	
Data output DOUT[3:0] valid time	t_3	CC	-6	–	8	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4	SR	23	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5	SR	1	–	–	ns	

1) $t_{SYS} = 1 / f_{PB}$

3.3.8.2 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: Operating Conditions apply.

Table 50 USIC IIC Standard Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

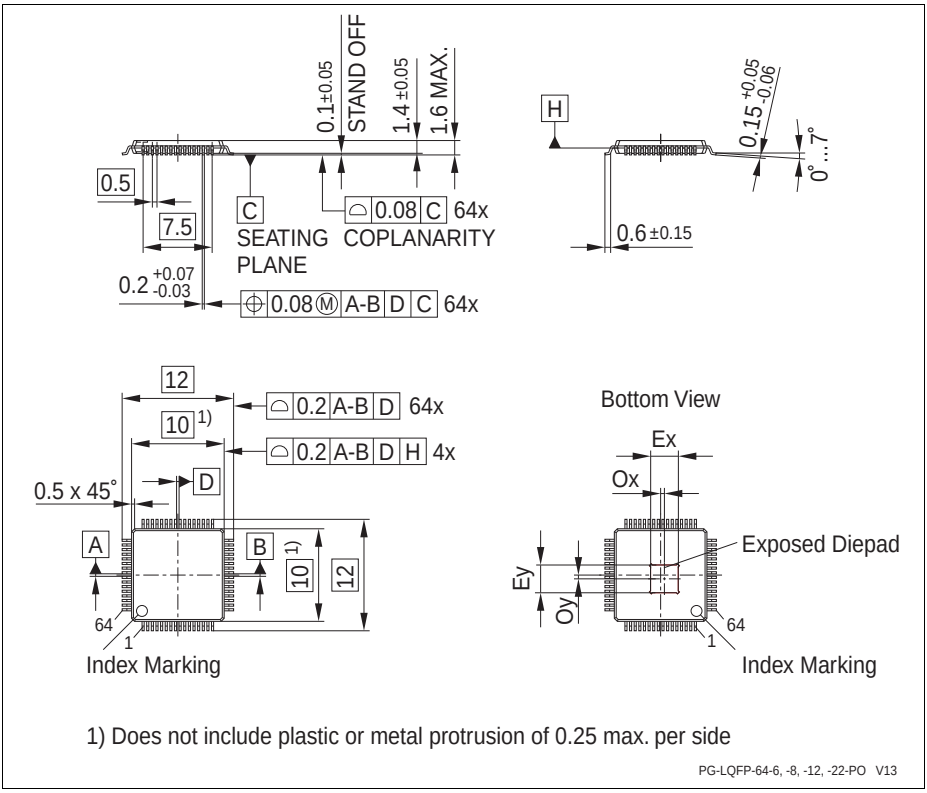

Figure 36 **PG-LQFP-64-19** (Plastic Green Low Profile Quad Flat Package)

5 Quality Declarations

The qualification of the XMC4[12]00 is executed according to the JEDEC standard JESD47H.

Note: For automotive applications refer to the Infineon automotive microcontrollers.

Table 58 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation lifetime	t_{OP} CC	20	–	–	a	$T_J \leq 109°C$, device permanent on
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	–	2 000	V	EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} SR	–	–	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	–	–	3	–	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	–	–	260	°C	Profile according to JEDEC J-STD-020D