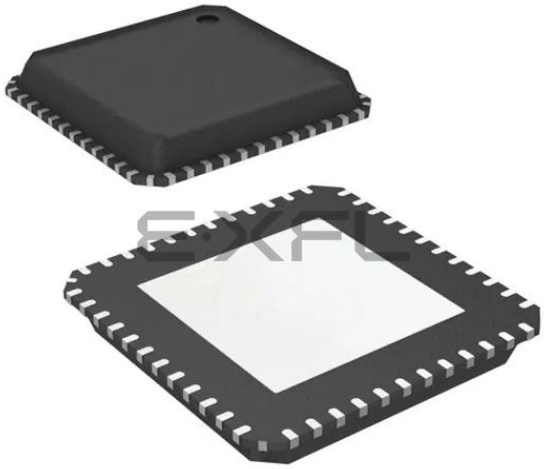
Infineon Technologies - XMC4104Q48K64BAXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 9x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-53
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4104q48k64baxuma1

Edition 2015-10

Published by
Infineon Technologies AG
81726 Munich, Germany

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1 Summary of Features

The XMC4[12]00 devices are members of the XMC4000 Family of microcontrollers based on the ARM Cortex-M4 processor core. The XMC4000 is a family of high performance and energy efficient microcontrollers optimized for Industrial Connectivity, Industrial Control, Power Conversion, Sense & Control.

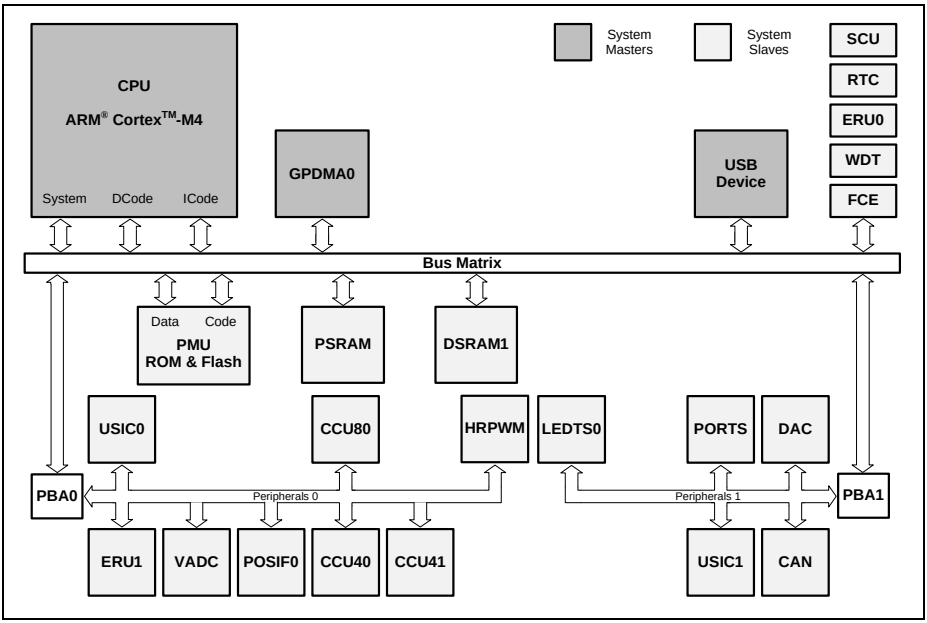

Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
  - High Performance 32-bit ARM Cortex-M4 CPU
  - 16-bit and 32-bit Thumb2 instruction set
  - DSP/MAC instructions
  - System timer (SysTick) for Operating System support
- Floating Point Unit
- Memory Protection Unit
- Nested Vectored Interrupt Controller
- One General Purpose DMA with up-to 8 channels
- Event Request Unit (ERU) for programmable processing of external and internal service requests
- Flexible CRC Engine (FCE) for multiple bit error detection

1.3 Package Variants

Different markings of the XMC4[12]00 use different package variants. Details of those packages are given in the **Package Parameters** section of the Data Sheet.

Table 2 XMC4[12]00 Package Variants

Package Variant	Marking	Package
XMC4[12]00-F64	EES-AA, ES-AA, ES-AB, AB	PG-LQFP-64-19
XMC4[12]00-Q48		PG-VQFN-48-53
XMC4[12]00-F64	BA	PG-TQFP-64-19
XMC4[12]00-Q48		PG-VQFN-48-71

1.4 Device Type Features

The following table lists the available features per device type.

Table 3 Features of XMC4[12]00 Device Types

Derivative[1)]	LEDTS Intf.	USB Intf.	USIC Chan.	MultiCAN Nodes, MO
XMC4200-F64x256	1	1	2 x 2	N0, N1 MO[0..63]
XMC4200-Q48x256	1	1	2 x 2	N0, N1 MO[0..63]
XMC4100-F64x128	1	1	2 x 2	N0, N1 MO[0..63]
XMC4100-Q48x128	1	1	2 x 2	N0, N1 MO[0..63]
XMC4104-F64x64	1	–	2 x 2	–
XMC4104-Q48x64	1	–	2 x 2	–
XMC4104-F64x128	1	–	2 x 2	–
XMC4104-Q48x128	1	–	2 x 2	–
XMC4108-F64x64	–	–	2 x 2	N0, MO[0..31]
XMC4108-Q48x64	–	–	2 x 2	N0, MO[0..31]

1) x is a placeholder for the supported temperature range.

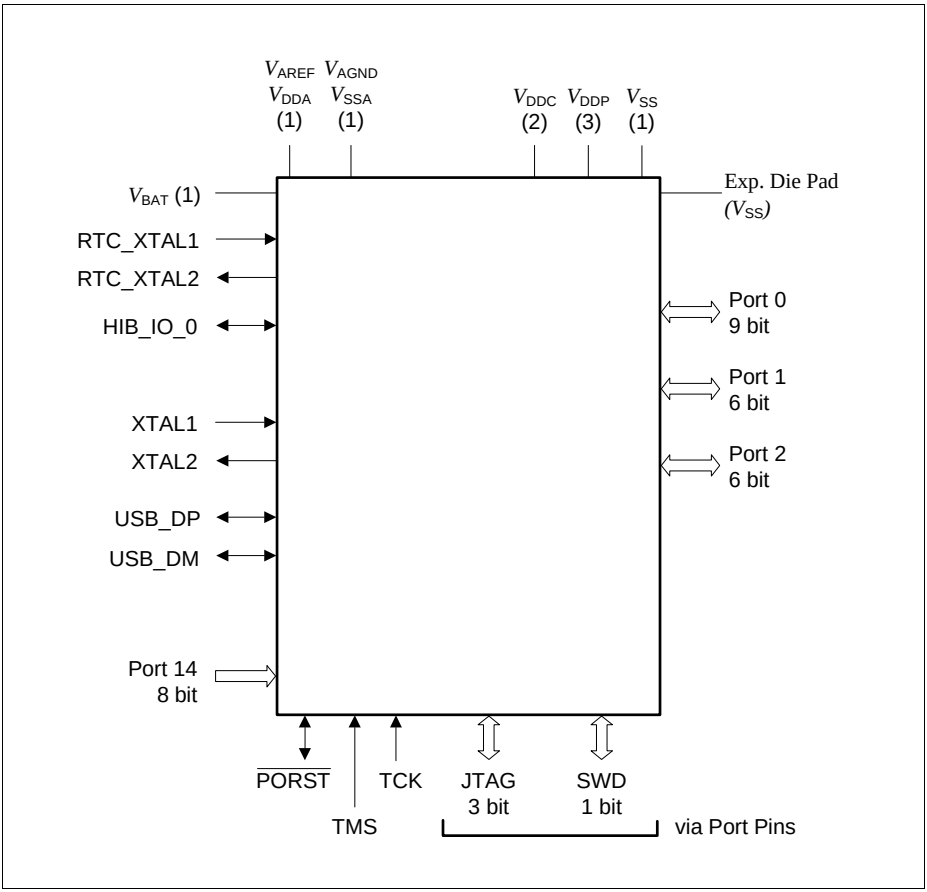

Figure 3 XMC4[12]00 Logic Symbol PG-VQFN-48

Table 11 Package Pin Mapping (cont'd)

Function	LQFP-64 TQFP-64	VQFN-48	Pad Type	Notes
VSSO	41	-	Power	
VSS	Exp. Pad	Exp. Pad	Power	**Exposed Die Pad** The exposed die pad is connected internally to VSS. For proper operation, it is mandatory to connect the exposed pad directly to the common ground on the board. For thermal aspects, please refer to the Data Sheet. Board layout examples are given in an application note.

2.2.2 Port I/O Functions

The following general scheme is used to describe each PORT pin:

Table 12 Port I/O Function Description

Function	Outputs			Inputs		
	ALT1	ALTn	HWO0	HWI0	Input	Input
P0.0		MODA.OUT	MODB.OUT	MODB.INA	MODC.INA	
Pn.y	MODA.OUT				MODA.INA	MODC.INB

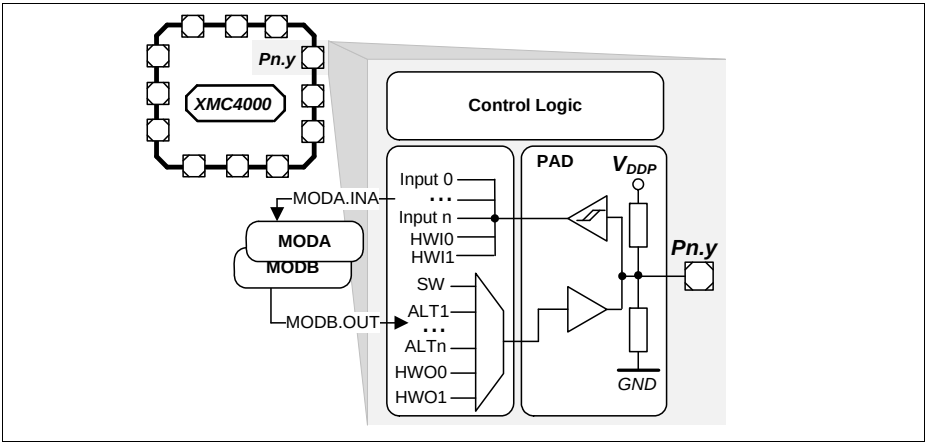

Figure 6 Simplified Port Structure

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to four alternate output functions (ALT1/2/3/4) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.
The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL it is possible to select between different hardware “masters” (HWO0/HWI0). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

2.2.2.1 Port I/O Function Table

Table 13 Port I/O Functions

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO0	HWI0	Input	Input	Input	Input	Input	Input	Input	Input
P0.0		CAN. N0_TXD	CCU80. OUT21	LEDTS0. COL2			U1C1. DX0D		ERU0. 0B0	USB. VBUSDETECT A		HRPWM0. C1INB		
P0.1		U1C1. DOUT0	CCU80. OUT11	LEDTS0. COL3					ERU0. 0A0			HRPWM0. C2INB		
P0.2		U1C1. SELO1	CCU80. OUT01	HRPWM0. HROUT01	U1C0. DOUT3	U1C0. HWIN3			ERU0. 3B3					
P0.3			CCU80. OUT20	HRPWM0. HROUT20	U1C0. DOUT2	U1C0. HWIN2				ERU1. 3B0				
P0.4			CCU80. OUT10	HRPWM0. HROUT21	U1C0. DOUT1	U1C0. HWIN1		U1C0. DX0A	ERU0. 2B3					
P0.5		U1C0. DOUT0	CCU80. OUT00	HRPWM0. HROUT00	U1C0. DOUT0	U1C0. HWIN0		U1C0. DX0B		ERU1. 3A0				
P0.6		U1C0. SELO0	CCU80. OUT30	HRPWM0. HROUT30				U1C0. DX2A	ERU0. 3B2		CCU80. IN2B			
P0.7	WWDT. SERVICE_OUT	U0C0. SELO0		HRPWM0. HROUT11		DB. TDI	U0C0. DX2B		ERU0. 2B1		CCU80. IN0A	CCU80. IN1A	CCU80. IN2A	CCU80. IN3A
P0.8	SCU. EXTCLK	U0C0. SCLKOUT		HRPWM0. HROUT10		$\overline{\text{DB.}}$ $\overline{\text{TRST}}$	U0C0. DX1B		ERU0. 2A1		CCU80. IN1B			
P0.9	HRPWM0. HROUT31	U1C1. SELO0	CCU80. OUT12	LEDTS0. COL0			U1C1. DX2A		ERU0. 1B0					
P0.10		U1C1. SCLKOUT	CCU80. OUT02	LEDTS0. COL1			U1C1. DX1A		ERU0. 1A0					
P0.11		U1C0. SCLKOUT	CCU80. OUT31					U1C0. DX1A	ERU0. 3A2					
P1.0		U0C0. SELO0	CCU40. OUT3	ERU1. PDOUT3			U0C0. DX2A		ERU0. 3B0		CCU40. IN3A	HRPWM0. C0INA		
P1.1		U0C0. SCLKOUT	CCU40. OUT2	ERU1. PDOUT2			U0C0. DX1A	POSIF0. IN2A	ERU0. 3A0		CCU40. IN2A	HRPWM0. C1INA		
P1.2			CCU40. OUT1	ERU1. PDOUT1	U0C0. DOUT3	U0C0. HWIN3		POSIF0. IN1A		ERU1. 2B0	CCU40. IN1A	HRPWM0. C2INA		
P1.3		U0C0. MCLKOUT	CCU40. OUT0	ERU1. PDOUT0	U0C0. DOUT2	U0C0. HWIN2		POSIF0. IN0A		ERU1. 2A0	CCU40. IN0A	HRPWM0. C0INB		
P1.4	WWDT. SERVICE_OUT	CAN. N0_TXD	CCU80. OUT33		U0C0. DOUT1	U0C0. HWIN1	U0C0. DX0B	CAN. N1_RXDD	ERU0. 2B0		CCU41. IN0C	HRPWM0. BL0A		
P1.5	CAN. N1_TXD	U0C0. DOUT0	CCU80. OUT23		U0C0. DOUT0	U0C0. HWIN0	U0C0. DX0A	CAN. N0_RXDA	ERU0. 2A0	ERU1. 0A0	CCU41. IN1C			
P1.7		U0C0. DOUT0		U1C1. SELO2						USB. VBUSDETECT B				

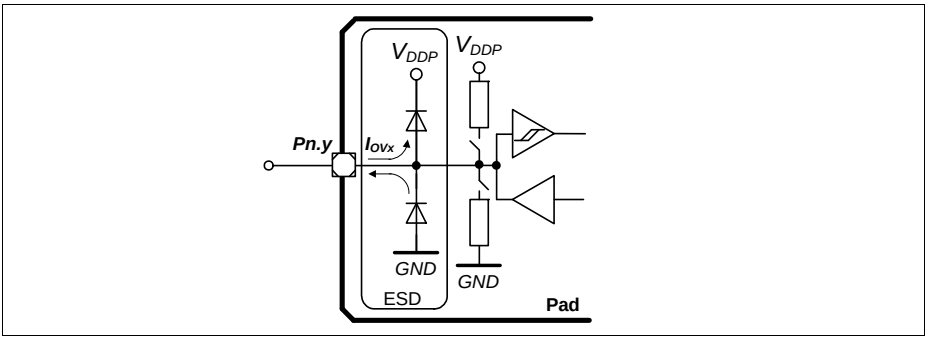

Figure 9 Input Overload Current via ESD structures

Table 16 and **Table 17** list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the **Absolute Maximum Ratings** must not be exceeded during overload.

Table 16 PN-Junction Characterisitics for positive Overload

Pad Type	I_{OV} = 5 mA, T_J = -40 °C	I_{OV} = 5 mA, T_J = 150 °C
A1 / A1+	$V_{IN} = V_{DDP} + 1.0$ V	$V_{IN} = V_{DDP} + 0.75$ V
AN/DIG_IN	$V_{IN} = V_{DDP} + 1.0$ V	$V_{IN} = V_{DDP} + 0.75$ V

Table 17 PN-Junction Characterisitics for negative Overload

Pad Type	I_{OV} = 5 mA, T_J = -40 °C	I_{OV} = 5 mA, T_J = 150 °C
A1 / A1+	$V_{IN} = V_{SS} - 1.0$ V	$V_{IN} = V_{SS} - 0.75$ V
AN/DIG_IN	$V_{IN} = V_{DDP} - 1.0$ V	$V_{IN} = V_{DDP} - 0.75$ V

Table 18 Port Groups for Overload and Short-Circuit Current Sum Parameters

Group	Pins
1	P0.[12:0], P3.0
2	P14.[8:0]
3	P2.[15:0]
4	P1.[15:0]

3.1.4 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in the **Section 3.2.1**.

Table 19 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub-Class	Speed Grade	Load	Termination
A	3.3 V	LVTTL I/O, LVTTL outputs	**A1** (e.g. GPIO)	6 MHz	100 pF	No
			A1+ (e.g. serial I/Os)	25 MHz	50 pF	Series termination recommended

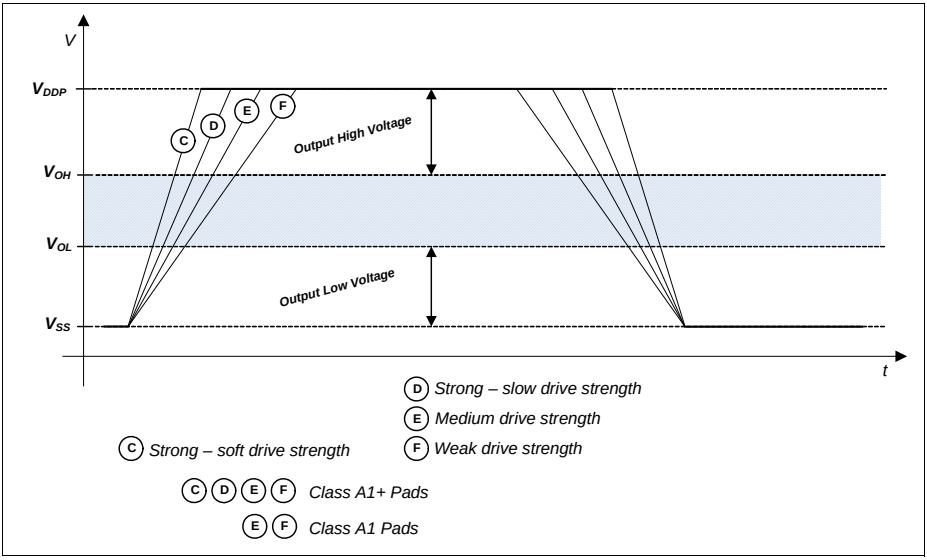

Figure 10 Output Slopes with different Pad Driver Modes

Figure 10 is a qualitative display of the resulting output slope performance with different output driver modes. The detailed input and output characteristics are listed in **Section 3.2.1**.

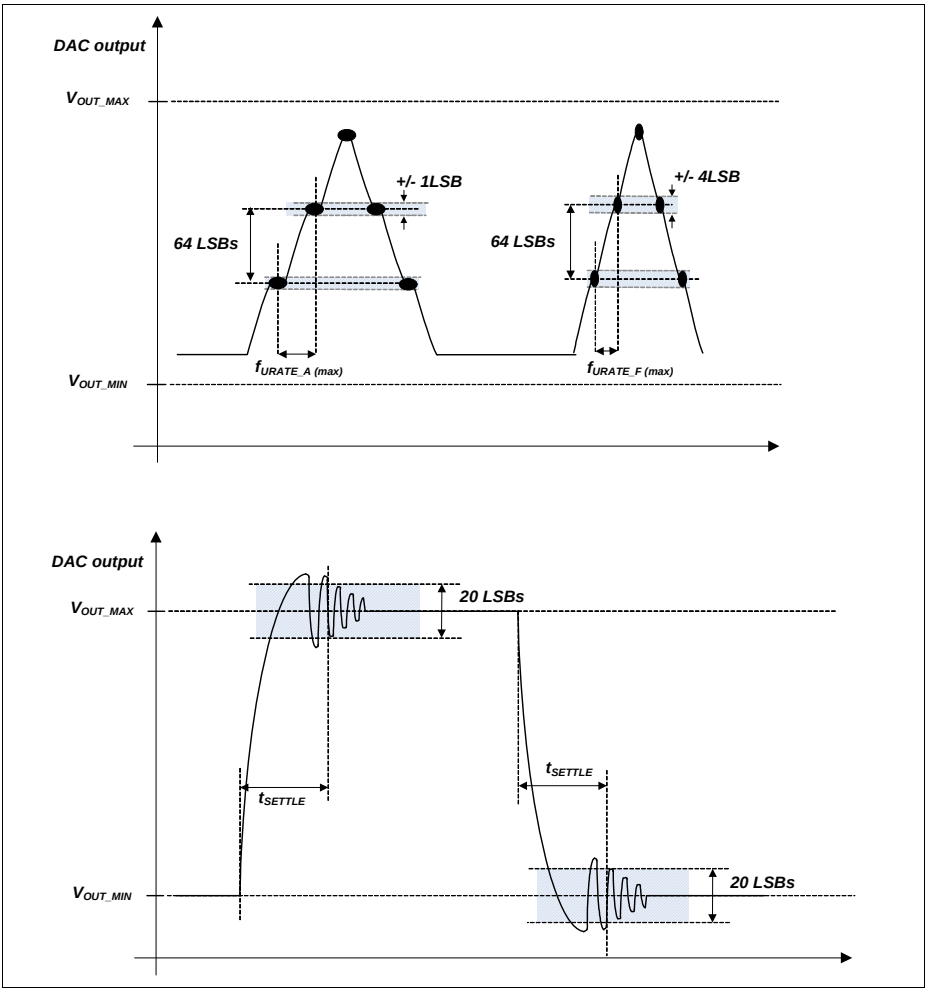

Figure 15 DAC Conversion Examples

3.2.4 Out-of-Range Comparator (ORC)

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above the analog reference[1] (V_{AREF}) on selected input pins (GxORCy) and generates a service request trigger (GxORCOUTy).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The parameters in **Table 28** apply for the maximum reference voltage $V_{AREF} = V_{DDA} + 50$ mV.

Table 28 ORC Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DC Switching Level	V_{ODC}	CC	100	125	200	mV	Ax-marking devices $V_{AIN} \geq V_{AREF} + V_{ODC}$
Hysteresis	V_{OHYS}	CC	50	–	V_{ODC}	mV	
Detection Delay of a persistent Overvoltage	t_{ODD}	CC	55	–	450	ns	Ax-marking devices $V_{AIN} \geq V_{AREF} + 200$ mV
			45	–	105	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Always detected Overvoltage Pulse	t_{OPDD}	CC	440	–	–	ns	Ax-marking devices $V_{AIN} \geq V_{AREF} + 200$ mV
			90	–	–	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Never detected Overvoltage Pulse	t_{OPDN}	CC	–	–	49	ns	Ax-marking devices $V_{AIN} \geq V_{AREF} + 200$ mV
			–	–	30	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Release Delay	t_{ORD}	CC	65	–	105	ns	$V_{AIN} \leq V_{AREF}$
Enable Delay	t_{OED}	CC	–	100	200	ns	

1) Always the standard VADC reference, alternate references do not apply to the ORC.

Table 32 External clock operating conditions

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Frequency	f_{eclk}	SR	–	–	$f_{hrpwm}/4$	MHz	
ON time	t_{oneclk}	SR	$2T_{ccu}$ [1)2)]	–	–	ns	
OFF time	$t_{offeclk}$	SR	$2T_{ccu}$ [1)2)]	–	–	ns	Only the rising edge is used

1) 50% duty cycle is not obligatory

2) Only valid if the signal was not previously synchronized/generated with the fccu clock (or a synchronous clock)

3.2.6 Low Power Analog Comparator (LPAC)

The Low Power Analog Comparator (LPAC) triggers a wake-up event from Hibernate state or an interrupt trigger during normal operation. It does so by comparing V_{BAT} or another external sensor voltage V_{LPS} with a pre-programmed threshold voltage.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 33 Low Power Analog Comparator Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
V_{BAT} supply voltage range for LPAC operation	V_{BAT}	SR	2.1	–	3.6	V	
Sensor voltage range	V_{LPCS}	CC	0	–	1.2	V	
Threshold step size	V_{th}	CC	–	18.75	–	mV	
Threshold trigger accuracy	ΔV_{th}	CC	–	–	±10	%	for V_{th} > 0.4 V
Conversion time	t_{LPCC}	CC	–	–	250	µs	
Average current consumption over time	I_{LPCAC}	CC	–	–	15	µA	conversion interval 10 ms[1)]
Current consumption during conversion	I_{LPCC}	CC	–	150	–	µA	[1)]

1) Single channel conversion, measuring V_{BAT} = 3.3 V, 8 cycles settling time

Table 38 Power Supply Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sleep supply current[3] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS} CC	–	76	–	mA	80 / 80 / 80
		–	73	–		80 / 40 / 40
		–	70	–		40 / 40 / 80
		–	56	–		24 / 24 / 24
		–	47	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	46	–		100 / 100 / 100
Sleep supply current[4] Peripherals disabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS} CC	–	59	–	mA	80 / 80 / 80
		–	58	–		80 / 40 / 40
		–	57	–		40 / 40 / 80
		–	51	–		24 / 24 / 24
		–	46	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	46	–		100 / 100 / 100
Deep Sleep supply current[5] Flash in Sleep mode Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPD} CC	–	6.9	–	mA	24 / 24 / 24
		–	4.3	–		4 / 4 / 4
		–	3.8	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	4.5	–		100 / 100 / 100 [6]
Hibernate supply current RTC on[7]	I_{DDPH} CC	–	10.8	–	µA	V_{BAT} = 3.3 V
		–	8.0	–		V_{BAT} = 2.4 V
		–	6.8	–		V_{BAT} = 2.0 V
Hibernate supply current RTC off[8]	I_{DDPH} CC	–	10.3	–	µA	V_{BAT} = 3.3 V
		–	7.5	–		V_{BAT} = 2.4 V
		–	6.3	–		V_{BAT} = 2.0 V
Worst case active supply current[9]	I_{DDPA} CC	–	–	140 [10]	mA	V_{DDP} = 3.6 V, T_J = 150 °C
V_{DDA} power supply current	I_{DDA} CC	–	–	–[11]	mA	
I_{DDP} current at $\overline{\text{PORST}}$ Low	I_{DDP_PORST} CC	–	–	24	mA	V_{DDP} = 3.6 V, T_J = 150 °C

3.3 AC Parameters

3.3.1 Testing Waveforms

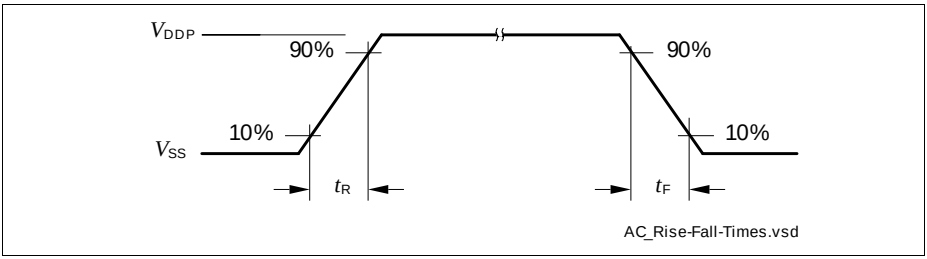

Figure 23 Rise/Fall Time Parameters

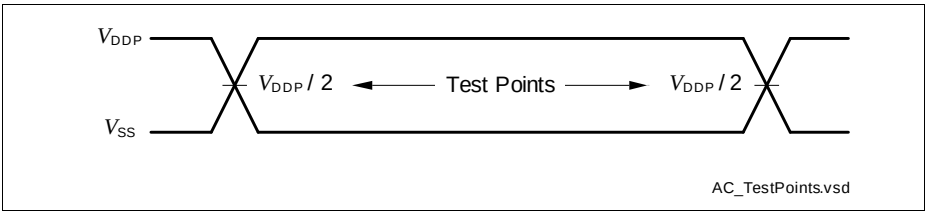

Figure 24 Testing Waveform, Output Delay

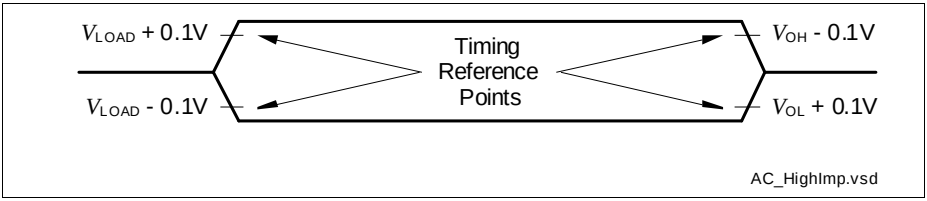

Figure 25 Testing Waveform, Output High Impedance

Slow Internal Clock Source

Table 45 Slow Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal frequency	f_{OSI} CC	–	32.768	–	kHz	
Accuracy	Δf_{OSI} CC	-4	–	4	%	V_{BAT} = const. 0 °C ≤ T_A ≤ 85 °C
		-5	–	5	%	V_{BAT} = const. T_A < 0 °C or T_A > 85 °C
		-5	–	5	%	2.4 V ≤ V_{BAT}, T_A = 25 °C
		-10	–	10	%	1.95 V ≤ V_{BAT} < 2.4 V, T_A = 25 °C
Start-up time	t_{OSIS} CC	–	50	–	µs	

3.3.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

Table 46 JTAG Interface Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TCK clock period	t_1	SR	30	–	–	ns	For C_L = 20 pF on TDO
TCK clock period	t_1	SR	40	–	–	ns	For C_L = 50 pF on TDO
TCK high time	t_2	SR	10	–	–	ns	
TCK low time	t_3	SR	10	–	–	ns	
TCK clock rise time	t_4	SR	–	–	4	ns	
TCK clock fall time	t_5	SR	–	–	4	ns	
TDI/TMS setup to TCK rising edge	t_6	SR	6	–	–	ns	
TDI/TMS hold after TCK rising edge	t_7	SR	6	–	–	ns	
TDO valid after TCK falling edge[1] (propagation delay)	t_8	CC	–	–	17	ns	C_L = 50 pF
			3	–	–	ns	C_L = 20 pF
TDO hold after TCK falling edge[1]	t_{18}	CC	2	–	–	ns	
TDO high imped. to valid from TCK falling edge[1)2)]	t_9	CC	–	–	14	ns	C_L = 50 pF
TDO valid to high imped. from TCK falling edge[1]	t_{10}	CC	–	–	13.5	ns	C_L = 50 pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

3.3.7 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

Table 47 SWD Interface Timing Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SWDCLK clock period	t_{SC}	SR	25	–	–	ns	C_L = 30 pF
			40	–	–	ns	C_L = 50 pF
SWDCLK high time	t_1	SR	10	–	500000	ns	
SWDCLK low time	t_2	SR	10	–	500000	ns	
SWDIO input setup to SWDCLK rising edge	t_3	SR	6	–	–	ns	
SWDIO input hold after SWDCLK rising edge	t_4	SR	6	–	–	ns	
SWDIO output valid time after SWDCLK rising edge	t_5	CC	–	–	17	ns	C_L = 50 pF
			–	–	13	ns	C_L = 30 pF
SWDIO output hold time from SWDCLK rising edge	t_6	CC	3	–	–	ns	

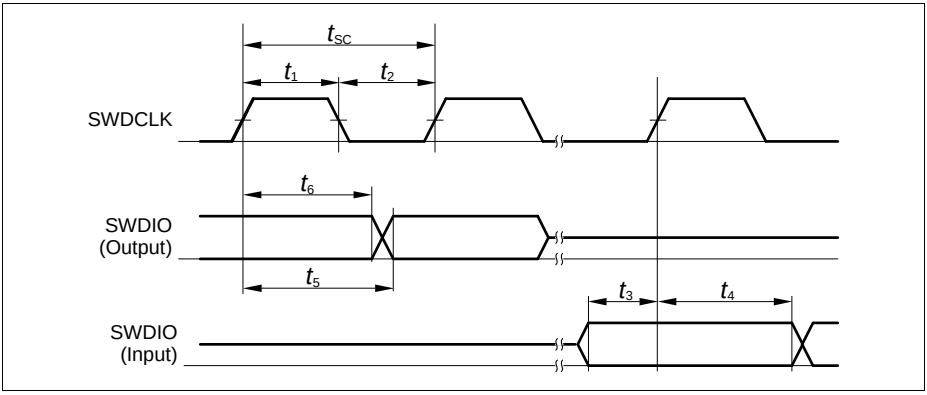

Figure 30 SWD Timing

4 Package and Reliability

The XMC4[12]00 is a member of the XMC4000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the Exposed Die Pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 55 provides the thermal characteristics of the packages used in XMC4[12]00. The availability of different packages for different markings is listed in **Table 2**.

Table 55 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad Dimensions	Ex × Ey CC	-	5.8 × 5.8	mm	PG-LQFP-64-19
		-	5.7 × 5.7	mm	PG-TQFP-64-19
		-	5.2 × 5.2	mm	PG-VQFN-48-53
		-	5.2 × 5.2	mm	PG-VQFN-48-71
Thermal resistance Junction-Ambient	$R_{\Theta JA}$ CC	-	30	K/W	PG-LQFP-64-19[1)]
		-	23.4	K/W	PG-TQFP-64-19[1)]
		-	34.8	K/W	PG-VQFN-48-53[1)] PG-VQFN-48-71[1)]

1) Device mounted on a 4-layer JEDEC board (JESD 51-7) with thermal vias; exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SS}, independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMC4[12]00 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The

5 Quality Declarations

The qualification of the XMC4[12]00 is executed according to the JEDEC standard JESD47H.

Note: For automotive applications refer to the Infineon automotive microcontrollers.

Table 58 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation lifetime	t_{OP} CC	20	–	–	a	$T_J \leq 109°C$, device permanent on
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	–	2 000	V	EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} SR	–	–	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	–	–	3	–	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	–	–	260	°C	Profile according to JEDEC J-STD-020D