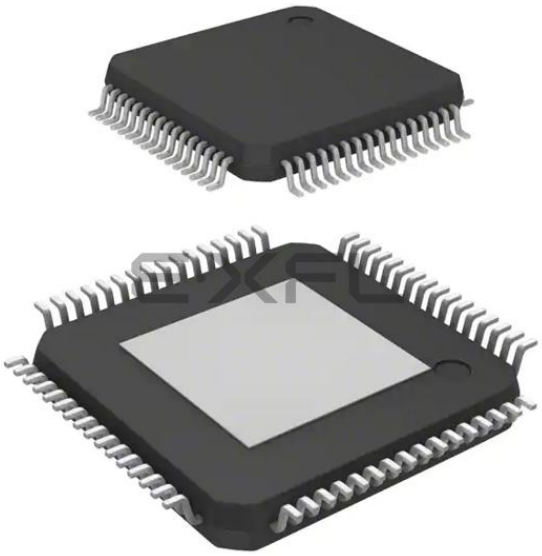
Infineon Technologies - XMC4108F64K64BAXQMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-64-19
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4108f64k64baxqma1

On-Chip Memories

- 16 KB on-chip boot ROM
- up to 16 KB on-chip high-speed program memory
- up to 24 KB on-chip high speed data memory
- up to 256 KB on-chip Flash Memory with 1 KB instruction cache

Communication Peripherals

- Universal Serial Bus, USB 2.0 device, with integrated PHY
- Controller Area Network interface (MultiCAN), Full-CAN/Basic-CAN with two nodes, 64 message objects (MO), data rate up to 1 MBit/s
- Four Universal Serial Interface Channels (USIC), providing four serial channels, usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- LED and Touch-Sense Controller (LEDTS) for Human-Machine interface

Analog Frontend Peripherals

- Two Analog-Digital Converters (VADC) of 12-bit resolution, 8 channels each, with input out-of-range comparators
- Digital-Analog Converter (DAC) with two channels of 12-bit resolution

Industrial Control Peripherals

- Two Capture/Compare Units 4 (CCU4) for use as general purpose timers
- One Capture/Compare Units 8 (CCU8) for motor control and power conversion
- Four High Resoultion PWM (HRPWM) channels
- One Position Interface (POSIF) for servo motor positioning
- Window Watchdog Timer (WDT) for safety sensitive applications
- Die Temperature Sensor (DTS)
- Real Time Clock module with alarm support
- System Control Unit (SCU) for system configuration and control

Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability
- Tri-stated in input mode
- Push/pull or open drain output mode
- Boundary scan test support over JTAG interface

On-Chip Debug Support

- Full support for debug features: 8 breakpoints, CoreSight, trace
- Various interfaces: ARM-JTAG, SWD, single wire trace

1.3 Package Variants

Different markings of the XMC4[12]00 use different package variants. Details of those packages are given in the **Package Parameters** section of the Data Sheet.

Table 2 XMC4[12]00 Package Variants

Package Variant	Marking	Package
XMC4[12]00-F64	EES-AA, ES-AA, ES-AB, AB	PG-LQFP-64-19
XMC4[12]00-Q48		PG-VQFN-48-53
XMC4[12]00-F64	BA	PG-TQFP-64-19
XMC4[12]00-Q48		PG-VQFN-48-71

1.4 Device Type Features

The following table lists the available features per device type.

Table 3 Features of XMC4[12]00 Device Types

Derivative[1)]	LEDTS Intf.	USB Intf.	USIC Chan.	MultiCAN Nodes, MO
XMC4200-F64x256	1	1	2 x 2	N0, N1 MO[0..63]
XMC4200-Q48x256	1	1	2 x 2	N0, N1 MO[0..63]
XMC4100-F64x128	1	1	2 x 2	N0, N1 MO[0..63]
XMC4100-Q48x128	1	1	2 x 2	N0, N1 MO[0..63]
XMC4104-F64x64	1	–	2 x 2	–
XMC4104-Q48x64	1	–	2 x 2	–
XMC4104-F64x128	1	–	2 x 2	–
XMC4104-Q48x128	1	–	2 x 2	–
XMC4108-F64x64	–	–	2 x 2	N0, MO[0..31]
XMC4108-Q48x64	–	–	2 x 2	N0, MO[0..31]

1) x is a placeholder for the supported temperature range.

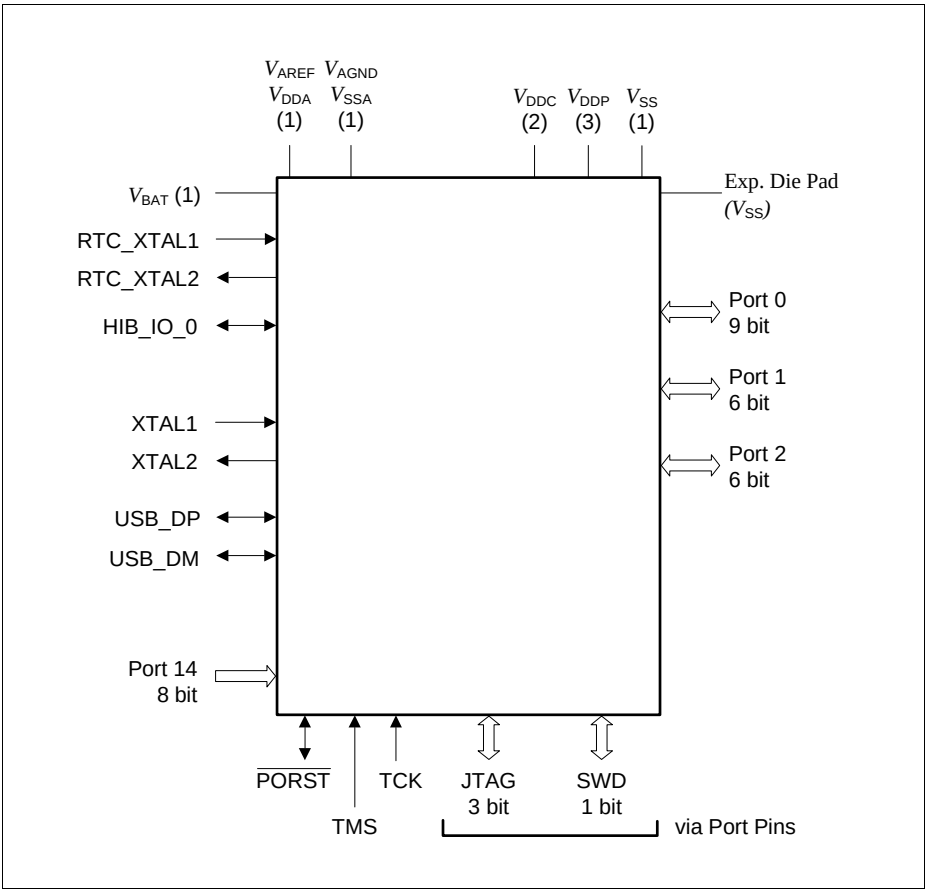

Figure 3 XMC4[12]00 Logic Symbol PG-VQFN-48

2.2.2 Port I/O Functions

The following general scheme is used to describe each PORT pin:

Table 12 Port I/O Function Description

Function	Outputs			Inputs		
	ALT1	ALTn	HWO0	HWI0	Input	Input
P0.0		MODA.OUT	MODB.OUT	MODB.INA	MODC.INA	
Pn.y	MODA.OUT				MODA.INA	MODC.INB

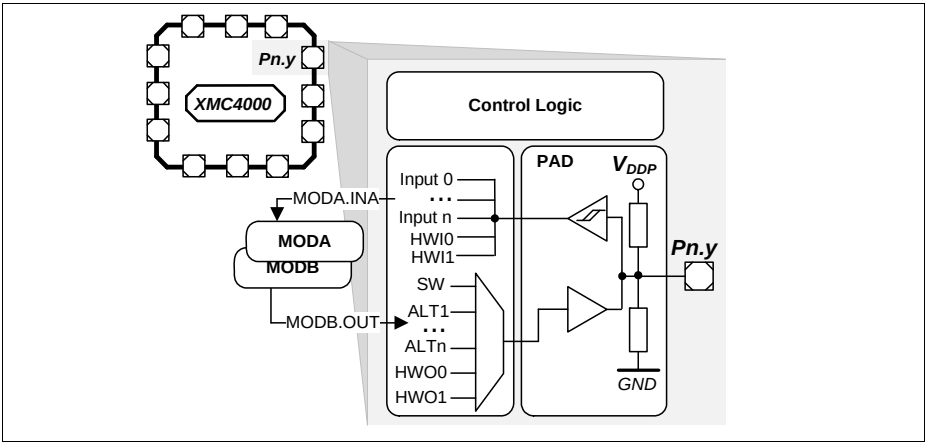

Figure 6 Simplified Port Structure

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to four alternate output functions (ALT1/2/3/4) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.
The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL it is possible to select between different hardware “masters” (HWO0/HWI0). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

Table 13 Port I/O Functions (cont'd)

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO0	HWI0	Input	Input	Input	Input	Input	Input	Input	Input
P1.8		U0C0. SELO1		U1C1. SCLKOUT										
P1.9	U0C0. SCLKOUT			U1C1. DOUT0										
P1.15	SCU. EXTCLK			U1C0. DOUT0						ERU1. 1A0				
P2.0	CAN. N0_TXD			LEDTS0. COL1					ERU0. 0B3		CCU40. IN1C			
P2.1				LEDTS0. COL0	DB.TDO/ TRACESWO					ERU1. 0B0	CCU40. IN0C			
P2.2	VADC. EMUX00		CCU41. OUT3	LEDTS0. LINE0	LEDTS0. EXTENDED0	LEDTS0. TSIN0A		U0C1. DX0A	ERU0. 1B2		CCU41. IN3A			
P2.3	VADC. EMUX01	U0C1. SELO0	CCU41. OUT2	LEDTS0. LINE1	LEDTS0. EXTENDED1	LEDTS0. TSIN1A		U0C1. DX2A	ERU0. 1A2		CCU41. IN2A			
P2.4	VADC. EMUX02	U0C1. SCLKOUT	CCU41. OUT1	LEDTS0. LINE2	LEDTS0. EXTENDED2	LEDTS0. TSIN2A		U0C1. DX1A	ERU0. 0B2		CCU41. IN1A	HRPWM0. BL1A		
P2.5		U0C1. DOUT0	CCU41. OUT0	LEDTS0. LINE3	LEDTS0. EXTENDED3	LEDTS0. TSIN3A		U0C1. DX0B	ERU0. 0A2		CCU41. IN0A	HRPWM0. BL2A		
P2.6			CCU80. OUT13	LEDTS0. COL3				CAN. N1_RXDA	ERU0. 1B3		CCU40. IN3C			
P2.7		CAN. N1_TXD	CCU80. OUT03	LEDTS0. COL2						ERU1. 1B0	CCU40. IN2C			
P2.8			CCU80. OUT32	LEDTS0. LINE4	LEDTS0. EXTENDED4	LEDTS0. TSIN4A	DAC. TRIGGER5				CCU40. IN0B	CCU40. IN1B	CCU40. IN2B	CCU40. IN3B
P2.9			CCU80. OUT22	LEDTS0. LINE5	LEDTS0. EXTENDED5	LEDTS0. TSIN5A	DAC. TRIGGER4				CCU41. IN0B	CCU41. IN1B	CCU41. IN2B	CCU41. IN3B
P2.14	VADC. EMUX11	U1C0. DOUT0	CCU80. OUT21					U1C0. DX0D						
P2.15	VADC. EMUX12		CCU80. OUT11	LEDTS0. LINE6	LEDTS0. EXTENDED6	LEDTS0. TSIN6A		U1C0. DX0C						
P3.0		U0C1. SCLKOUT					U0C1. DX1B				CCU80. IN2C			
P14.0							VADC. G0CH0							
P14.3							VADC. G0CH3	VADC. G1CH3			CAN. N0_RXDB			
P14.4							VADC. G0CH4							
P14.5							VADC. G0CH5				POSIF0. IN2B			
P14.6							VADC. G0CH6				POSIF0. IN1B		G0ORC6	
P14.7							VADC. G0CH7				POSIF0. IN0B			
P14.8					DAC. OUT_0			VADC. G1CH0						

The XMC4[12]00 has a common ground concept, all V_{SS}, V_{SSA} and V_{SSO} pins share the same ground potential. In packages with an exposed die pad it must be connected to the common ground as well.

There are no dedicated connections for the analog reference V_{AREF} and V_{AGND}. Instead, they share the same pins as the analog supply pins V_{DDA} and V_{SSA}.Some analog channels can optionally serve as “Alternate Reference”; further details on this operating mode are described in the Reference Manual.

When V_{DDP} is supplied, V_{BAT} must be supplied as well. If no other supply source (e.g. battery) is connected to V_{BAT}, the V_{BAT} pin can also be connected directly to V_{DDP}.

Figure 8 explains the input voltage ranges of V_{IN} and V_{AIN} and its dependency to the supply level of V_{DDP}.The input voltage must not exceed 4.3 V, and it must not be more than 1.0 V above V_{DDP}. For the range up to V_{DDP} + 1.0 V also see the definition of the overload conditions in **Section 3.1.3**.

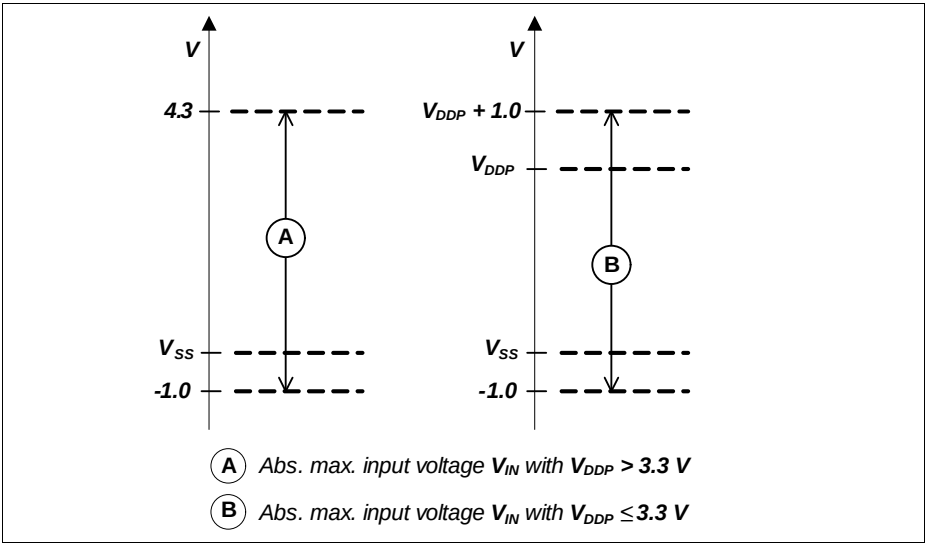

Figure 8 Absolute Maximum Input Voltage Ranges

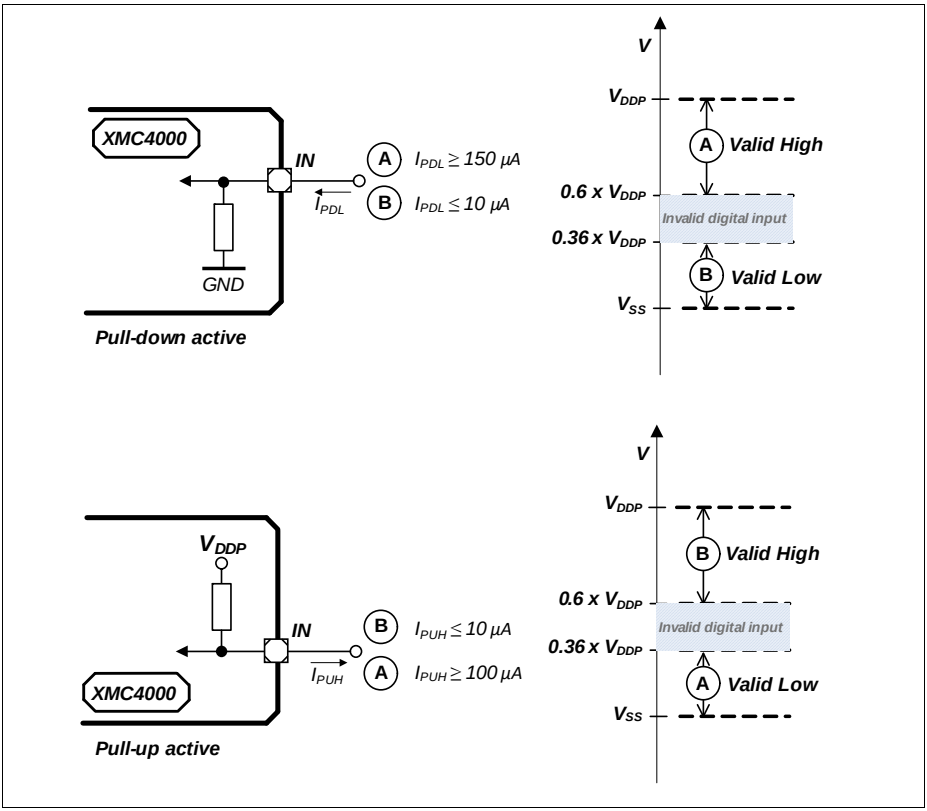

Figure 11 Pull Device Input Characteristics

Figure 11 visualizes the input characteristics with an active internal pull device:

- in the cases “A” the internal pull device is overridden by a strong external driver;
- in the cases “B” the internal pull device defines the input logical state against a weak external load.

Table 23 Standard Pads Class_A1+

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Output high voltage, POD[1] = weak	V_{OHA1+} CC	V_{DDP} - 0.4		–	V	$I_{OH} \geq$ -400 µA
		2.4		–	V	$I_{OH} \geq$ -500 µA
Output high voltage, POD[1] = medium		V_{DDP} - 0.4		–	V	$I_{OH} \geq$ -1.4 mA
		2.4		–	V	$I_{OH} \geq$ -2 mA
Output high voltage, POD[1] = strong		V_{DDP} - 0.4		–	V	$I_{OH} \geq$ -1.4 mA
		2.4		–	V	$I_{OH} \geq$ -2 mA
Output low voltage	V_{OLA1+} CC	–		0.4	V	$I_{OL} \leq$ 500 µA; POD[1] = weak
		–		0.4	V	$I_{OL} \leq$ 2 mA; POD[1] = medium
		–		0.4	V	$I_{OL} \leq$ 2 mA; POD[1] = strong
Fall time	t_{FA1+} CC	–		150	ns	C_L = 20 pF; POD[1] = weak
		–		50	ns	C_L = 50 pF; POD[1] = medium
		–		28	ns	C_L = 50 pF; POD[1] = strong; edge = slow
		–		16	ns	C_L = 50 pF; POD[1] = strong; edge = soft;
Rise time	t_{RA1+} CC	–		150	ns	C_L = 20 pF; POD[1] = weak
		–		50	ns	C_L = 50 pF; POD[1] = medium
		–		28	ns	C_L = 50 pF; POD[1] = strong; edge = slow
		–		16	ns	C_L = 50 pF; POD[1] = strong; edge = soft

1) POD = Pin Out Driver

Table 25 ADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Total capacitance of the alternate reference inputs[5]	$C_{AREFTOT}$ CC	–	20	40	pF	
Total Unadjusted Error	TUE CC	-6	–	6	LSB	12-bit resolution; V_{DDA} = 3.3 V; $V_{AREF} = V_{DDA}$[7]
Differential Non-Linearity Error[8]	EA_{DNL} CC	-4.5	–	4.5	LSB	
Gain Error[8]	EA_{GAIN} CC	-6	–	6	LSB	
Integral Non-Linearity[8]	EA_{INL}CC	-4.5	–	4.5	LSB	
Offset Error[8]	EA_{OFF} CC	-6	–	6	LSB	
Worst case ADC V_{DDA} power supply current per active converter	I_{DDAA} CC	–	1.5	2	mA	during conversion V_{DDP} = 3.6 V, T_J = 150 °C
Charge consumption on alternate reference per conversion[5]	Q_{CONV} CC	–	30	–	pC	0 V ≤ V_{AREF} ≤ V_{DDA}[9]
ON resistance of the analog input path	R_{AIN} CC	–	600	1 200	Ohm	
ON resistance for the ADC test (pull down for AIN7)	R_{AIN7T} CC	180	550	900	Ohm	

1) A running conversion may become imprecise in case the normal conditions are violated (voltage overshoot).
2) If the analog reference voltage is below V_{DDA}, then the ADC converter errors increase. If the reference voltage is reduced by the factor k (k<1), TUE, DNL, INL, Gain, and Offset errors increase also by the factor 1/k.
3) The leakage current definition is a continuous function, as shown in figure ADCx Analog Inputs Leakage. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function (see **Figure 14**).
4) The sampling capacity of the conversion C-network is pre-charged to V_{AREF}/2 before the sampling moment. Because of the parasitic elements, the voltage measured at AINx can deviate from V_{AREF}/2.
5) Applies to AINx, when used as alternate reference input.
6) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead, smaller capacitances are successively switched to the reference voltage.
7) For 10-bit conversions, the errors are reduced to 1/4; for 8-bit conversions, the errors are reduced to 1/16. Never less than ±1 LSB.
8) The sum of DNL/INL/GAIN/OFF errors does not exceed the related total unadjusted error TUE.

3.2.5 High Resolution PWM (HRPWM)

The following chapters describe the operating conditions, characteristics and timing requirements, for all the components inside the HRPWM module. Each description is given for just one sub unit, e.g., one CSG or one HRC.

All the timing information is related to the module clock, f_{hrpwm}.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.2.5.1 HRC characteristics

Table 29 summarizes the characteristics of the HRC units.

Table 29 HRC characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
High resolution step size[1)2)]	t_{HRS} CC	–	150	–	ps	
Startup time (after reset release)	t_{start} CC	–	–	2	µs	

1) The step size for clock frequencies equal to 180, 120 and 80 MHz is 150 ps.

2) The step size for clock frequencies different from 180, 120 and 80 MHz but within the range from 180 to 64 MHz can be between 118 to 180 ps (fixed over process and operating conditions)

3.2.5.2 CMP and 10-bit DAC characteristics

The **Table 30** summarizes the characteristics of the CSG unit.

The specified characteristics require that the setup of the HRPWM follows the initialization sequence as documented in the Reference Manual.

Table 30 CMP and 10-bit DAC characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAC Resolution	*RES* CC		10		bits	
DAC differential nonlinearity	*DNL CC*	-1	–	1.5	LSB	Monotonic behavior, See **Figure 18**
DAC integral nonlinearity	*INL* CC	-3	–	3	LSB	See **Figure 18**

3.2.9 Oscillator Pins

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The oscillator pins can be operated with an external crystal (see **Figure 21**) or in direct input mode (see **Figure 22**).

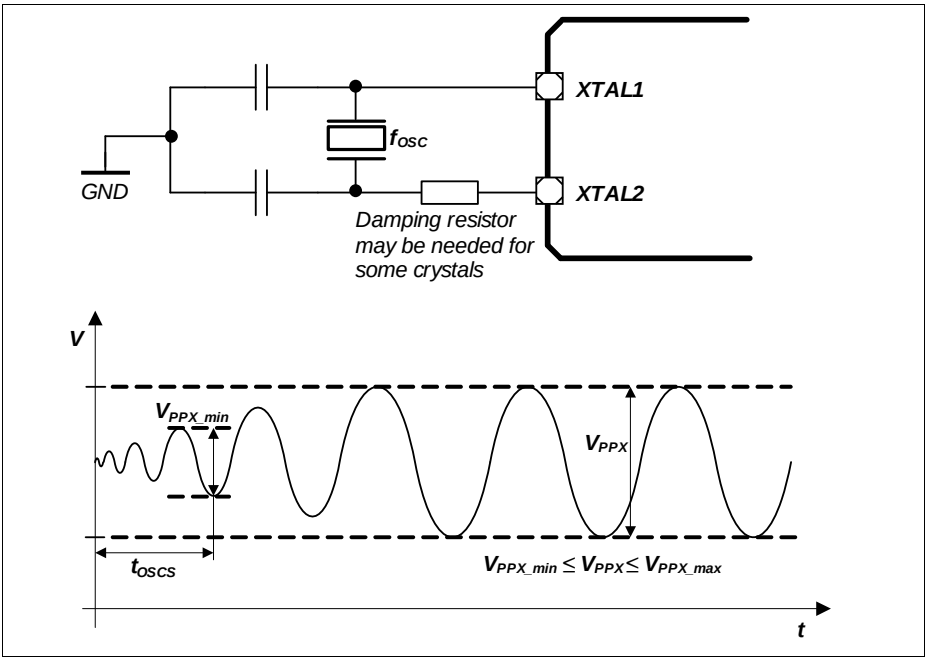

Figure 21 Oscillator in Crystal Mode

Table 38 Power Supply Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Power Dissipation	P_{DISS}	CC	–	–	1	W	V_{DDP} = 3.6 V, T_J = 150 °C
Wake-up time from Sleep to Active mode	t_{SSA}	CC	–	6	–	cycles	
Wake-up time from Deep Sleep to Active mode			–	–	–	ms	Defined by the wake-up of the Flash module, see **Section 3.2.11**
Wake-up time from Hibernate mode			–	–	–	ms	Wake-up via power-on reset event, see **Section 3.3.2**

1) CPU executing code from Flash, all peripherals idle.
2) CPU executing code from Flash. USB and CCU clock off.
3) CPU in sleep, all peripherals idle, Flash in Active mode.
4) CPU in sleep, Flash in Active mode.
5) CPU in sleep, peripherals disabled, after wake-up code execution from RAM.
6) To wake-up the Flash from its Sleep mode, $f_{CPU} \geq 1$ MHz is required.
7) OSC_ULP operating with external crystal on RTC_XTAL
8) OSC_ULP off, Hibernate domain operating with OSC_SI clock
9) Test Power Loop: f_{SYS} = 80 MHz, CPU executing benchmark code from Flash, all CCUs in 100kHz timer mode, all ADC groups in continuous conversion mode, USICs as SPI in internal loop-back mode, CAN in 500kHz internal loop-back mode, interrupt triggered DMA block transfers to parity protected RAMs and FCE, DTS measurements and FPU calculations.
   The power consumption of each customer application will most probably be lower than this value, but must be evaluated separately.
10) I_{DDP} decreases typically by 3.5 mA when f_{SYS} decreases by 10 MHz, at constant T_J
11) Sum of currents of all active converters (ADC and DAC)

2) Maximum threshold for reset deassertion.
3) The V_{DDP} monitoring has a typical hysteresis of V_{PORHYS} = 180 mV.

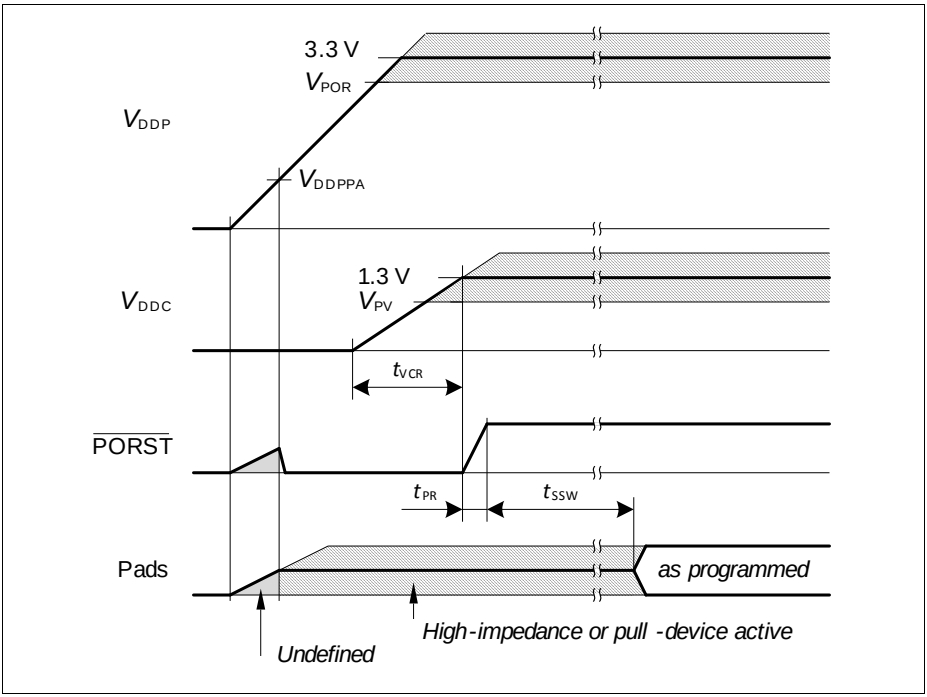

Figure 27 Power-Up Behavior

3.3.3 Power Sequencing

While starting up and shutting down as well as when switching power modes of the system it is important to limit the current load steps. A typical cause for such load steps is changing the CPU frequency f_{CPU}. Load steps exceeding the below defined values may cause a power on reset triggered by the supply monitor.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.7 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

Table 47 SWD Interface Timing Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SWDCLK clock period	t_{SC}	SR	25	–	–	ns	C_L = 30 pF
			40	–	–	ns	C_L = 50 pF
SWDCLK high time	t_1	SR	10	–	500000	ns	
SWDCLK low time	t_2	SR	10	–	500000	ns	
SWDIO input setup to SWDCLK rising edge	t_3	SR	6	–	–	ns	
SWDIO input hold after SWDCLK rising edge	t_4	SR	6	–	–	ns	
SWDIO output valid time after SWDCLK rising edge	t_5	CC	–	–	17	ns	C_L = 50 pF
			–	–	13	ns	C_L = 30 pF
SWDIO output hold time from SWDCLK rising edge	t_6	CC	3	–	–	ns	

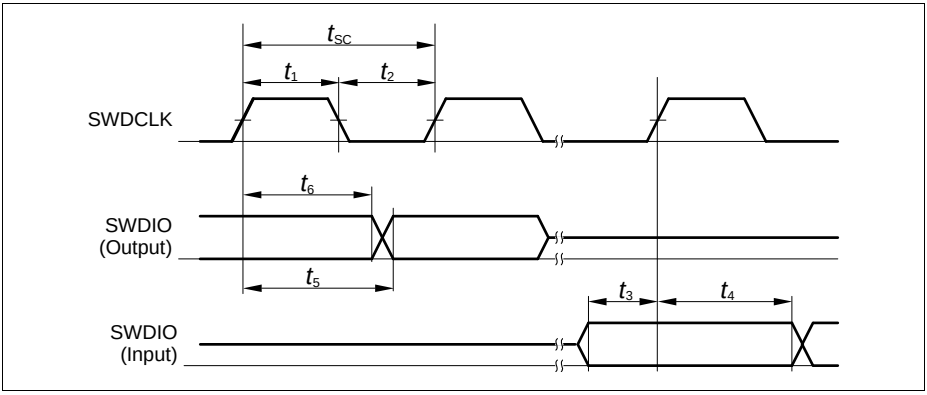

Figure 30 SWD Timing

Table 49 USIC SSC Slave Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DX1 slave clock period	t_{CLK}	SR	66.6	–	–	ns	
Select input DX2 setup to first clock input DX1 transmit edge[1]	t_{10}	SR	3	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1]	t_{11}	SR	4	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1]	t_{12}	SR	6	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1]	t_{13}	SR	4	–	–	ns	
Data output DOUT[3:0] valid time	t_{14}	CC	0	–	24	ns	

1) These input timing are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

4 Package and Reliability

The XMC4[12]00 is a member of the XMC4000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the Exposed Die Pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 55 provides the thermal characteristics of the packages used in XMC4[12]00. The availability of different packages for different markings is listed in **Table 2**.

Table 55 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad Dimensions	Ex × Ey CC	-	5.8 × 5.8	mm	PG-LQFP-64-19
		-	5.7 × 5.7	mm	PG-TQFP-64-19
		-	5.2 × 5.2	mm	PG-VQFN-48-53
		-	5.2 × 5.2	mm	PG-VQFN-48-71
Thermal resistance Junction-Ambient	$R_{\Theta JA}$ CC	-	30	K/W	PG-LQFP-64-19[1)]
		-	23.4	K/W	PG-TQFP-64-19[1)]
		-	34.8	K/W	PG-VQFN-48-53[1)] PG-VQFN-48-71[1)]

1) Device mounted on a 4-layer JEDEC board (JESD 51-7) with thermal vias; exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SS}, independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMC4[12]00 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The

power dissipation must be limited so that the average junction temperature does not exceed 150 °C.

The difference between junction temperature and ambient temperature is determined by
$\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

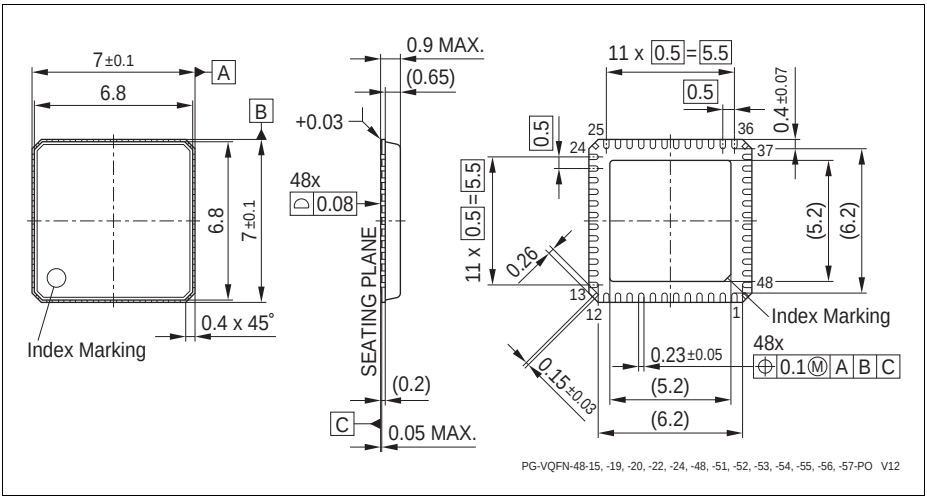

Figure 38 **PG-VQFN-48-53** (Plastic Green Very Thin Profile Flat Non Leaded Package)

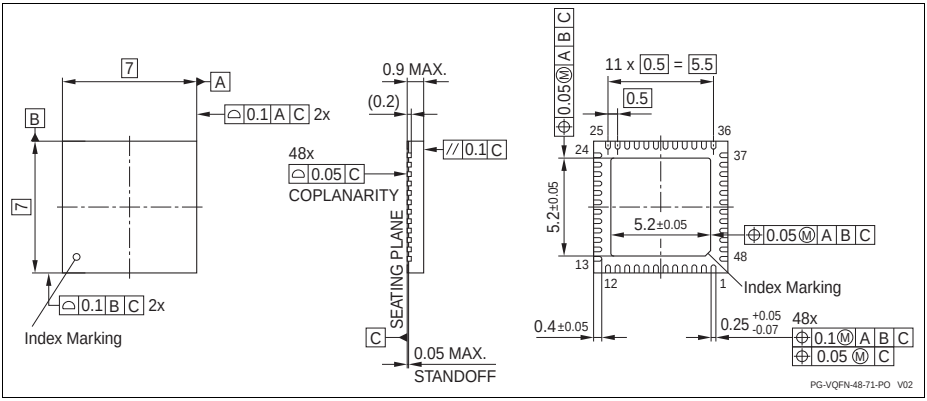

Figure 39 **PG-VQFN-48-71** (Plastic Green Very Thin Profile Flat Non Leaded Package)

All dimensions in mm.

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