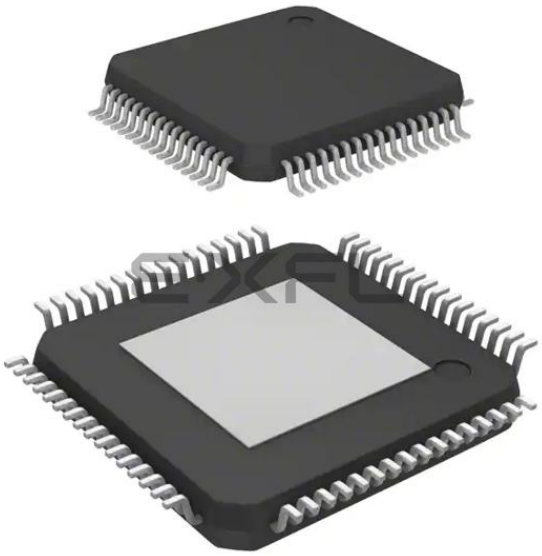
Infineon Technologies - XMC4200F64F256ABXQMA1 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-64-19
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4200f64f256abxqma1

1 Summary of Features

The XMC4[12]00 devices are members of the XMC4000 Family of microcontrollers based on the ARM Cortex-M4 processor core. The XMC4000 is a family of high performance and energy efficient microcontrollers optimized for Industrial Connectivity, Industrial Control, Power Conversion, Sense & Control.

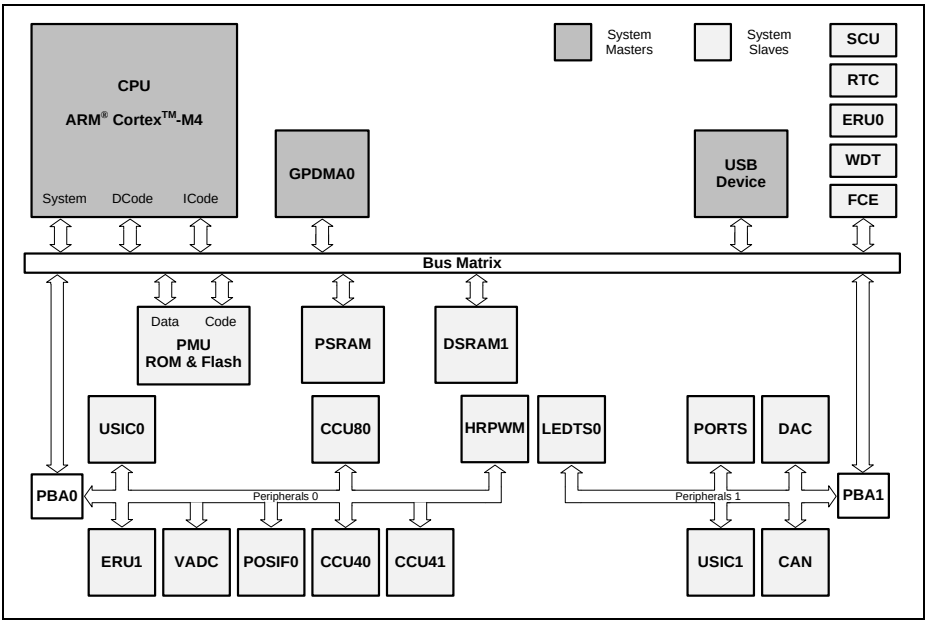

Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
  - High Performance 32-bit ARM Cortex-M4 CPU
  - 16-bit and 32-bit Thumb2 instruction set
  - DSP/MAC instructions
  - System timer (SysTick) for Operating System support
- Floating Point Unit
- Memory Protection Unit
- Nested Vectored Interrupt Controller
- One General Purpose DMA with up-to 8 channels
- Event Request Unit (ERU) for programmable processing of external and internal service requests
- Flexible CRC Engine (FCE) for multiple bit error detection

On-Chip Memories

- 16 KB on-chip boot ROM
- up to 16 KB on-chip high-speed program memory
- up to 24 KB on-chip high speed data memory
- up to 256 KB on-chip Flash Memory with 1 KB instruction cache

Communication Peripherals

- Universal Serial Bus, USB 2.0 device, with integrated PHY
- Controller Area Network interface (MultiCAN), Full-CAN/Basic-CAN with two nodes, 64 message objects (MO), data rate up to 1 MBit/s
- Four Universal Serial Interface Channels (USIC), providing four serial channels, usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- LED and Touch-Sense Controller (LEDTS) for Human-Machine interface

Analog Frontend Peripherals

- Two Analog-Digital Converters (VADC) of 12-bit resolution, 8 channels each, with input out-of-range comparators
- Digital-Analog Converter (DAC) with two channels of 12-bit resolution

Industrial Control Peripherals

- Two Capture/Compare Units 4 (CCU4) for use as general purpose timers
- One Capture/Compare Units 8 (CCU8) for motor control and power conversion
- Four High Resoultion PWM (HRPWM) channels
- One Position Interface (POSIF) for servo motor positioning
- Window Watchdog Timer (WDT) for safety sensitive applications
- Die Temperature Sensor (DTS)
- Real Time Clock module with alarm support
- System Control Unit (SCU) for system configuration and control

Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability
- Tri-stated in input mode
- Push/pull or open drain output mode
- Boundary scan test support over JTAG interface

On-Chip Debug Support

- Full support for debug features: 8 breakpoints, CoreSight, trace
- Various interfaces: ARM-JTAG, SWD, single wire trace

Table 9 XMC4100 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	0004 2001$_H$	EES-AA, ES-AA
SCU_IDCHIP	0004 2002$_H$	ES-AB, AB
SCU_IDCHIP	0004 1003$_H$	BA
JTAG IDCODE	101D D083$_H$	EES-AA, ES-AA
JTAG IDCODE	201D D083$_H$	ES-AB, AB
JTAG IDCODE	301D D083$_H$	BA

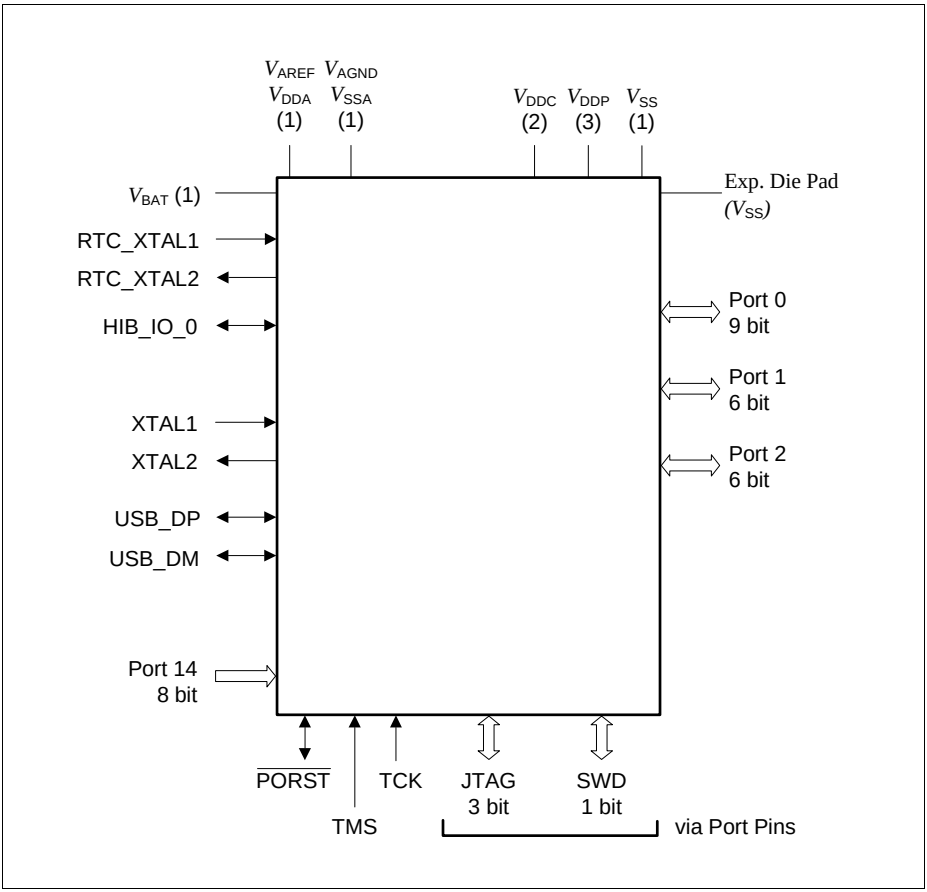

Figure 3 XMC4[12]00 Logic Symbol PG-VQFN-48

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

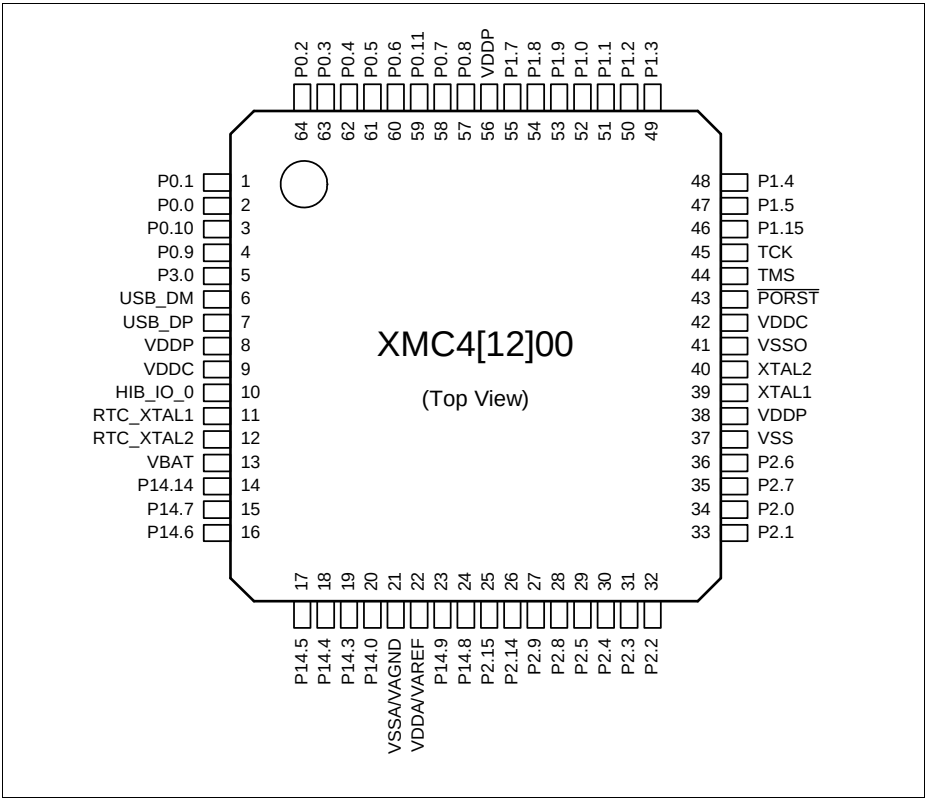

Figure 4 XMC4[12]00 PG-LQFP-64 and PG-TQFP-64 Pin Configuration (top view)

Table 11 Package Pin Mapping (cont'd)

Function	LQFP-64 TQFP-64	VQFN-48	Pad Type	Notes
VSSO	41	-	Power	
VSS	Exp. Pad	Exp. Pad	Power	**Exposed Die Pad** The exposed die pad is connected internally to VSS. For proper operation, it is mandatory to connect the exposed pad directly to the common ground on the board. For thermal aspects, please refer to the Data Sheet. Board layout examples are given in an application note.

3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 15 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
  - pad supply levels (V_{DDP} or V_{DDA})
  - temperature

If a pin current is outside of the **Operating Conditions** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

Table 15 Overload Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Input current on any port pin during overload condition	I_{OV}	SR	-5	–	5	mA	
Absolute sum of all input circuit currents for one port group during overload condition[1)]	I_{OVG}	SR	–	–	20	mA	$\Sigma\|I_{OVx}\|$, for all $I_{OVx} < 0$ mA
			–	–	20	mA	$\Sigma\|I_{OVx}\|$, for all $I_{OVx} > 0$ mA
Absolute sum of all input circuit currents during overload condition	I_{OVS}	SR	–	–	80	mA	ΣI_{OVG}

1) The port groups are defined in **Table 18**.

Figure 9 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

3.1.4 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in the **Section 3.2.1**.

Table 19 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub-Class	Speed Grade	Load	Termination
A	3.3 V	LVTTL I/O, LVTTL outputs	**A1** (e.g. GPIO)	6 MHz	100 pF	No
			A1+ (e.g. serial I/Os)	25 MHz	50 pF	Series termination recommended

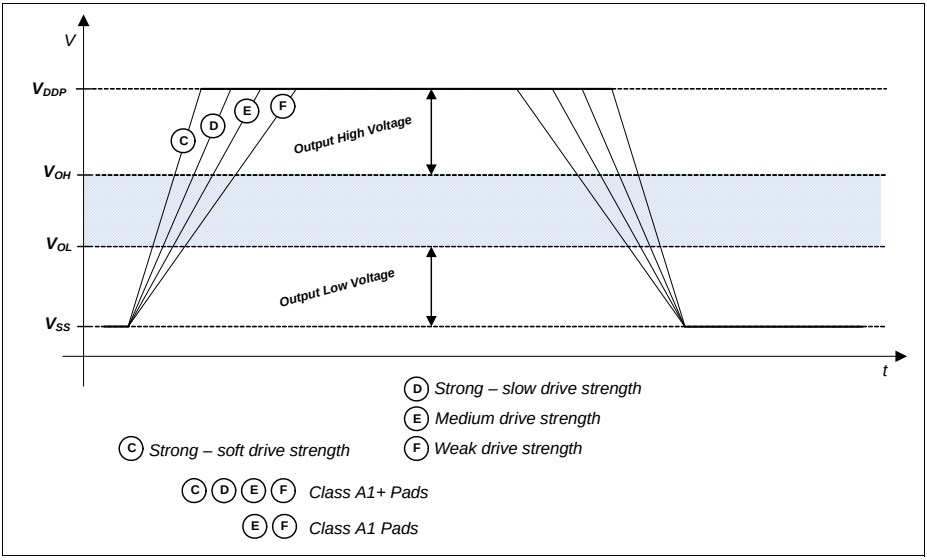

Figure 10 Output Slopes with different Pad Driver Modes

Figure 10 is a qualitative display of the resulting output slope performance with different output driver modes. The detailed input and output characteristics are listed in **Section 3.2.1**.

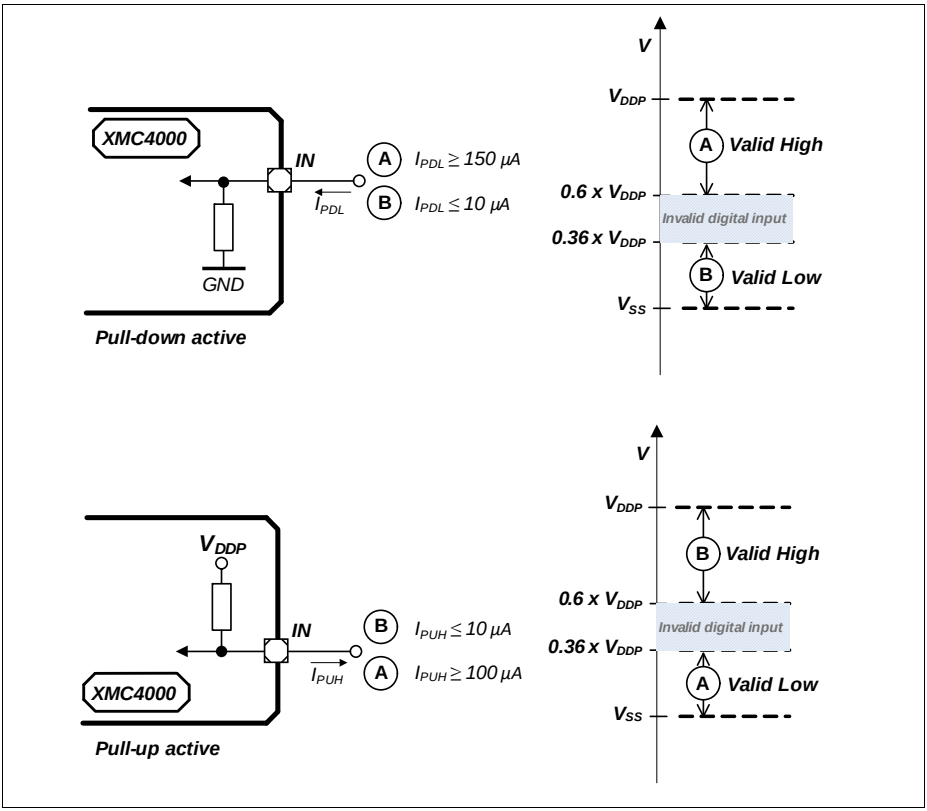

Figure 11 Pull Device Input Characteristics

Figure 11 visualizes the input characteristics with an active internal pull device:

- in the cases “A” the internal pull device is overridden by a strong external driver;
- in the cases “B” the internal pull device defines the input logical state against a weak external load.

Table 24 HIB_IO Class_A1 special Pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Input leakage current	I_{OZHIB} CC	-500		500	nA	$0\ V \le V_{IN} \le V_{BAT}$
Input high voltage	V_{IHHIB} SR	$0.6 \times V_{BAT}$		V_{BAT} + 0.3	V	max. 3.6 V
Input low voltage	V_{ILHIB} SR	-0.3		$0.36 \times V_{BAT}$	V	
Input Hysteresis for HIB_IO pins[1]	$HYSHIB$ CC	$0.1 \times V_{BAT}$		–	V	$V_{BAT} \ge 3.13$ V
		$0.06 \times V_{BAT}$		–	V	$V_{BAT} < 3.13$ V
Output high voltage, POD[1] = medium	V_{OHHIB} CC	V_{BAT} - 0.4		–	V	$I_{OH} \ge$ -1.4 mA
Output low voltage	V_{OLHIB} CC	–		0.4	V	$I_{OL} \le 2$ mA
Fall time	t_{FHIB} CC	–		50	ns	$V_{BAT} \ge 3.13$ V, $C_L = 50$ pF
		–		100	ns	$V_{BAT} < 3.13$ V, $C_L = 50$ pF
Rise time	t_{RHIB} CC	–		50	ns	$V_{BAT} \ge 3.13$ V, $C_L = 50$ pF
		–		100	ns	$V_{BAT} < 3.13$ V, $C_L = 50$ pF

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

9) The resulting current for a conversion can be calculated with $I_{AREF} = Q_{CONV} / t_c$.
The fastest 12-bit post-calibrated conversion of t_c = 566 ns results in a typical average current of I_{AREF} = 53 µA.

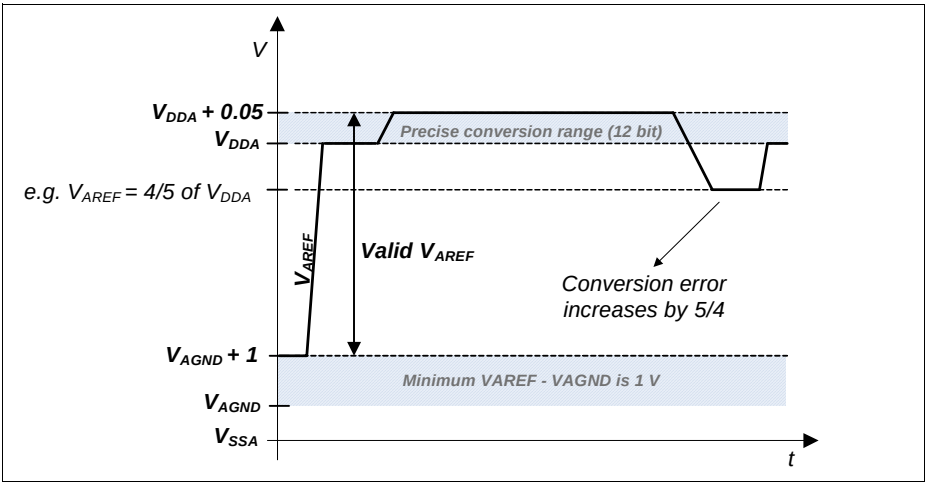

Figure 12 VADC Reference Voltage Range

Conversion Time

Table 26 Conversion Time (Operating Conditions apply)

Parameter	Symbol	Values	Unit	Note
Conversion time	t_C CC	$2 \times T_{ADC}$ + $(2 + N + STC + PC + DM) \times T_{ADCI}$	µs	N = 8, 10, 12 for N-bit conversion $T_{ADC} = 1 / f_{PERIPH}$ $T_{ADCI} = 1 / f_{ADCI}$

- STC defines additional clock cycles to extend the sample time
- PC adds two cycles if post-calibration is enabled
- DM adds one cycle for an extended conversion time of the MSB

Conversion Time Examples

System assumptions (max. f_{ADC}):
f_{ADC} = 80 MHz i.e. t_{ADC} = 12.5 ns, DIVA = 2, f_{ADCI} = 26.7 MHz i.e. t_{ADCI} = 37.5 ns
According to the given formulas the following minimum conversion times can be achieved (STC = 0, DM = 0):

12-bit post-calibrated conversion (PC = 2):
$t_{CN12C} = (2 + 12 + 2) \times t_{ADCI} + 2 \times t_{ADC} = 16 \times 37.5$ ns $+ 2 \times 12.5$ ns = 625 ns

12-bit uncalibrated conversion:
$t_{CN12} = (2 + 12) \times t_{ADCI} + 2 \times t_{ADC} = 14 \times 37.5$ ns $+ 2 \times 12.5$ ns = 550 ns

10-bit uncalibrated conversion:
$t_{CN10} = (2 + 10) \times t_{ADCI} + 2 \times t_{ADC} = 12 \times 37.5$ ns $+ 2 \times 12.5$ ns = 475 ns

8-bit uncalibrated:
$t_{CN8} = (2 + 8) \times t_{ADCI} + 2 \times t_{ADC} = 10 \times 37.5$ ns $+ 2 \times 12.5$ ns = 400 ns

System assumptions (max. f_{ADCI}):
f_{ADC} = 60 MHz i.e. t_{ADC} = 16.67 ns, DIVA = 1, f_{ADCI} = 30 MHz i.e. t_{ADCI} = 33.33 ns

12-bit post-calibrated conversion (PC = 2):
$t_{CN12C} = (2 + 12 + 2) \times t_{ADCI} + 2 \times t_{ADC} = 16 \times 33.33$ ns $+ 2 \times 16.67$ ns = 566 ns

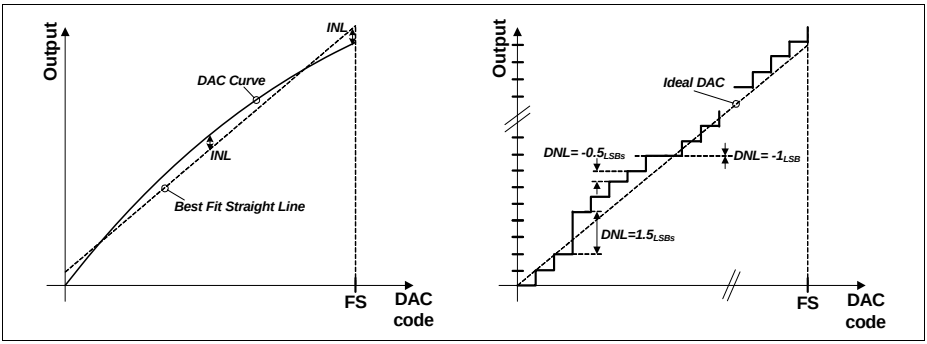

Figure 18 CSG DAC INL and DNL example

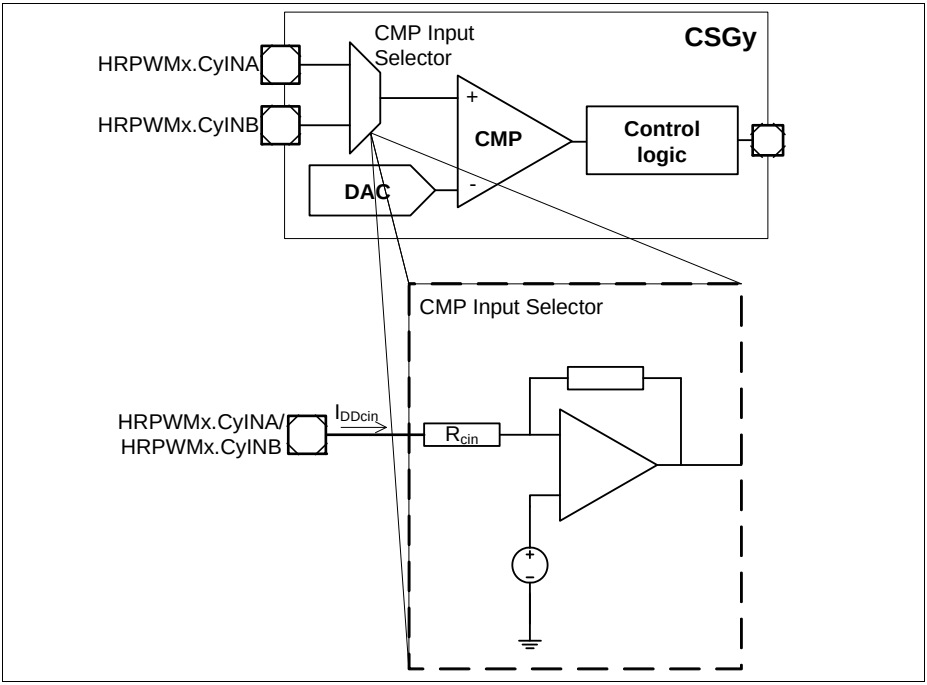

Figure 19 Input operation current

Table 38 Power Supply Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sleep supply current[3] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS} CC	–	76	–	mA	80 / 80 / 80
		–	73	–		80 / 40 / 40
		–	70	–		40 / 40 / 80
		–	56	–		24 / 24 / 24
		–	47	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	46	–		100 / 100 / 100
Sleep supply current[4] Peripherals disabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS} CC	–	59	–	mA	80 / 80 / 80
		–	58	–		80 / 40 / 40
		–	57	–		40 / 40 / 80
		–	51	–		24 / 24 / 24
		–	46	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	46	–		100 / 100 / 100
Deep Sleep supply current[5] Flash in Sleep mode Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPD} CC	–	6.9	–	mA	24 / 24 / 24
		–	4.3	–		4 / 4 / 4
		–	3.8	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	4.5	–		100 / 100 / 100 [6]
Hibernate supply current RTC on[7]	I_{DDPH} CC	–	10.8	–	µA	V_{BAT} = 3.3 V
		–	8.0	–		V_{BAT} = 2.4 V
		–	6.8	–		V_{BAT} = 2.0 V
Hibernate supply current RTC off[8]	I_{DDPH} CC	–	10.3	–	µA	V_{BAT} = 3.3 V
		–	7.5	–		V_{BAT} = 2.4 V
		–	6.3	–		V_{BAT} = 2.0 V
Worst case active supply current[9]	I_{DDPA} CC	–	–	140 [10]	mA	V_{DDP} = 3.6 V, T_J = 150 °C
V_{DDA} power supply current	I_{DDA} CC	–	–	–[11]	mA	
I_{DDP} current at $\overline{\text{PORST}}$ Low	I_{DDP_PORST} CC	–	–	24	mA	V_{DDP} = 3.6 V, T_J = 150 °C

Table 40 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data Retention Time, User Configuration Block (UCB)[3)4)]	t_{RTU} CC	20	–	–	years	Max. 4 erase/program cycles per UCB
Endurance on 64 Kbyte Physical Sector PS4	N_{EPS4} CC	10000	–	–	cycles	BA-marking devices only! Cycling distributed over life time[5)]

1) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes an additional time of 5.5 ms.

2) The following formula applies to the wait state configuration: FCON.WSPFLASH × (1 / f_{CPU}) ≥ t_a.

3) Storage and inactive time included.

4) Values given are valid for an average weighted junction temperature of T_J = 110°C.

5) Only valid with robust EEPROM emulation algorithm, equally cycling the logical sectors. For more details see the Reference Manual.

Table 42 Power Sequencing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Positive Load Step Current	ΔI_{PLS} SR	-	–	50	mA	Load increase on V_{DDP} $\Delta t \leq 10$ ns
Negative Load Step Current	ΔI_{NLS} SR	-	–	150	mA	Load decrease on V_{DDP} $\Delta t \leq 10$ ns
V_{DDC} Voltage Over- / Undershoot from Load Step	ΔV_{LS} CC	-	–	±100	mV	For maximum positive or negative load step
Positive Load Step Settling Time	t_{PLSS} SR	50	–	-	µs	
Negative Load Step Settling Time	t_{NLSS} SR	100	–	-	µs	
External Buffer Capacitor on V_{DDC}	C_{EXT} SR	3	4.7	6	µF	In addition C = 100 nF capacitor on each V_{DDC} pin

Positive Load Step Examples

System assumptions:
$f_{CPU} = f_{SYS}$, target frequency f_{CPU} = 80 MHz, main PLL f_{VCO} = 480 MHz, stepping done by K2 divider, t_{PLSS} between individual steps:

24 MHz - 48 MHz - 80 MHz (K2 steps 20 - 10 - 6)
24 MHz - 60 MHz - 80 MHz (K2 steps 20 - 8 - 6)

3.3.5 Internal Clock Source Characteristics

Fast Internal Clock Source

Table 44 Fast Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal frequency	f_{OFINC} CC	–	36.5	–	MHz	not calibrated
		–	24	–	MHz	calibrated
Accuracy	Δf_{OFI} CC	-0.5	–	0.5	%	automatic calibration[1)2)]
		-15	–	15	%	factory calibration, V_{DDP} = 3.3 V
		-25	–	25	%	no calibration, V_{DDP} = 3.3 V
		-7	–	7	%	Variation over voltage range[3)] 3.13 V ≤ V_{DDP} ≤ 3.63 V
Start-up time	t_{OFIS} CC	–	50	–	µs	

1) Error in addition to the accuracy of the reference clock.

2) Automatic calibration compensates variations of the temperature and in the V_{DDP} supply voltage.

3) Deviations from the nominal V_{DDP} voltage induce an additional error to the uncalibrated and/or factory calibrated oscillator frequency.

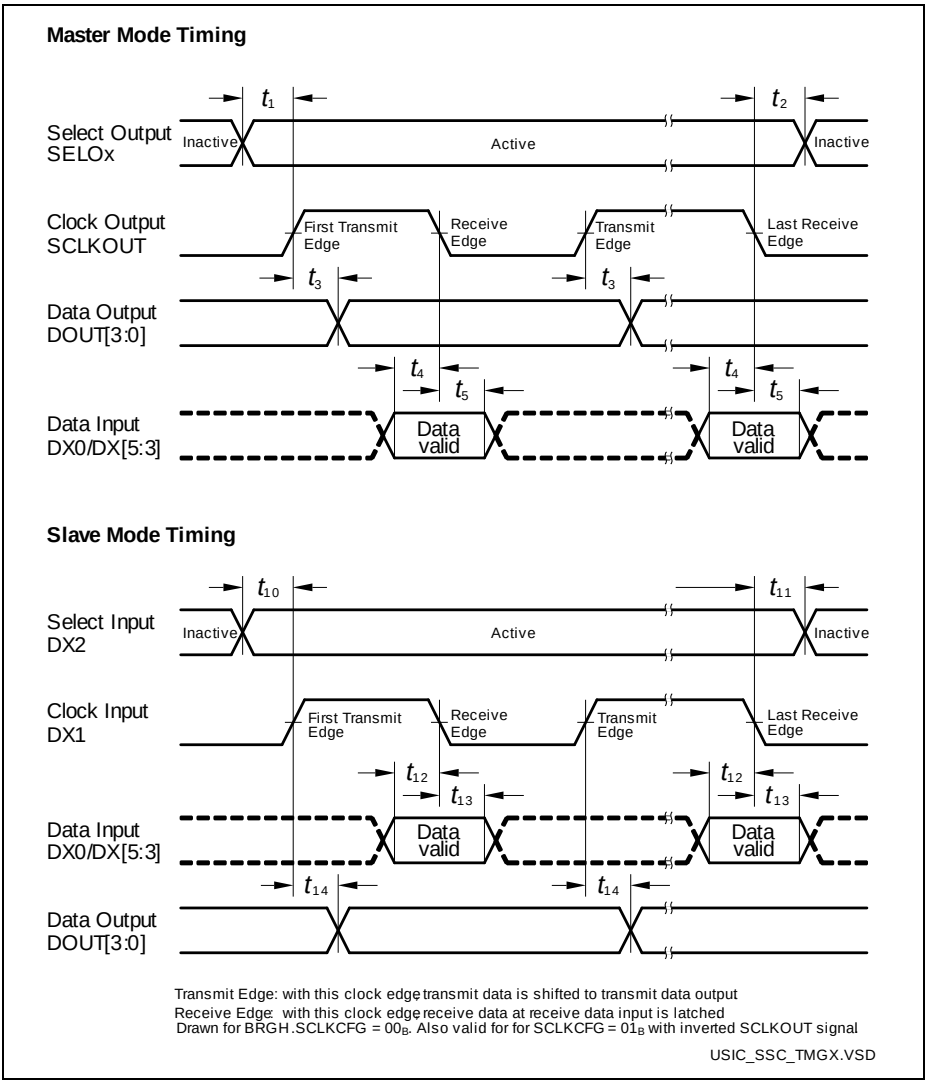

Figure 31 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.

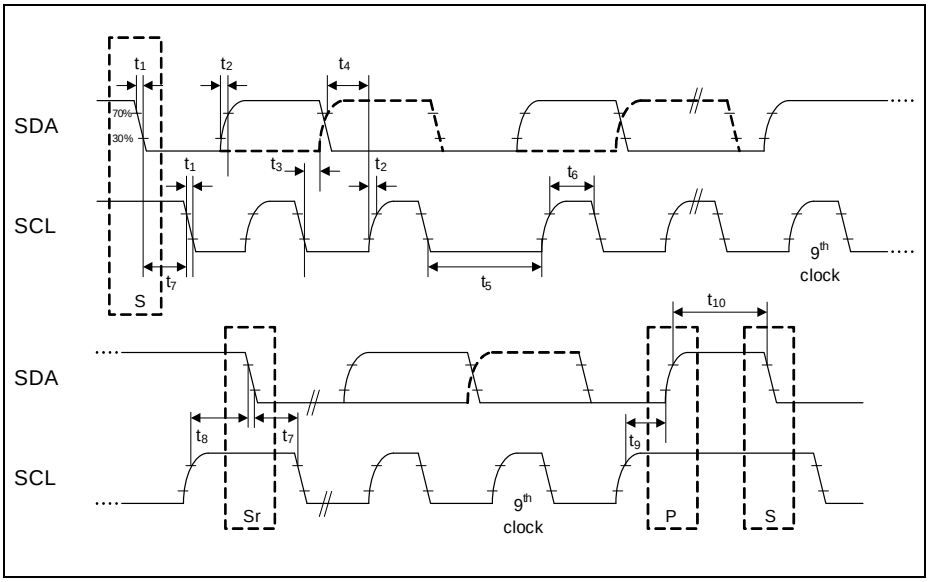

Figure 32 USIC IIC Stand and Fast Mode Timing

3.3.8.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

Note: Operating Conditions apply.

Table 52 USIC IIS Master Transmitter Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_1 CC	33.3	–	–	ns	
Clock high time	t_2 CC	0.35 x t_{1min}	–	–	ns	
Clock low time	t_3 CC	0.35 x t_{1min}	–	–	ns	
Hold time	t_4 CC	0	–	–	ns	
Clock rise time	t_5 CC	–	–	0.15 x t_{1min}	ns	

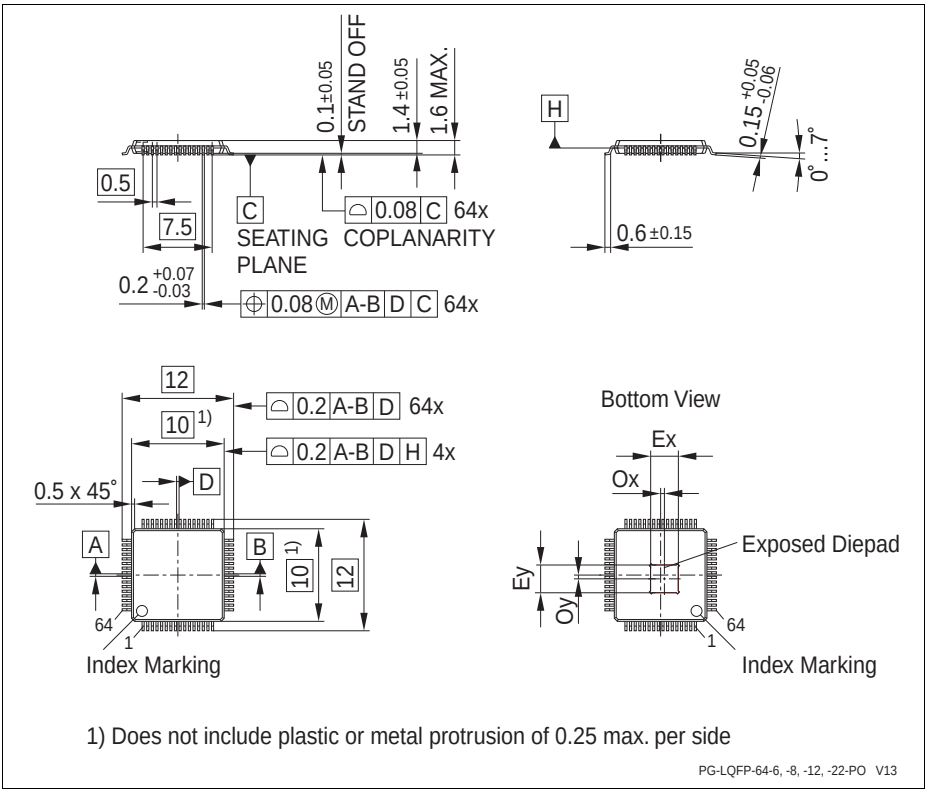

Figure 36 **PG-LQFP-64-19** (Plastic Green Low Profile Quad Flat Package)