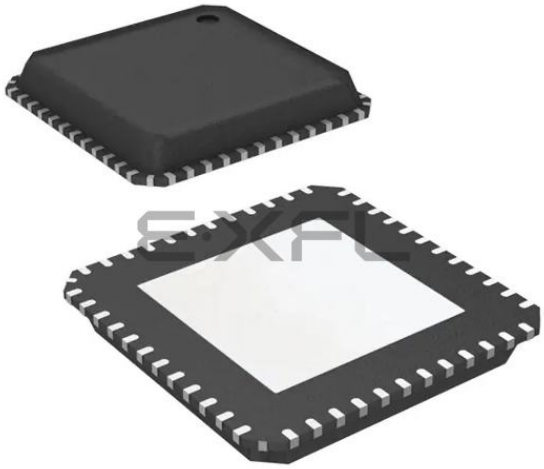
Infineon Technologies - XMC4200Q48F256ABXUMA1 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	21
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-53
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4200q48f256abxuma1

Edition 2015-10

Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

XMC4100 / XMC4200

Microcontroller Series
for Industrial Applications

XMC4000 Family

ARM® Cortex®-M4
32-bit processor core

Data Sheet

V1.3 2015-10

Microcontrollers

XMC4[12]00 Data Sheet

Revision History: V1.3 2015-10

Previous Versions:
V1.2 2014-06
V1.1 2014-03
V1.0 2013-10
V0.6 2012-11

Page	Subjects
12	Added a section listing the packages of the different markings.
14	Added BA marking variant.
14	Corrected SCU_IDCHIP value of XMC4100 EES-AA/ES-AA.
36	Added footnote explaining minimum V_{BAT} requirements to start the hibernate domain and/or oscillation of a crystal on RTC_XTAL.
37	Changed pull device definition to System Requirement (SR) to reflect that the specified currents are defined by the characteristics of the external load/driver.
37	Added information that $\overline{\text{PORST}}$ Pull-up is identical to the pull-up on standard I/O pins.
42	Updated C_{AINSW}, C_{AINTOT} and R_{AIN} parameters with improved values.
56	Added footnote on test configuration for LPAC measurement.
58	Corrected parameter name of of USB pull device (upstream port receiving) definition according to USB standard (referenced to DM instead of DP)
62	Relaxed RTC_XTAL V_{PPX} parameter value and changed it to a system requirement.
66	Added footnote on current consumption by enabling of f_{CCU}.
67	Added Flash endurance parameter for 64 Kbytes Physical Sector PS4 N_{EPS4} for devices with BA marking.
many	Added PG-TQFP-64-19 and PG-VQFN-48-71 package information.
89, 91	Added tables describing the differences between PG-LQFP-64-19 to PG-TQFP-64-19 as well as PG-VQFN-48-53 to PG-VQFN-48-71 packages.
93	Updated to JEDEC standard J-STD-020D for the moisture sensitivity level and added solder temperature parameter according to the same standard.

1 Summary of Features

The XMC4[12]00 devices are members of the XMC4000 Family of microcontrollers based on the ARM Cortex-M4 processor core. The XMC4000 is a family of high performance and energy efficient microcontrollers optimized for Industrial Connectivity, Industrial Control, Power Conversion, Sense & Control.

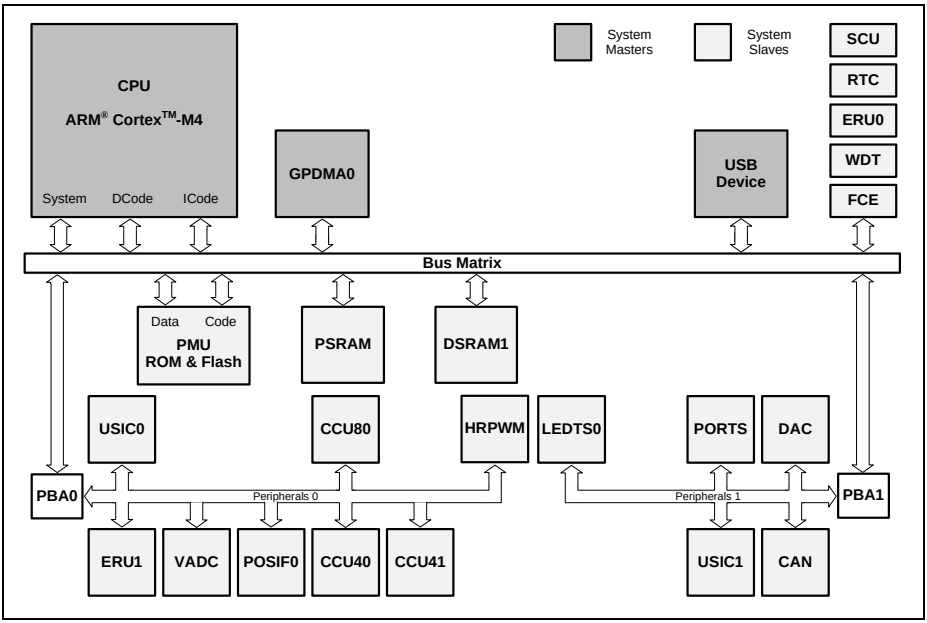


Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
  - High Performance 32-bit ARM Cortex-M4 CPU
  - 16-bit and 32-bit Thumb2 instruction set
  - DSP/MAC instructions
  - System timer (SysTick) for Operating System support
- Floating Point Unit
- Memory Protection Unit
- Nested Vectored Interrupt Controller
- One General Purpose DMA with up-to 8 channels
- Event Request Unit (ERU) for programmable processing of external and internal service requests
- Flexible CRC Engine (FCE) for multiple bit error detection

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

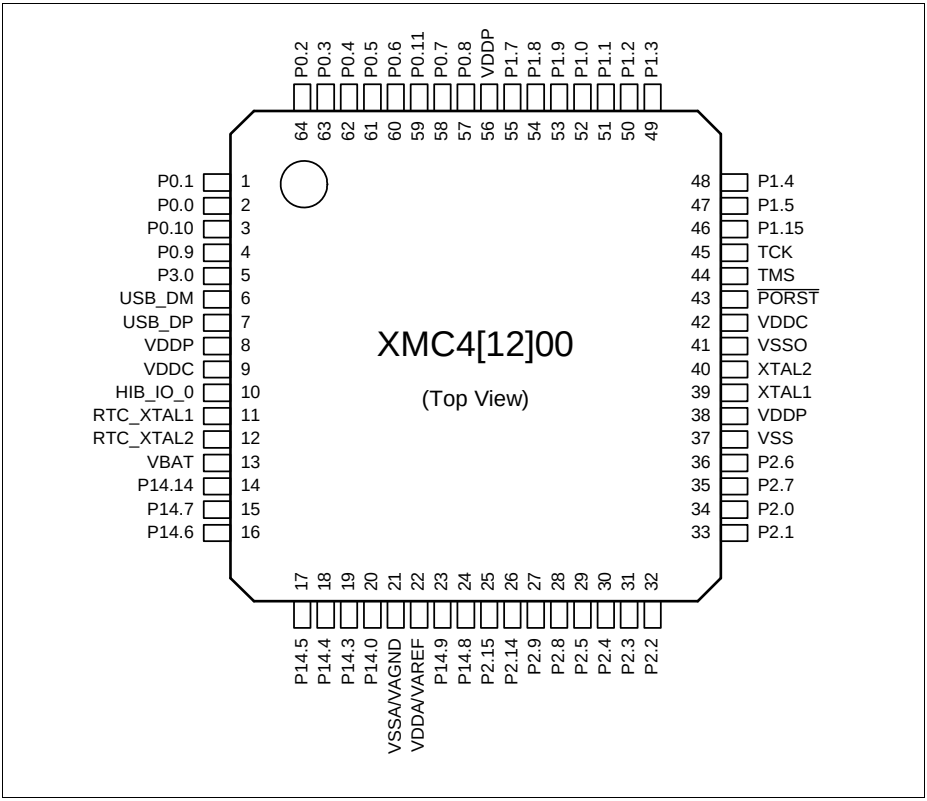


Figure 4 XMC4[12]00 PG-LQFP-64 and PG-TQFP-64 Pin Configuration (top view)

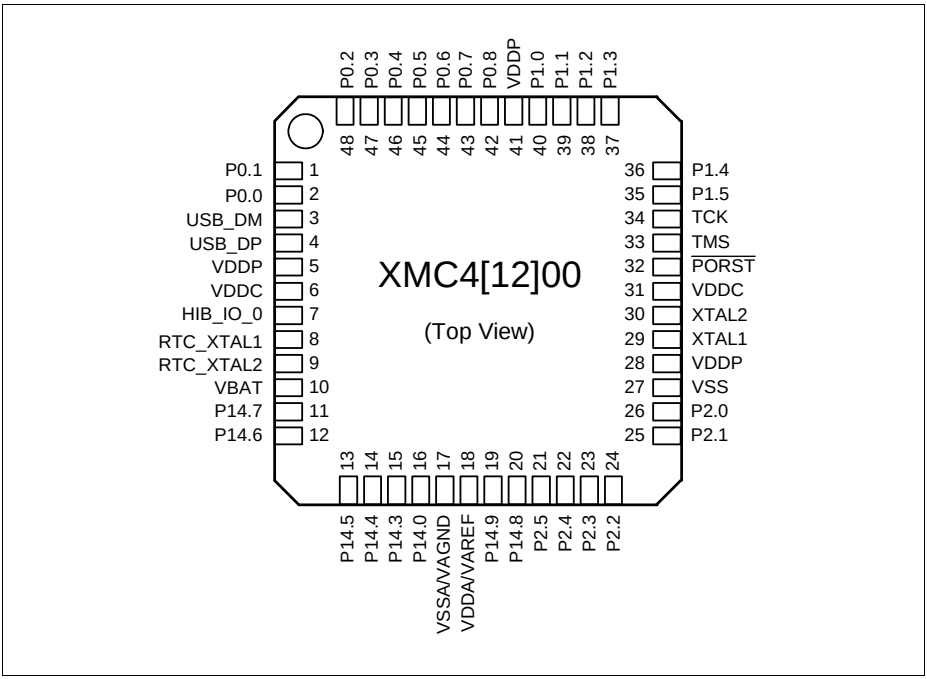


Figure 5 XMC4[12]00 PG-VQFN-48 Pin Configuration (top view)

Table 11 Package Pin Mapping (cont'd)

Function	LQFP-64 TQFP-64	VQFN-48	Pad Type	Notes
P14.9	23	19	AN/DAC/DIG_IN	
P14.14	14	-	AN/DIG_IN	
USB_DP	7	4	special	
USB_DM	6	3	special	
HIB_IO_0	10	7	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as open-drain output and drives "0". As output the medium driver mode is active.
TCK	45	34	A1	Weak pull-down active.
TMS	44	33	A1+	Weak pull-up active. As output the strong-soft driver mode is active.
$\overline{\text{PORST}}$	43	32	special	Strong pull-down controlled by EVR. Weak pull-up active while strong pull-down is not active.
XTAL1	39	29	clock_IN	
XTAL2	40	30	clock_O	
RTC_XTAL1	11	8	clock_IN	
RTC_XTAL2	12	9	clock_O	
VBAT	13	10	Power	When VDDP is supplied VBAT has to be supplied as well.
VDDA/VAREF	22	18	AN_Power/AN_ Ref	Shared analog supply and reference voltage pin.
VSSA/VAGND	21	17	AN_Power/AN_ Ref	Shared analog supply and reference ground pin.
VDDC	9	6	Power	
VDDC	42	31	Power	
VDDP	8	5	Power	
VDDP	38	28	Power	
VDDP	56	41	Power	
VSS	37	27	Power	

3 Electrical Parameters

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the XMC4[12]00 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are a distinctive feature of the XMC4[12]00 and must be regarded for system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC4[12]00 is designed in.

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 14 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Storage temperature	T_{ST}	SR	-65	–	150	°C	–
Junction temperature	T_J	SR	-40	–	150	°C	–
Voltage at 3.3 V power supply pins with respect to V_{SS}	V_{DDP}	SR	–	–	4.3	V	–
Voltage on any Class A and dedicated input pin with respect to V_{SS}	V_{IN}	SR	-1.0	–	V_{DDP} + 1.0 or max. 4.3	V	whichever is lower
Voltage on any analog input pin with respect to V_{AGND}	V_{AIN} V_{AREF}	SR	-1.0	–	V_{DDP} + 1.0 or max. 4.3	V	whichever is lower
Input current on any pin during overload condition	I_{IN}	SR	-10	–	+10	mA	
Absolute maximum sum of all input circuit currents for one port group during overload condition[1)]	ΣI_{IN}	SR	-25	–	+25	mA	
Absolute maximum sum of all input circuit currents during overload condition	ΣI_{IN}	SR	-100	–	+100	mA	

1) The port groups are defined in **Table 18**.

3.1.4 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in the **Section 3.2.1**.

Table 19 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub-Class	Speed Grade	Load	Termination
A	3.3 V	LVTTL I/O, LVTTL outputs	**A1** (e.g. GPIO)	6 MHz	100 pF	No
			A1+ (e.g. serial I/Os)	25 MHz	50 pF	Series termination recommended

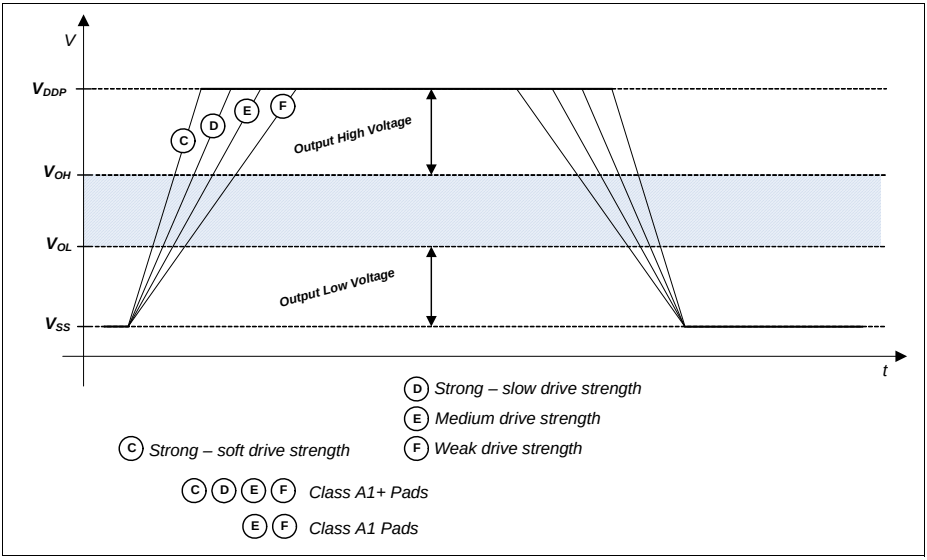


Figure 10 Output Slopes with different Pad Driver Modes

Figure 10 is a qualitative display of the resulting output slope performance with different output driver modes. The detailed input and output characteristics are listed in **Section 3.2.1**.

Table 23 Standard Pads Class_A1+

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Output high voltage, POD[1] = weak	V_{OHA1+} CC	V_{DDP} - 0.4		–	V	$I_{OH} \geq$ -400 µA
		2.4		–	V	$I_{OH} \geq$ -500 µA
Output high voltage, POD[1] = medium		V_{DDP} - 0.4		–	V	$I_{OH} \geq$ -1.4 mA
		2.4		–	V	$I_{OH} \geq$ -2 mA
Output high voltage, POD[1] = strong		V_{DDP} - 0.4		–	V	$I_{OH} \geq$ -1.4 mA
		2.4		–	V	$I_{OH} \geq$ -2 mA
Output low voltage	V_{OLA1+} CC	–		0.4	V	$I_{OL} \leq$ 500 µA; POD[1] = weak
		–		0.4	V	$I_{OL} \leq$ 2 mA; POD[1] = medium
		–		0.4	V	$I_{OL} \leq$ 2 mA; POD[1] = strong
Fall time	t_{FA1+} CC	–		150	ns	C_L = 20 pF; POD[1] = weak
		–		50	ns	C_L = 50 pF; POD[1] = medium
		–		28	ns	C_L = 50 pF; POD[1] = strong; edge = slow
		–		16	ns	C_L = 50 pF; POD[1] = strong; edge = soft;
Rise time	t_{RA1+} CC	–		150	ns	C_L = 20 pF; POD[1] = weak
		–		50	ns	C_L = 50 pF; POD[1] = medium
		–		28	ns	C_L = 50 pF; POD[1] = strong; edge = slow
		–		16	ns	C_L = 50 pF; POD[1] = strong; edge = soft

1) POD = Pin Out Driver

Table 25 ADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Total capacitance of the alternate reference inputs[5]	$C_{AREFTOT}$ CC	–	20	40	pF	
Total Unadjusted Error	TUE CC	-6	–	6	LSB	12-bit resolution; V_{DDA} = 3.3 V; $V_{AREF} = V_{DDA}$[7]
Differential Non-Linearity Error[8]	EA_{DNL} CC	-4.5	–	4.5	LSB	
Gain Error[8]	EA_{GAIN} CC	-6	–	6	LSB	
Integral Non-Linearity[8]	EA_{INL}CC	-4.5	–	4.5	LSB	
Offset Error[8]	EA_{OFF} CC	-6	–	6	LSB	
Worst case ADC V_{DDA} power supply current per active converter	I_{DDAA} CC	–	1.5	2	mA	during conversion V_{DDP} = 3.6 V, T_J = 150 °C
Charge consumption on alternate reference per conversion[5]	Q_{CONV} CC	–	30	–	pC	0 V ≤ V_{AREF} ≤ V_{DDA}[9]
ON resistance of the analog input path	R_{AIN} CC	–	600	1 200	Ohm	
ON resistance for the ADC test (pull down for AIN7)	R_{AIN7T} CC	180	550	900	Ohm	

1) A running conversion may become imprecise in case the normal conditions are violated (voltage overshoot).
2) If the analog reference voltage is below V_{DDA}, then the ADC converter errors increase. If the reference voltage is reduced by the factor k (k<1), TUE, DNL, INL, Gain, and Offset errors increase also by the factor 1/k.
3) The leakage current definition is a continuous function, as shown in figure ADCx Analog Inputs Leakage. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function (see **Figure 14**).
4) The sampling capacity of the conversion C-network is pre-charged to V_{AREF}/2 before the sampling moment. Because of the parasitic elements, the voltage measured at AINx can deviate from V_{AREF}/2.
5) Applies to AINx, when used as alternate reference input.
6) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead, smaller capacitances are successively switched to the reference voltage.
7) For 10-bit conversions, the errors are reduced to 1/4; for 8-bit conversions, the errors are reduced to 1/16. Never less than ±1 LSB.
8) The sum of DNL/INL/GAIN/OFF errors does not exceed the related total unadjusted error TUE.

Table 27 DAC Parameters (Operating Conditions apply) (cont'd)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Offset error	ED_{OFF}	CC		±20		mV	
Gain error	ED_{G_IN}	CC	-5	0	5	%	
Startup time	$t_{STARTUP}$	CC	–	15	30	µs	time from output enabling till code valid ±16 LSB
3dB Bandwidth of Output Buffer	f_{C1}	CC	2.5	5	–	MHz	verified by design
Output sourcing current	I_{OUT_SOURCE}	CC	–	-30	–	mA	
Output sinking current	I_{OUT_SINK}	CC	–	0.6	–	mA	
Output resistance	R_{OUT}	CC	–	50	–	Ohm	
Load resistance	R_L	SR	5	–	–	kOhm	
Load capacitance	C_L	SR	–	–	50	pF	
Signal-to-Noise Ratio	*SNR*	CC	–	70	–	dB	examination bandwidth < 25 kHz
Total Harmonic Distortion	*THD*	CC	–	70	–	dB	examination bandwidth < 25 kHz
Power Supply Rejection Ratio	*PSRR*	CC	–	56	–	dB	to V_{DDA} verified by design

1) According to best straight line method.

Conversion Calculation

Unsigned:
DACxDATA = 4095 × (V_{OUT} - V_{OUT_MIN}) / (V_{OUT_MAX} - V_{OUT_MIN})
Signed:
DACxDATA = 4095 × (V_{OUT} - V_{OUT_MIN}) / (V_{OUT_MAX} - V_{OUT_MIN}) - 2048

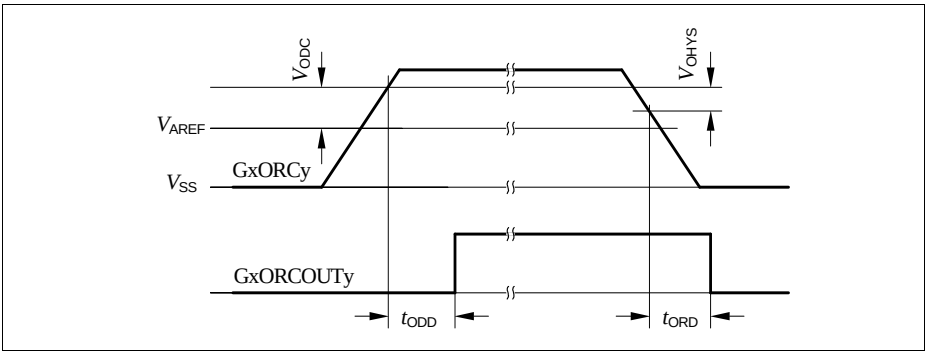


Figure 16 GxORCOUTy Trigger Generation

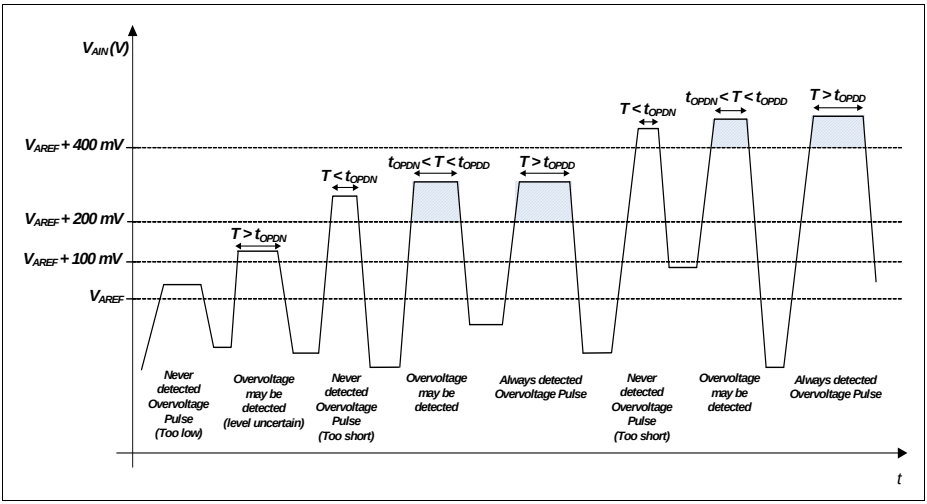


Figure 17 ORC Detection Ranges

3.2.10 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

If not stated otherwise, the operating conditions for the parameters in the following table are:
V_{DDP} = 3.3 V, T_A = 25 °C

Table 38 Power Supply Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Active supply current[1] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPA}	CC	–	80	–	mA	80 / 80 / 80
			–	75	–		80 / 40 / 40
			–	73	–		40 / 40 / 80
			–	59	–		24 / 24 / 24
			–	50	–		1 / 1 / 1
Active supply current Code execution from RAM Flash in Sleep mode Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPA}	CC	–	24	–	mA	80 / 80 / 80
			–	19	–		80 / 40 / 40
Active supply current[2] Peripherals disabled Frequency: f_{CPU} / f_{PERIPH} in MHz	I_{DDPA}	CC	–	63	–	mA	80 / 80 / 80
			–	62	–		80 / 40 / 40
			–	60	–		40 / 40 / 80
			–	54	–		24 / 24 / 24
			–	50	–		1 / 1 / 1

Table 38 Power Supply Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Power Dissipation	P_{DISS}	CC	–	–	1	W	V_{DDP} = 3.6 V, T_J = 150 °C
Wake-up time from Sleep to Active mode	t_{SSA}	CC	–	6	–	cycles	
Wake-up time from Deep Sleep to Active mode			–	–	–	ms	Defined by the wake-up of the Flash module, see **Section 3.2.11**
Wake-up time from Hibernate mode			–	–	–	ms	Wake-up via power-on reset event, see **Section 3.3.2**

1) CPU executing code from Flash, all peripherals idle.
2) CPU executing code from Flash. USB and CCU clock off.
3) CPU in sleep, all peripherals idle, Flash in Active mode.
4) CPU in sleep, Flash in Active mode.
5) CPU in sleep, peripherals disabled, after wake-up code execution from RAM.
6) To wake-up the Flash from its Sleep mode, $f_{CPU} \geq 1$ MHz is required.
7) OSC_ULP operating with external crystal on RTC_XTAL
8) OSC_ULP off, Hibernate domain operating with OSC_SI clock
9) Test Power Loop: f_{SYS} = 80 MHz, CPU executing benchmark code from Flash, all CCUs in 100kHz timer mode, all ADC groups in continuous conversion mode, USICs as SPI in internal loop-back mode, CAN in 500kHz internal loop-back mode, interrupt triggered DMA block transfers to parity protected RAMs and FCE, DTS measurements and FPU calculations.
   The power consumption of each customer application will most probably be lower than this value, but must be evaluated separately.
10) I_{DDP} decreases typically by 3.5 mA when f_{SYS} decreases by 10 MHz, at constant T_J
11) Sum of currents of all active converters (ADC and DAC)

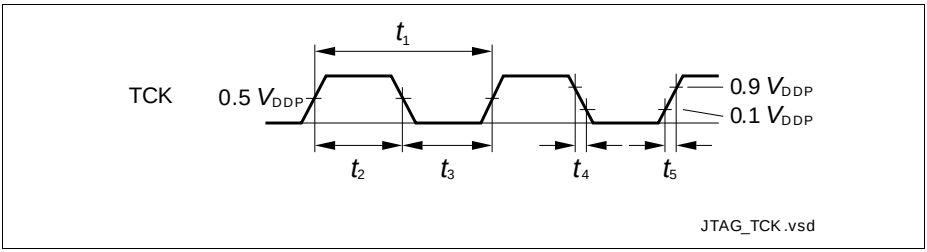


Figure 28 Test Clock Timing (TCK)

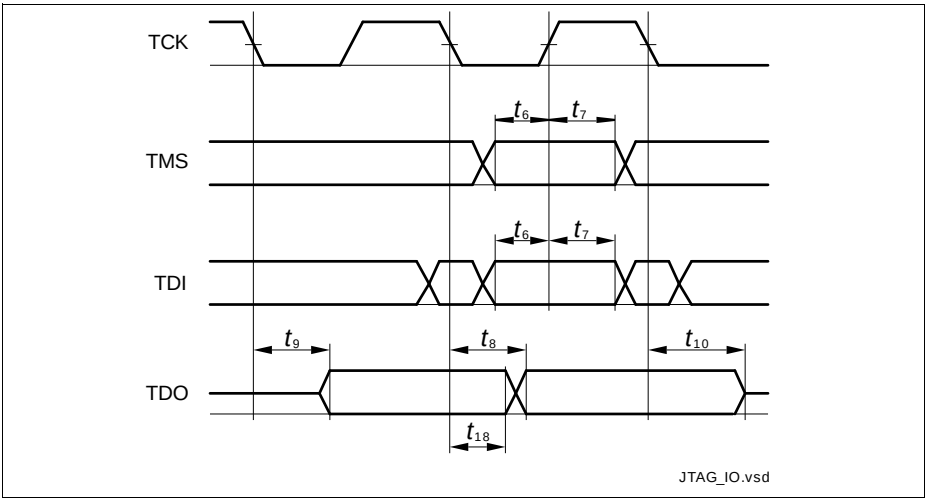


Figure 29 JTAG Timing

3.3.8.2 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: Operating Conditions apply.

Table 50 USIC IIC Standard Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

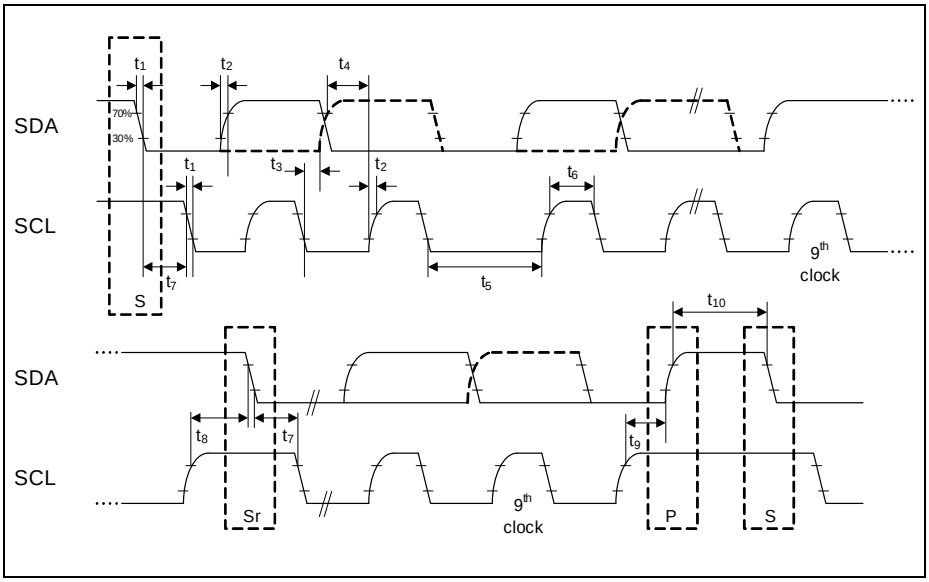


Figure 32 USIC IIC Stand and Fast Mode Timing

3.3.8.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

Note: Operating Conditions apply.

Table 52 USIC IIS Master Transmitter Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_1 CC	33.3	–	–	ns	
Clock high time	t_2 CC	0.35 x t_{1min}	–	–	ns	
Clock low time	t_3 CC	0.35 x t_{1min}	–	–	ns	
Hold time	t_4 CC	0	–	–	ns	
Clock rise time	t_5 CC	–	–	0.15 x t_{1min}	ns	

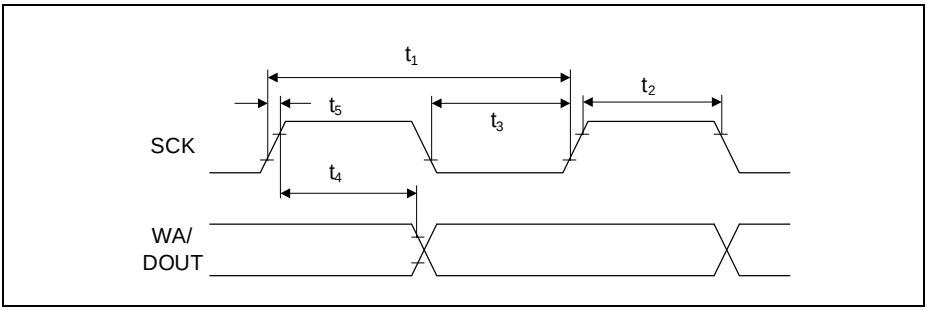


Figure 33 USIC IIS Master Transmitter Timing

Table 53 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	66.6	–	–	ns	
Clock high time	t_7 SR	0.35 x t_{6min}	–	–	ns	
Clock low time	t_8 SR	0.35 x t_{6min}	–	–	ns	
Set-up time	t_9 SR	0.2 x t_{6min}	–	–	ns	
Hold time	t_{10} SR	0	–	–	ns	

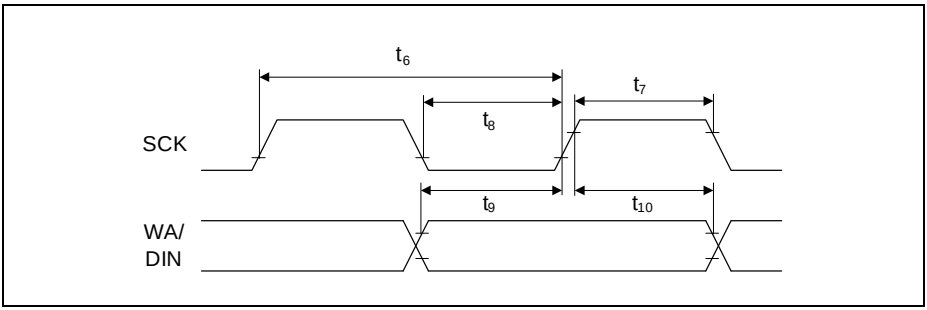


Figure 34 USIC IIS Slave Receiver Timing