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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	668-BBGA Exposed Pad
Supplier Device Package	668-PBGA-PGE (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc8358ecvragdda

- — Advanced encryption standard unit (AESU)
- — Implements the Rinjdael symmetric key cipher
- — Key lengths of 128, 192, and 256 bits, two key
  - – ECB, CBC, CCM, and counter modes
- — ARC four execution unit (AFEU)
  - – Implements a stream cipher compatible with the RC4 algorithm
  - – 40- to 128-bit programmable key
- — Message digest execution unit (MDEU)
  - – SHA with 160-, 224-, or 256-bit message digest
  - – MD5 with 128-bit message digest
  - – HMAC with either SHA or MD5 algorithm
- — Random number generator (RNG)
- — Four crypto-channels, each supporting multi-command descriptor chains
  - – Static and/or dynamic assignment of crypto-execution units via an integrated controller
  - – Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
- — Storage/NAS XOR parity generation accelerator for RAID applications

- DDR SDRAM memory controller on the MPC8358E
  - — Programmable timing supporting both DDR1 and DDR2 SDRAM
  - — On the MPC8358E, the DDR bus can be configured as a 32- or 64-bit bus
  - — 32- or 64-bit data interface, up to 266 MHz (for the MPC8358E) data rate
  - — Four banks of memory, each up to 1 Gbyte
  - — DRAM chip configurations from 64 Mbits to 1 Gigabit with ×8/×16 data ports
  - — Full ECC support
  - — Page mode support (up to 16 simultaneous open pages for DDR1, up to 32 simultaneous open pages for DDR2)
  - — Contiguous or discontiguous memory mapping
  - — Read-modify-write support
  - — Sleep mode support for self refresh SDRAM
  - — Supports auto refreshing
  - — Supports source clock mode
  - — On-the-fly power management using CKE
  - — Registered DIMM support
  - — 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2
  - — External driver impedance calibration
  - — On-die termination (ODT)
- PCI interface
  - — PCI Specification Revision 2.3 compatible