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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e300 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 400MHz |
| Co-Processors/DSP | Communications; QUICC Engine, Security; SEC |
| RAM Controllers | DDR, DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (1) |
| SATA | - |
| USB | USB 1.x (1) |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 668-BBGA Exposed Pad |
| Supplier Device Package | 668-PBGA-PGE (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc8358eczqagdga |

## 2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the device. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

**Table 2. Recommended Operating Conditions**

| Characteristic | Symbol | Recommended Value | Unit | Notes |
|---|---|---|---|---|
| Core supply voltage | $V_{DD}$ | 1.2 V ± 60 mV | V | 1 |
| PLL supply voltage | $AV_{DD}$ | 1.2 V ± 60 mV | V | 1 |
| DDR and DDR2 DRAM I/O supply voltage<br>DDR<br>DDR2 | $GV_{DD}$ | <br>2.5 V ± 125 mV<br>1.8 V ± 90 mV | V | — |
| Three-speed Ethernet I/O supply voltage | $LV_{DD}0$ | 3.3 V ± 330 mV<br>2.5 V ± 125 mV | V | — |
| Three-speed Ethernet I/O supply voltage | $LV_{DD}1$ | 3.3 V ± 330 mV<br>2.5 V ± 125 mV | V | — |
| Three-speed Ethernet I/O supply voltage | $LV_{DD}2$ | 3.3 V ± 330 mV<br>2.5 V ± 125 mV | V | — |
| PCI, local bus, DUART, system control and power management, $I^2C$, SPI, and JTAG I/O voltage | $OV_{DD}$ | 3.3 V ± 330 mV | V | — |
| Junction temperature | $T_J$ | 0 to 105<br>–40 to 105 | °C | — |

**Notes:**
1. $GV_{DD}$, $LV_{DD}$, $OV_{DD}$, $AV_{DD}$, and $V_{DD}$ must track each other and must vary in the same direction—either in the positive or negative direction.

Table 5 shows the estimated typical I/O power dissipation for the device.

**Table 5. Estimated Typical I/O Power Dissipation**

| Interface | Parameter | $GV_{DD}$ (1.8 V) | $GV_{DD}$ (2.5 V) | $OV_{DD}$ (3.3 V) | $LV_{DD}$ (3.3 V) | $LV_{DD}$ (2.5 V) | Unit | Comments |
|---|---|---|---|---|---|---|---|---|
| DDR I/O<br>65% utilization<br>2.5 V<br>$R_s$ = 20 Ω<br>$R_t$ = 50 Ω<br>2 pairs of clocks | 200 MHz, 1x32 bits | 0.3 | 0.46 | — | — | — | W | — |
| | 200 MHz, 1x64 bits | 0.4 | 0.58 | — | — | — | W | — |
| | 200 MHz, 2x32 bits | 0.6 | 0.92 | — | — | — | W | — |
| | 266 MHz, 1x32 bits | 0.35 | 0.56 | — | — | — | W | — |
| | 266 MHz, 1x64 bits | 0.46 | 0.7 | — | — | — | W | — |
| | 266 MHz, 2x32 bits | 0.7 | 1.11 | — | — | — | W | — |
| Local Bus I/O<br>Load = 25 pf<br>3 pairs of clocks | 133 MHz, 32 bits | — | — | 0.22 | — | — | W | — |
| | 83 MHz, 32 bits | — | — | 0.14 | — | — | W | — |
| | 66 MHz, 32 bits | — | — | 0.12 | — | — | W | — |
| | 50 MHz, 32 bits | — | — | 0.09 | — | — | W | — |
| PCI I/O<br>Load = 30 pF | 33 MHz, 32 bits | — | — | 0.05 | — | — | W | — |
| | 66 MHz, 32 bits | — | — | 0.07 | — | — | W | — |
| 10/100/1000 Ethernet I/O<br>Load = 20 pF | MII or RMII | — | — | — | 0.01 | — | W | Multiply by number of interfaces used. |
| | GMII or TBI | — | — | — | 0.04 | — | W | |
| | RGMII or RTBI | — | — | — | — | 0.04 | W | |
| Other I/O | — | — | — | 0.1 | — | — | W | — |

# 4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8358E.

**NOTE**

The rise/fall time on QUICC Engine block input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of $V_{DD}$; fall time refers to transitions from 90% to 10% of $V_{DD}$.

**Table 9. RESET Pins DC Electrical Characteristics (continued)**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V |

**Notes:**
1. This table applies for pins $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, and $\overline{\text{QUIESCE}}$.
2. $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are open drain pins, thus $V_{OH}$ is not relevant for those pins.

## 5.2 RESET AC Electrical Characteristics

This section describes the AC electrical specifications for the reset initialization timing requirements of the device. Table 10 provides the reset initialization AC timing specifications for the DDR SDRAM component(s).

**Table 10. RESET Initialization Timing Specifications**

| Parameter/Condition | Min | Max | Unit | Notes |
|---|---|---|---|---|
| Required assertion time of $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$ (input) to activate reset flow | 32 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to CLKIN when the device is in PCI host mode | 32 | — | $t_{CLKIN}$ | 2 |
| Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_SYNC_IN when the device is in PCI agent mode | 32 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| $\overline{\text{HRESET}}$/$\overline{\text{SRESET}}$ assertion (output) | 512 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| $\overline{\text{HRESET}}$ negation to $\overline{\text{SRESET}}$ negation (output) | 16 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| Input setup time for POR config signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode | 4 | — | $t_{CLKIN}$ | 2 |
| Input setup time for POR config signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode | 4 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$ | 0 | — | ns | |
| Time for the device to turn off POR config signals with respect to the assertion of $\overline{\text{HRESET}}$ | — | 4 | ns | 3 |
| Time for the device to turn on POR config signals with respect to the negation of $\overline{\text{HRESET}}$ | 1 | — | $t_{PCI\_SYNC\_IN}$ | 1, 3 |

**Notes:**
1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8360E PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for more details.
2. $t_{CLKIN}$ is the clock period of the input clock applied to CLKIN. It is only valid when the device is in PCI host mode. See the *MPC8360E PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for more details.
3. POR config signals consists of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 16 provides the DDR capacitance when $GV_{DD}$(typ) = 2.5 V.

**Table 16. DDR SDRAM Capacitance for $GV_{DD}$(typ) = 2.5 V**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input/output capacitance: DQ, DQS | $C_{IO}$ | 6 | 8 | pF | 1 |
| Delta input/output capacitance: DQ, DQS | $C_{DIO}$ | — | 0.5 | pF | 1 |

**Note:**
1. This parameter is sampled. $GV_{DD}$ = 2.5 V ± 0.125 V, f = 1 MHz, $T_A$ = 25°C, $V_{OUT}$ = $GV_{DD}$/2, $V_{OUT}$ (peak-to-peak) = 0.2 V.

## 6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

### 6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR2 SDRAM interface when $GV_{DD}$(typ) = 1.8 V.

**Table 17. DDR2 SDRAM Input AC Timing Specifications for $GV_{DD}$(typ) = 1.8 V**

At recommended operating conditions with $GV_{DD}$ of 1.8 V ± 5%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| AC input low voltage | $V_{IL}$ | — | $MV_{REF}$ – 0.25 | V | — |
| AC input high voltage | $V_{IH}$ | $MV_{REF}$ + 0.25 | — | V | — |

Table 18 provides the input AC timing specifications for the DDR SDRAM interface when $GV_{DD}$(typ) = 2.5 V.

**Table 18. DDR SDRAM Input AC Timing Specifications**

At recommended operating conditions with $GV_{DD}$ of 2.5 V ± 5%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| AC input low voltage | $V_{IL}$ | — | $MV_{REF}$ – 0.31 | V | — |
| AC input high voltage | $V_{IH}$ | $MV_{REF}$ + 0.31 | — | V | — |

**Note:**
1. Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 ≤ n ≤ 7) or ECC (MECC[{0...7}] if n = 8).

## 8.1 Three-Speed Ethernet Controller (10/100/1000 Mbps)—GMII/MII/RMII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), MII (media independent interface), RMII (reduced media independent interface), TBI (ten-bit interface), RGMII (reduced gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The MII, RMII, GMII, and TBI interfaces are only defined for 3.3 V, while the RGMII and RTBI interfaces are only defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for the MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

### 8.1.1 10/100/1000 Ethernet DC Electrical Characteristics

The electrical characteristics specified here apply to media independent interface (MII), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), reduced media independent interface (RMII) signals, management data input/output (MDIO) and management data clock (MDC).

The MII and RMII interfaces are defined for 3.3 V, while the RGMII and RTBI interfaces can be operated at 2.5 V. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3*. The RMII interface follows the *RMII Consortium RMII Specification Version 1.2*.

**Table 24. RGMII/RTBI, GMII, TBI, MII, and RMII DC Electrical Characteristics (when operating at 3.3 V)**

| Parameter | Symbol | Conditions | | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Supply voltage 3.3 V | $LV_{DD}$ | — | | 2.97 | 3.63 | V | 1 |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –4.0 mA | $LV_{DD}$ = Min | 2.40 | $LV_{DD}$ + 0.3 | V | — |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 4.0 mA | $LV_{DD}$ = Min | GND | 0.50 | V | — |
| Input high voltage | $V_{IH}$ | — | — | 2.0 | $LV_{DD}$ + 0.3 | V | — |
| Input low voltage | $V_{IL}$ | — | — | –0.3 | 0.90 | V | — |
| Input current | $I_{IN}$ | $0 V \le V_{IN} \le LV_{DD}$ | | — | ±10 | μA | — |

**Note:**
1. GMII/MII pins that are not needed for RGMII, RMII, or RTBI operation are powered by the $OV_{DD}$ supply.

**Table 25. RGMII/RTBI DC Electrical Characteristics (when operating at 2.5 V)**

| Parameters | Symbol | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage 2.5 V | $LV_{DD}$ | — | | 2.37 | 2.63 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –1.0 mA | $LV_{DD}$ = Min | 2.00 | $LV_{DD}$ + 0.3 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 1.0 mA | $LV_{DD}$ = Min | GND – 0.3 | 0.40 | V |
| Input high voltage | $V_{IH}$ | — | $LV_{DD}$ = Min | 1.7 | $LV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | $LV_{DD}$ = Min | –0.3 | 0.70 | V |
| Input current | $I_{IN}$ | $0 V \le V_{IN} \le LV_{DD}$ | | — | ±10 | μA |

## 8.2 GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

### 8.2.1 GMII Timing Specifications

This sections describe the GMII transmit and receive AC timing specifications.

#### 8.2.1.1 GMII Transmit AC Timing Specifications

Table 26 provides the GMII transmit AC timing specifications.

**Table 26. GMII Transmit AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/OV_{DD}$ of 3.3 V ± 10%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| GTX_CLK clock period | $t_{GTX}$ | — | 8.0 | — | ns | — |
| GTX_CLK duty cycle | $t_{GTXH}/t_{GTX}$ | 40 | — | 60 | % | — |
| GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay | $t_{GTKHDX}$<br>$t_{GTKHDV}$ | 0.5<br>— | — | —<br>5.0 | ns | — |
| GTX_CLK clock rise time, (20% to 80%) | $t_{GTXR}$ | — | — | 1.0 | ns | — |
| GTX_CLK clock fall time, (80% to 20%) | $t_{GTXF}$ | — | — | 1.0 | ns | — |
| GTX_CLK125 clock period | $t_{G125}$ | — | 8.0 | — | ns | 2 |
| GTX_CLK125 reference clock duty cycle measured at $LV_{DD/2}$ | $t_{G125H}/t_{G125}$ | 45 | — | 55 | % | 2 |

**Notes:**

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{GTKHDV}$ symbolizes GMII transmit timing (GT) with respect to the $t_{GTX}$ clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, $t_{GTKHDX}$ symbolizes GMII transmit timing (GT) with respect to the $t_{GTX}$ clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{GTX}$ represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This symbol is used to represent the external GTX_CLK125 signal and does not follow the original symbol naming convention.

Figure 10 shows the GMII receive AC timing diagram.

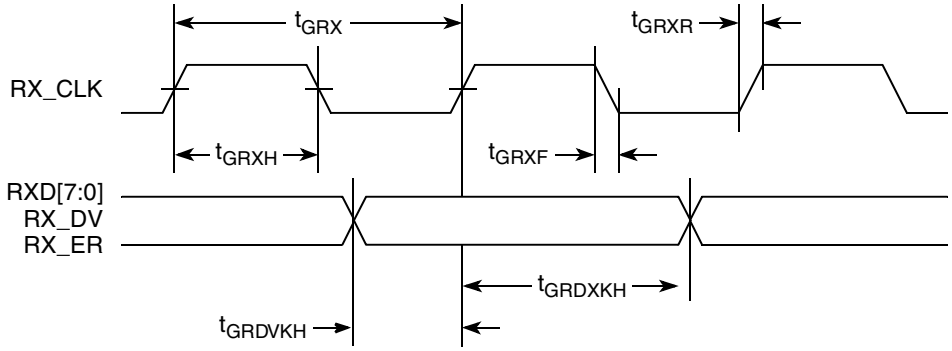


**Figure 10. GMII Receive AC Timing Diagram**

## 8.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

### 8.2.2.1 MII Transmit AC Timing Specifications

Table 28 provides the MII transmit AC timing specifications.

**Table 28. MII Transmit AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/OV_{DD}$ of 3.3 V ± 10%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TX_CLK clock period 10 Mbps | $t_{MTX}$ | — | 400 | — | ns |
| TX_CLK clock period 100 Mbps | $t_{MTX}$ | — | 40 | — | ns |
| TX_CLK duty cycle | $t_{MTXH}/t_{MTX}$ | 35 | — | 65 | % |
| TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay | $t_{MTKHDX}$<br>$t_{MTKHDV}$ | 1<br>— | 5 | —<br>15 | ns |
| TX_CLK data clock rise time, (20% to 80%) | $t_{MTXR}$ | 1.0 | — | 4.0 | ns |
| TX_CLK data clock fall time, (80% to 20%) | $t_{MTXF}$ | 1.0 | — | 4.0 | ns |

**Note:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MTKHDX}$ symbolizes MII transmit timing (MT) for the time $t_{MTX}$ clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of $t_{MTX}$ represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 11 shows the MII transmit AC timing diagram.

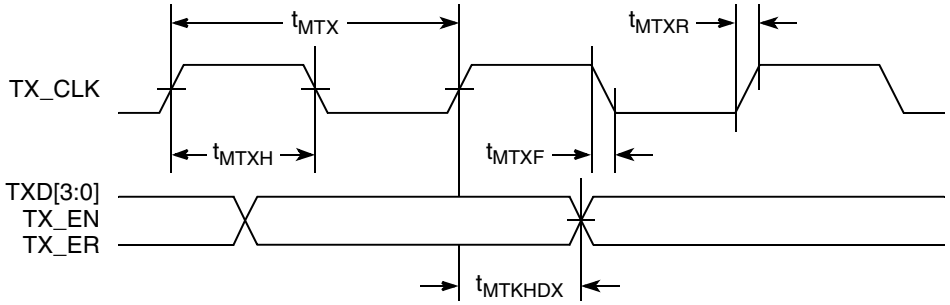


**Figure 11. MII Transmit AC Timing Diagram**

### 8.2.2.2 MII Receive AC Timing Specifications

Table 29 provides the MII receive AC timing specifications.

**Table 29. MII Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/OV_{DD}$ of 3.3 V ± 10%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period 10 Mbps | $t_{MRX}$ | — | 400 | — | ns |
| RX_CLK clock period 100 Mbps | $t_{MRX}$ | — | 40 | — | ns |
| RX_CLK duty cycle | $t_{MRXH}/t_{MRX}$ | 35 | — | 65 | % |
| RXD[3:0], RX_DV, RX_ER setup time to RX_CLK | $t_{MRDVKH}$ | 10.0 | — | — | ns |
| RXD[3:0], RX_DV, RX_ER hold time to RX_CLK | $t_{MRDXKH}$ | 10.0 | — | — | ns |
| RX_CLK clock rise time, (20% to 80%) | $t_{MRXR}$ | 1.0 | — | 4.0 | ns |
| RX_CLK clock fall time, (80% to 20%) | $t_{MRXF}$ | 1.0 | — | 4.0 | ns |

**Note:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MRDVKH}$ symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{MRDXKL}$ symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{MRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{MRX}$ represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 12 provides the AC test load.

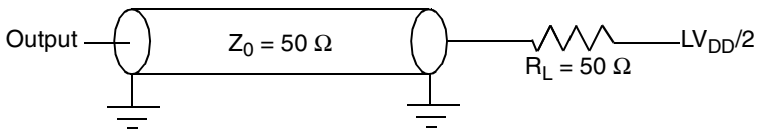


**Figure 12. AC Test Load**

Figure 14 shows the RMII transmit AC timing diagram.

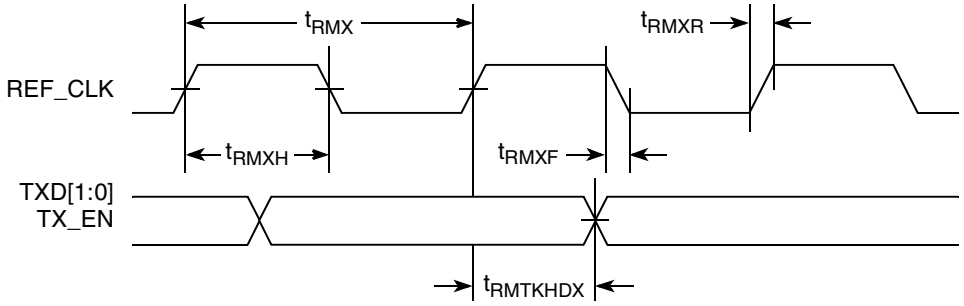


**Figure 14. RMII Transmit AC Timing Diagram**

### 8.2.3.2 RMII Receive AC Timing Specifications

Table 31 provides the RMII receive AC timing specifications.

**Table 31. RMII Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/OV_{DD}$ of 3.3 V ± 10%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| REF_CLK clock period | $t_{RMX}$ | — | 20 | — | ns |
| REF_CLK duty cycle | $t_{RMXH}/t_{RMX}$ | 35 | — | 65 | % |
| RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK | $t_{RMRDVKH}$ | 4.0 | — | — | ns |
| RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK | $t_{RMRDXKH}$ | 2.0 | — | — | ns |
| REF_CLK clock rise time | $t_{RMXR}$ | 1.0 | — | 4.0 | ns |
| REF_CLK clock fall time | $t_{RMXF}$ | 1.0 | — | 4.0 | ns |

**Note:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{RMX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{RMX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{RMX}$ represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 15 provides the AC test load.

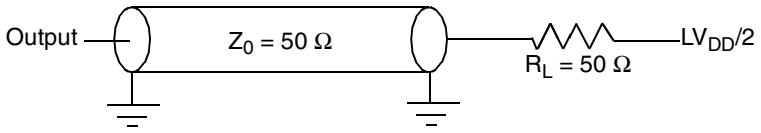


**Figure 15. AC Test Load**

**Table 37. IEEE 1588 Timer AC Specifications (continued)**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Timer alarm to output valid | $t_{TMRAL}$ | — | — | — | 2 |

**Notes:**
1. The timer can operate on rtc_clock or tmr_clock. These clocks get muxed and any one of them can be selected. The minimum and maximum requirement for both rtc_clock and tmr_clock are the same.
2. These are asynchronous signals.
3. Inputs need to be stable at least one TMR clock.

# 9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8358E.

## 9.1 Local Bus DC Electrical Characteristics

Table 38 provides the DC electrical characteristics for the local bus interface.

**Table 38. Local Bus DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| High-level output voltage, $I_{OH}$ = –100 µA | $V_{OH}$ | $OV_{DD}$ – 0.4 | — | V |
| Low-level output voltage, $I_{OL}$ = 100 µA | $V_{OL}$ | — | 0.2 | V |
| Input current | $I_{IN}$ | — | ±10 | µA |

## 9.2 Local Bus AC Electrical Specifications

Table 39 describes the general timing parameters of the local bus interface of the device.

**Table 39. Local Bus General Timing Parameters—DLL Enabled**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 7.5 | — | ns | 2 |
| Input setup to local bus clock (except LUPWAIT) | $t_{LBIVKH1}$ | 1.7 | — | ns | 3, 4 |
| LUPWAIT input setup to local bus clock | $t_{LBIVKH2}$ | 1.9 | — | ns | 3, 4 |
| Input hold from local bus clock (except LUPWAIT) | $t_{LBIXKH1}$ | 1.0 | — | ns | 3, 4 |
| LUPWAIT input hold from local bus clock | $t_{LBIXKH2}$ | 1.0 | — | ns | 3, 4 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT1}$ | 1.5 | — | ns | 5 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT2}$ | 3.0 | — | ns | 6 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT3}$ | 2.5 | — | ns | 7 |

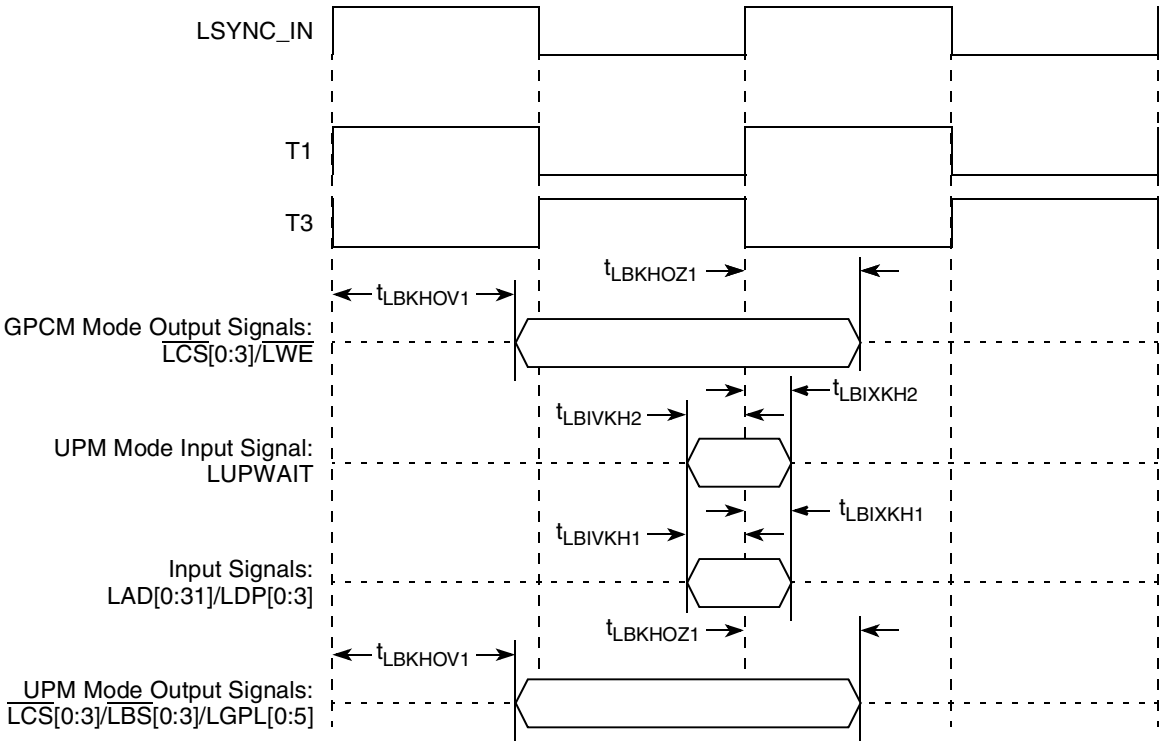


**Figure 24. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (DLL Enabled)**

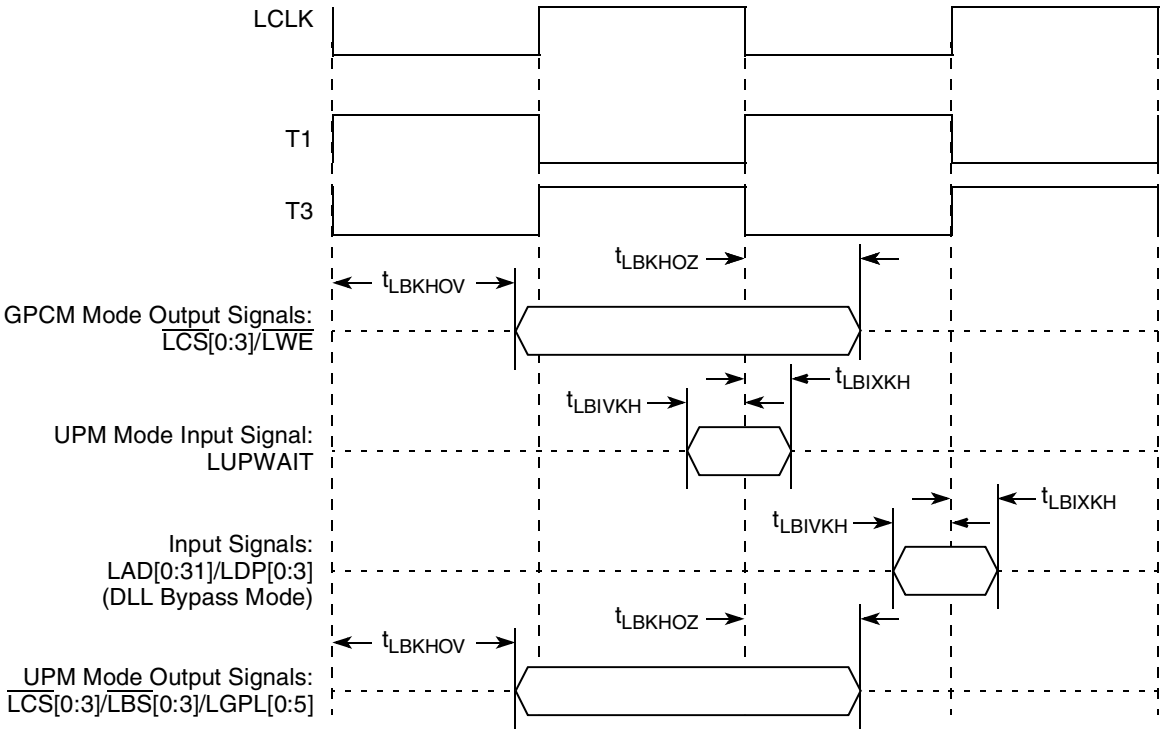


**Figure 25. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (DLL Bypass Mode)**

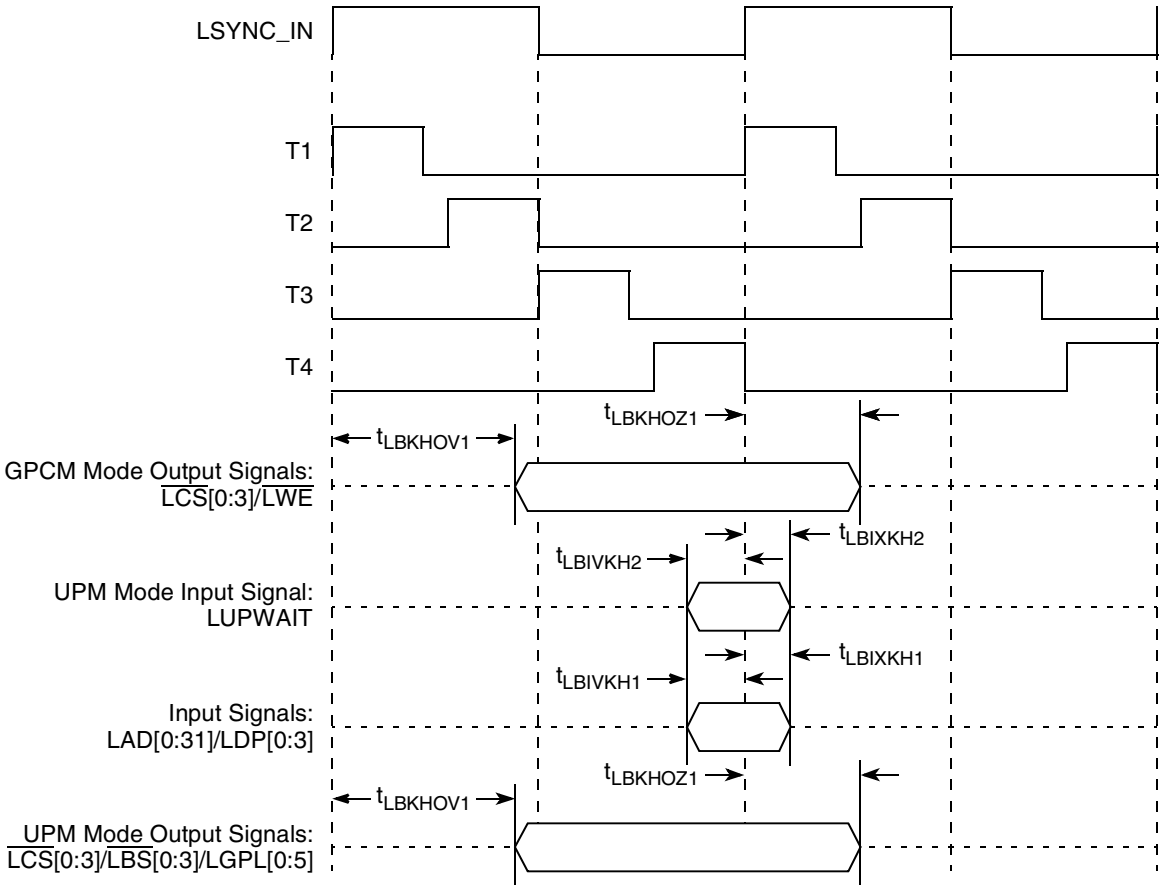


**Figure 27. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (DLL Enabled)**

# 10 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8358E.

## 10.1 JTAG DC Electrical Characteristics

Table 41 provides the DC electrical characteristics for the IEEE 1149.1 (JTAG) interface of the device.

**Table 41. JTAG interface DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –6.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 6.0 mA | — | 0.5 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V |
| Input high voltage | $V_{IH}$ | — | 2.5 | $OV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | $0 V \le V_{IN} \le OV_{DD}$ | — | ±10 | μA |

Figure 32 provides the test access port timing diagram.

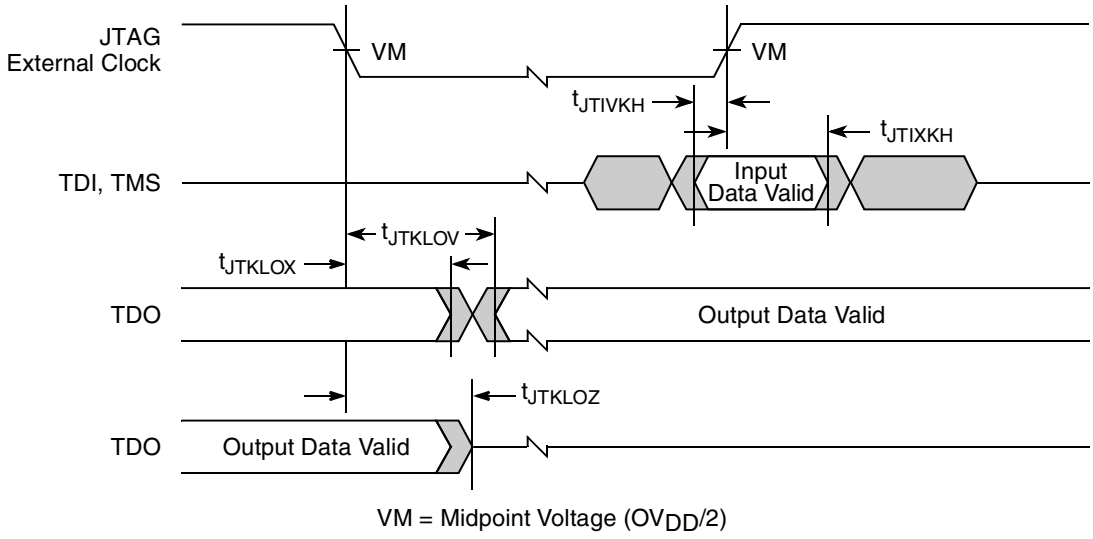


**Figure 32. Test Access Port Timing Diagram**

**Table 44. I²C AC Electrical Specifications (continued)**

All values refer to $V_{IH}$ (min) and $V_{IL}$ (max) levels (see Table 43).

| Parameter | Symbol[1] | Min | Max | Unit |
|---|---|---|---|---|
| Data hold time:<br>CBUS compatible masters<br>I²C bus devices | $t_{I2DXKL}$ | <br>—<br>0[2] | <br>—<br>0.9[3] | µs |
| Rise time of both SDA and SCL signals | $t_{I2CR}$ | 20 + 0.1 $C_b$[4] | 300 | ns |
| Fall time of both SDA and SCL signals | $t_{I2CF}$ | 20 + 0.1 $C_b$[4] | 300 | ns |
| Set-up time for STOP condition | $t_{I2PVKH}$ | 0.6 | — | µs |
| Bus free time between a STOP and START condition | $t_{I2KHDX}$ | 1.3 | — | µs |
| Noise margin at the LOW level for each connected device (including hysteresis) | $V_{NL}$ | 0.1 × $OV_{DD}$ | — | V |
| Noise margin at the HIGH level for each connected device (including hysteresis) | $V_{NH}$ | 0.2 × $OV_{DD}$ | — | V |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{I2DVKH}$ symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{I2SXKL}$ symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the $t_{I2C}$ clock reference (K) going to the low (L) state or hold time. Also, $t_{I2PVKH}$ symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The device provides a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH}$ min of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum $t_{I2DVKH}$ has only to be met if the device does not stretch the LOW period ($t_{I2CL}$) of the SCL signal.
4. $C_B$ = capacitance of one bus line in pF.

Figure 33 provides the AC test load for the I²C.

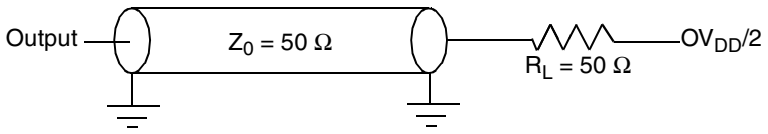


**Figure 33. I²C AC Test Load**

Figure 34 shows the AC timing diagram for the I²C bus.

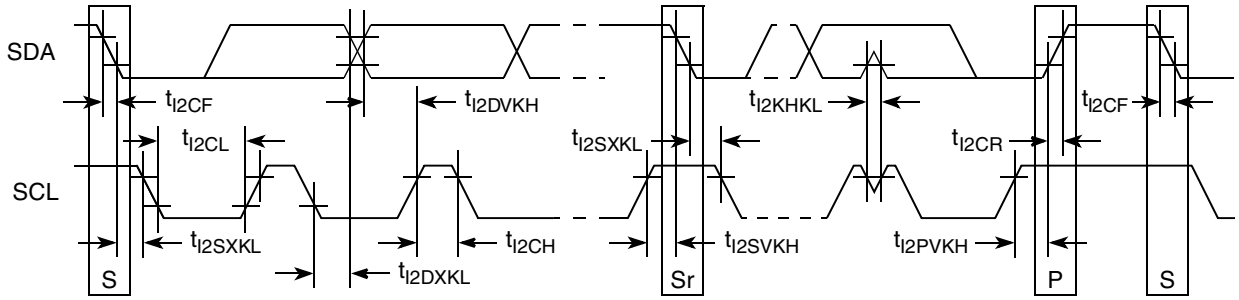


**Figure 34. I²C Bus AC Timing Diagram**

**Table 47. PCI AC Timing Specifications at 33 MHz**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Clock to output valid | $t_{PCKHOV}$ | — | 11 | ns | 2 |
| Output hold from clock | $t_{PCKHOX}$ | 2 | — | ns | 2 |
| Clock to output high impedance | $t_{PCKHOZ}$ | — | 14 | ns | 2, 3 |
| Input setup to clock | $t_{PCIVKH}$ | 7.0 | — | ns | 2, 4 |
| Input hold from clock | $t_{PCIXKH}$ | 0.3 | — | ns | 2, 4 |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{PCIVKH}$ symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, $t_{SYS}$, reference (K) going to the high (H) state or setup time. Also, $t_{PCRHFV}$ symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Figure 35 provides the AC test load for PCI.

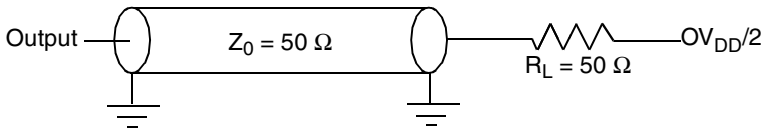


**Figure 35. PCI AC Test Load**

Figure 36 shows the PCI input AC timing conditions.

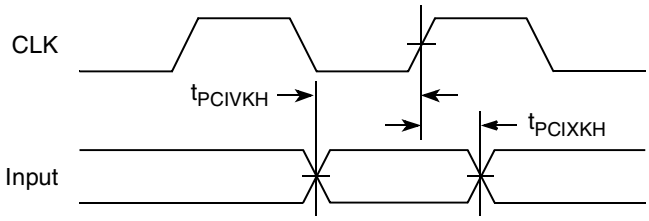


**Figure 36. PCI Input AC Timing Measurement Conditions**

Figure 38 provides the AC test load for the timers.

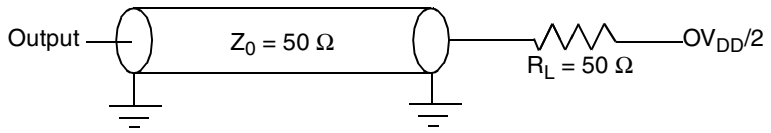


**Figure 38. Timers AC Test Load**

# 14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8358E.

## 14.1 GPIO DC Electrical Characteristics

Table 50 provides the DC electrical characteristics for the device GPIO.

**Table 50. GPIO DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –6.0 mA | 2.4 | — | V | 1 |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 6.0 mA | — | 0.5 | V | 1 |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V | 1 |
| Input high voltage | $V_{IH}$ | — | 2.0 | $OV_{DD}$ + 0.3 | V | 1 |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V | — |
| Input current | $I_{IN}$ | 0 V ≤ $V_{IN}$ ≤ $OV_{DD}$ | — | ±10 | μA | — |

**Note:** This specification applies when operating from 3.3-V supply.

## 14.2 GPIO AC Timing Specifications

Table 51 provides the GPIO input and output AC timing specifications.

**Table 51. GPIO Input AC Timing Specifications[1]**

| Characteristic | Symbol[2] | Typ | Unit |
|---|---|---|---|
| GPIO inputs—minimum pulse width | $t_{PIWID}$ | 20 | ns |

**Notes:**
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least $t_{PIWID}$ ns to ensure proper operation.

**Table 65. MPC8358E PBGA Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| LGPL2/<br>LSDRAS/<br>LOE | AH19 | O | $OV_{DD}$ | — |
| LGPL3/<br>LSDCAS/<br>cfg_reset_source2 | AE18 | I/O | $OV_{DD}$ | — |
| LGPL4/<br>LGTA/<br>LUPWAIT/<br>LPBSE | AG19 | I/O | $OV_{DD}$ | — |
| LGPL5/<br>cfg_clkin_div | AF19 | I/O | $OV_{DD}$ | — |
| LCKE | AD8 | O | $OV_{DD}$ | — |
| LCLK[0] | AC9 | O | $OV_{DD}$ | — |
| LCLK[1]/<br>LCS[6] | AG6 | O | $OV_{DD}$ | — |
| LCLK[2]/<br>LCS[7] | AE7 | O | $OV_{DD}$ | — |
| LSYNC_OUT | AG4 | O | $OV_{DD}$ | — |
| LSYNC_IN | AC8 | I | $OV_{DD}$ | — |
| **Programmable Interrupt Controller** | | | | |
| MCP_OUT | AG3 | O | $OV_{DD}$ | 2 |
| IRQ0/<br>MCP_IN | AH4 | I | $OV_{DD}$ | — |
| IRQ[1:2] | AG5, AH5 | I/O | $OV_{DD}$ | — |
| IRQ[3]/<br>CORE_SRESET | AD7 | I/O | $OV_{DD}$ | — |
| IRQ[4:5] | AC7, AD6 | I/O | $OV_{DD}$ | — |
| IRQ[6:7] | AC6, AC10 | I/O | $OV_{DD}$ | — |
| **DUART** | | | | |
| UART1_SOUT | AE3 | O | $OV_{DD}$ | — |
| UART1_SIN | AE4 | I/O | $OV_{DD}$ | — |
| UART1_CTS | AG2 | I/O | $OV_{DD}$ | — |
| UART1_RTS | AA6 | O | $OV_{DD}$ | — |
| **$I^2C$ Interface** | | | | |
| IIC1_SDA | AB6 | I/O | $OV_{DD}$ | 2 |
| IIC1_SCL | AD5 | I/O | $OV_{DD}$ | 2 |
| IIC2_SDA | AF3 | I/O | $OV_{DD}$ | 2 |
| IIC2_SCL | AH2 | I/O | $OV_{DD}$ | 2 |
| **QUICC Engine** | | | | |
| CE_PA[0] | F6 | I/O | $LV_{DD}0$ | — |

# 22 Clocking

Figure 53 shows the internal distribution of clocks within the MPC8358E.

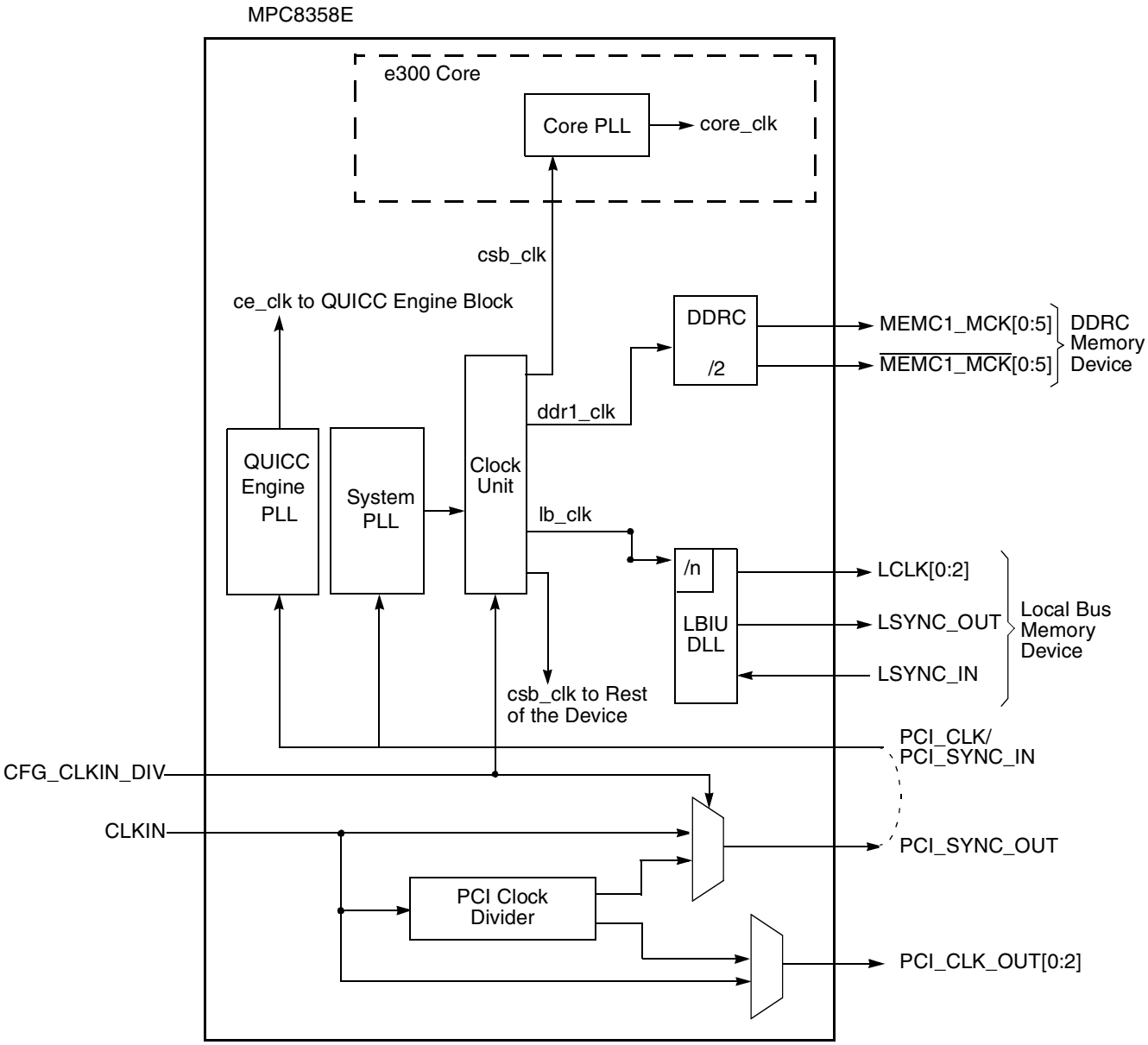


**Figure 53. MPC8358E Clock Subsystem**

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Note that in PCI host mode, the primary clock input also depends on whether PCI clock outputs are selected with RCWH[PCICKDRV]. When the device is configured as a PCI host device (RCWH[PCIHOST] = 1) and PCI clock output is selected (RCWH[PCICKDRV] = 1), CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration

Table 76 shows heat sinks and junction-to-ambient thermal resistance for PBGA package.

**Table 76. Heat Sinks and Junction-to-Ambient Thermal Resistance of PBGA Package**

| Heat Sink Assuming Thermal Grease | Air Flow | 29 × 29 mm PBGA |
|---|---|---|
| | | Thermal Resistance |
| AAVID 30 × 30 × 9.4 mm Pin Fin | Natural Convection | 12.6 |
| AAVID 30 × 30 × 9.4 mm Pin Fin | 1 m/s | 8.2 |
| AAVID 30 × 30 × 9.4 mm Pin Fin | 2 m/s | 7.0 |
| AAVID 31 × 35 × 23 mm Pin Fin | Natural Convection | 10.5 |
| AAVID 31 × 35 × 23 mm Pin Fin | 1 m/s | 6.6 |
| AAVID 31 × 35 × 23 mm Pin Fin | 2 m/s | 6.1 |
| Wakefield, 53 × 53 × 25 mm Pin Fin | Natural Convection | 9.0 |
| Wakefield, 53 × 53 × 25 mm Pin Fin | 1 m/s | 5.6 |
| Wakefield, 53 × 53 × 25 mm Pin Fin | 2 m/s | 5.1 |
| MEI, 75 × 85 × 12 no adjacent board, extrusion | Natural Convection | 9.0 |
| MEI, 75 × 85 × 12 no adjacent board, extrusion | 1 m/s | 5.7 |
| MEI, 75 × 85 × 12 no adjacent board, extrusion | 2 m/s | 5.1 |

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
473 Sapena Ct. #15
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

### 23.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

$T_J$ = junction temperature (°C)

$T_C$ = case temperature of the package (°C)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$P_D$ = power dissipation (W)

# 24 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8358E. Additional information can be found in *MPC8360E/MPC8358E PowerQUICC Design Checklist* (AN3097).

## 24.1 System Clocking

The device includes two PLLs, as follows.

- The platform PLL ($AV_{DD}1$) generates the platform clock from the externally supplied CLKIN input. The frequency ratio between the platform and CLKIN is selected using the platform PLL ratio configuration bits as described in Section 22.1, “System PLL Configuration.”
- The e300 core PLL ($AV_{DD}2$) generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 22.2, “Core PLL Configuration.”

## 24.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins ($AV_{DD}1$, $AV_{DD}2$, respectively). The $AV_{DD}$ level should always be equivalent to $V_{DD}$, and preferably these voltages will be derived directly from $V_{DD}$ through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in Figure 54, one to each of the five $AV_{DD}$ pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced.