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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	668-BBGA Exposed Pad
Supplier Device Package	668-PBGA-PGE (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8358czqagdga

  - 32-Kbyte instruction cache, 32-Kbyte data cache
  - Lockable portion of L1 cache
  - Dynamic power management
  - Software-compatible with the Freescale processor families implementing the Power Architecture™ technology
- QUICC Engine unit
  - Two 32-bit RISC controllers for flexible support of the communications peripherals, each operating up to 400 MHz (for the MPC8358E)
  - Serial DMA channel for receive and transmit on all serial channels
  - QUICC Engine module peripheral request interface (for SEC, PCI, IEEE Std. 1588™)
  - Six UCCs on the MPC8358E supporting the following protocols and interfaces (not all of them simultaneously):
    - IEEE 1588 protocol supported
    - 10/100 Mbps Ethernet/IEEE Std. 802.3™ CDMA/CS interface through a media-independent interface (MII, RMII, RGMII)[1]
    - 1000 Mbps Ethernet/IEEE 802.3 CDMA/CS interface through a media-independent interface (GMII, RGMII, TBI, RTBI) on UCC1 and UCC2
    - 9.6-Kbyte jumbo frames
    - ATM full-duplex SAR, up to 622 Mbps (OC-12/STM-4), AAL0, AAL1, and AAL5 in accordance ITU-T I.363.5
    - ATM AAL2 CPS, SSSAR, and SSTED up to 155 Mbps (OC-3/STM-1) Mbps full duplex (with 4 CPS packets per cell) in accordance ITU-T I.366.1 and I.363.2
    - ATM traffic shaping for CBR, VBR, UBR, and GFR traffic types compatible with ATM forum TM4.1 for up to 64-Kbyte simultaneous ATM channels
    - ATM AAL1 structured and unstructured circuit emulation service (CES 2.0) in accordance with ITU-T I.163.1 and ATM Forum af-vtoa-00-0078.000
    - IMA (Inverse Multiplexing over ATM) for up to 31 IMA links over 8 IMA groups in accordance with the ATM forum AF-PHY-0086.000 (Version 1.0) and AF-PHY-0086.001 (Version 1.1)
    - ATM Transmission Convergence layer support in accordance with ITU-T I.432
    - ATM OAM handling features compatible with ITU-T I.610
    - PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686, and 3153
    - IP support for IPv4 packets including TOS, TTL, and header checksum processing
    - Ethernet over first mile IEEE 802.3ah
    - Shim header
    - Ethernet-to-Ethernet/AAL5/AAL2 inter-working
    - L2 Ethernet switching using MAC address or IEEE Std. 802.1P/Q™ VLAN tags

1.SMII or SGMII media-independent interface is not currently supported.

- Advanced encryption standard unit (AESU)
- Implements the Rinjdael symmetric key cipher
- Key lengths of 128, 192, and 256 bits, two key
  - ECB, CBC, CCM, and counter modes
- ARC four execution unit (AFEU)
  - Implements a stream cipher compatible with the RC4 algorithm
  - 40- to 128-bit programmable key
- Message digest execution unit (MDEU)
  - SHA with 160-, 224-, or 256-bit message digest
  - MD5 with 128-bit message digest
  - HMAC with either SHA or MD5 algorithm
- Random number generator (RNG)
- Four crypto-channels, each supporting multi-command descriptor chains
  - Static and/or dynamic assignment of crypto-execution units via an integrated controller
  - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
- Storage/NAS XOR parity generation accelerator for RAID applications

- DDR SDRAM memory controller on the MPC8358E
  - Programmable timing supporting both DDR1 and DDR2 SDRAM
  - On the MPC8358E, the DDR bus can be configured as a 32- or 64-bit bus
  - 32- or 64-bit data interface, up to 266 MHz (for the MPC8358E) data rate
  - Four banks of memory, each up to 1 Gbyte
  - DRAM chip configurations from 64 Mbits to 1 Gigabit with ×8/×16 data ports
  - Full ECC support
  - Page mode support (up to 16 simultaneous open pages for DDR1, up to 32 simultaneous open pages for DDR2)
  - Contiguous or discontiguous memory mapping
  - Read-modify-write support
  - Sleep mode support for self refresh SDRAM
  - Supports auto refreshing
  - Supports source clock mode
  - On-the-fly power management using CKE
  - Registered DIMM support
  - 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2
  - External driver impedance calibration
  - On-die termination (ODT)
- PCI interface
  - PCI Specification Revision 2.3 compatible

2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the device. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	1.2 V ± 60 mV	V	1
PLL supply voltage	AV_{DD}	1.2 V ± 60 mV	V	1
DDR and DDR2 DRAM I/O supply voltage DDR DDR2	GV_{DD}	 2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Three-speed Ethernet I/O supply voltage	$LV_{DD}0$	3.3 V ± 330 mV 2.5 V ± 125 mV	V	—
Three-speed Ethernet I/O supply voltage	$LV_{DD}1$	3.3 V ± 330 mV 2.5 V ± 125 mV	V	—
Three-speed Ethernet I/O supply voltage	$LV_{DD}2$	3.3 V ± 330 mV 2.5 V ± 125 mV	V	—
PCI, local bus, DUART, system control and power management, I^2C, SPI, and JTAG I/O voltage	OV_{DD}	3.3 V ± 330 mV	V	—
Junction temperature	T_J	0 to 105 –40 to 105	°C	—

Notes:
1. GV_{DD}, LV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.

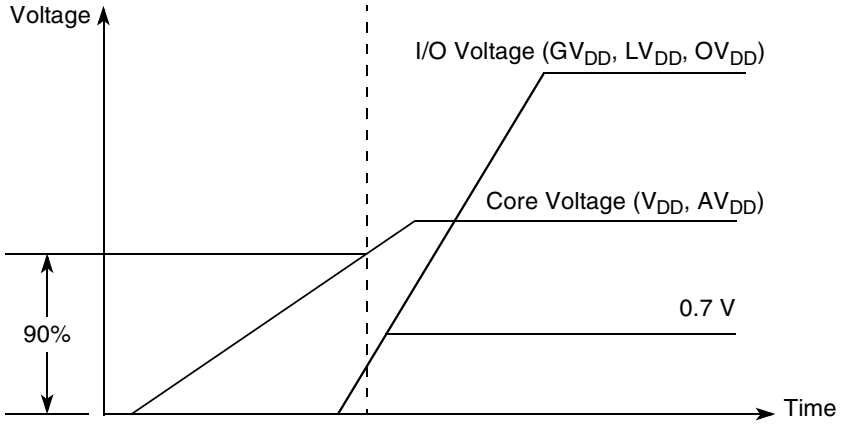

Figure 4. Power Sequencing Example

I/O voltage supplies (GV_{DD}, LV_{DD}, and OV_{DD}) do not have any ordering requirements with respect to one another.

2.2.2 Power-Down Sequencing

The MPC8358E does not require the core supply voltage and I/O supply voltages to be powered down in any particular order.

3 Power Characteristics

The estimated typical power dissipation values are shown in Table 4.

Table 4. MPC8358E PBGA Core Power Dissipation[1]

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
266	266	266	2.2	2.3	W	2, 3, 4
400	266	266	2.4	2.5	W	2, 3, 4
400	266	400	2.5	2.6	W	2, 3, 4

Notes:
1. The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see Table 5.
2. Typical power is based on a voltage of V_{DD} = 1.2 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.
3. Thermal solutions will likely need to design to a value higher than typical power on the end application, T_A target, and I/O power.
4. Maximum power is based on a voltage of V_{DD} = 1.2 V, WC process, a junction T_J = 105°C, and an artificial smoke test.

Table 12. QUICC Engine Block Operating Frequency Limitations (continued)

Interface	Interface Operating Frequency (MHz)	Max Interface Bit Rate (Mbps)	Min QUICC Engine Operating Frequency[1] (MHz)	Notes
UART/async HDLC	3.68 (max internal ref clock)	115 (Kbps)	20	—
BISYNC	2 (max)	2	20	—
USB	48 (ref clock)	12	96	—

Notes:
1. The QUICC Engine module needs to run at a frequency higher than or equal to what is listed in this table.
2. 'F' is the actual interface operating frequency.
3. The bit rate limit is independent of the data bus width (that is, the same for serial, nibble, or octal interfaces).
4. TDM in high-speed mode for serial data interface.

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR and DDR2 SDRAM interface of the MPC8358E.

6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

Table 13 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the device when GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.125$	V	—
Output leakage current	I_{OZ}	—	±10	µA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—
MV_{REF} input leakage current	I_{VREF}	—	±10	µA	—

Table 16 provides the DDR capacitance when GV_{DD}(typ) = 2.5 V.

Table 16. DDR SDRAM Capacitance for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR2 SDRAM interface when GV_{DD}(typ) = 1.8 V.

Table 17. DDR2 SDRAM Input AC Timing Specifications for GV_{DD}(typ) = 1.8 V

At recommended operating conditions with GV_{DD} of 1.8 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V	—

Table 18 provides the input AC timing specifications for the DDR SDRAM interface when GV_{DD}(typ) = 2.5 V.

Table 18. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V	—

Note:
1. Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 ≤ n ≤ 7) or ECC (MECC[{0...7}] if n = 8).

Figure 11 shows the MII transmit AC timing diagram.

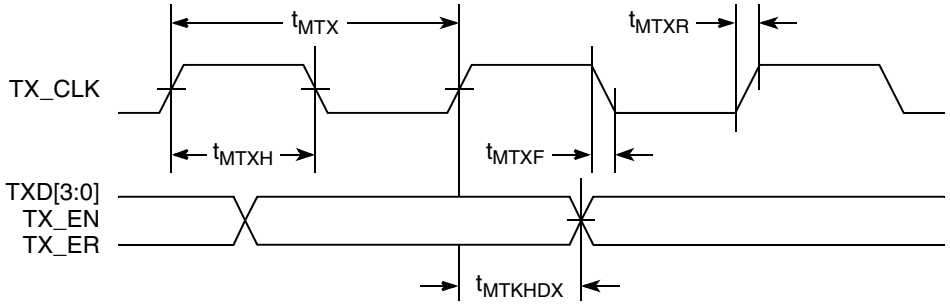

Figure 11. MII Transmit AC Timing Diagram

8.2.2.2 MII Receive AC Timing Specifications

Table 29 provides the MII receive AC timing specifications.

Table 29. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise time, (20% to 80%)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time, (80% to 20%)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 12 provides the AC test load.

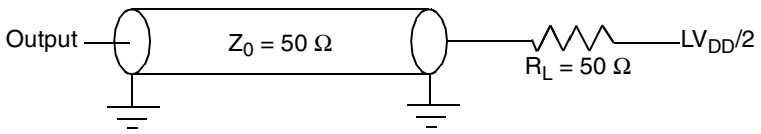

Figure 12. AC Test Load

Figure 16 shows the RMII receive AC timing diagram.

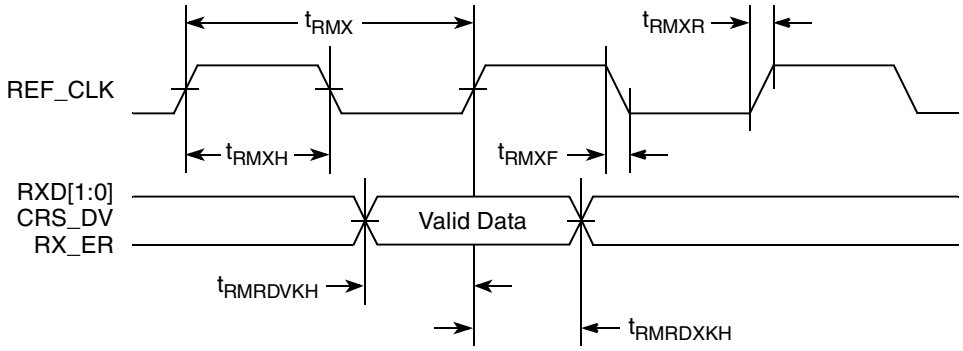

Figure 16. RMII Receive AC Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

Table 32 provides the TBI transmit AC timing specifications.

Table 32. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns	—
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	—	60	%	—
GTX_CLK to TBI data TCG[9:0] delay	t_{TTKHDX} t_{TTKHDV}	0.9 —	—	— 5.0	ns	
GTX_CLK clock rise time, (20% to 80%)	t_{TTXR}	—	—	1.0	ns	—
GTX_CLK clock fall time, (80% to 20%)	t_{TTXF}	—	—	1.0	ns	—
GTX_CLK125 reference clock period	t_{G125}	—	8.0	—	ns	2
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	45	—	55	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.

Figure 17 shows the TBI transmit AC timing diagram.

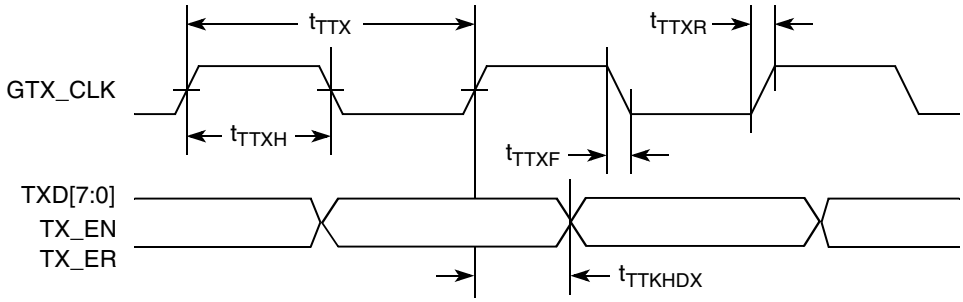

Figure 17. TBI Transmit AC Timing Diagram

8.2.4.2 TBI Receive AC Timing Specifications

Table 33 provides the TBI receive AC timing specifications.

Table 33. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
PMA_RX_CLK clock period	t_{TRX}	—	16.0	—	ns	—
PMA_RX_CLK skew	t_{SKTRX}	7.5	—	8.5	ns	—
RX_CLK duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%	—
RCG[9:0] setup time to rising PMA_RX_CLK	t_{TRDVKH}	2.5	—	—	ns	2
RCG[9:0] hold time to rising PMA_RX_CLK	t_{TRDXKH}	1.0	—	—	ns	2
RX_CLK clock rise time, V_{IL}(min) to V_{IH}(max)	t_{TRXR}	0.7	—	2.4	ns	—
RX_CLK clock fall time, V_{IH}(max) to V_{IL}(min)	t_{TRXF}	0.7	—	2.4	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. Setup and hold time of even numbered RCG are measured from riding edge of PMA_RX_CLK1. Setup and hold time of odd numbered RCG are measured from riding edge of PMA_RX_CLK0.

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, TBI, and RTBI are specified in Section 8.1, "Three-Speed Ethernet Controller (10/100/1000 Mbps)— GMII/MII/RMII/TBI/RGMII/RTBI Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 35.

Table 35. MII Management DC Electrical Characteristics When Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	OV_{DD} = Min	2.10	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	OV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±10	μA

8.3.2 MII Management AC Electrical Specifications

Table 36 provides the MII management AC timing specifications.

Table 36. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} is 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	$t_{MDTKHDX}$ $t_{MDTKHDV}$	10 —	—	— 110	ns	3
MDIO to MDC setup time	$t_{MDRDVKH}$	10	—	—	ns	—
MDIO to MDC hold time	$t_{MDRDXKH}$	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—

Figure 22 through Figure 27 show the local bus signals.

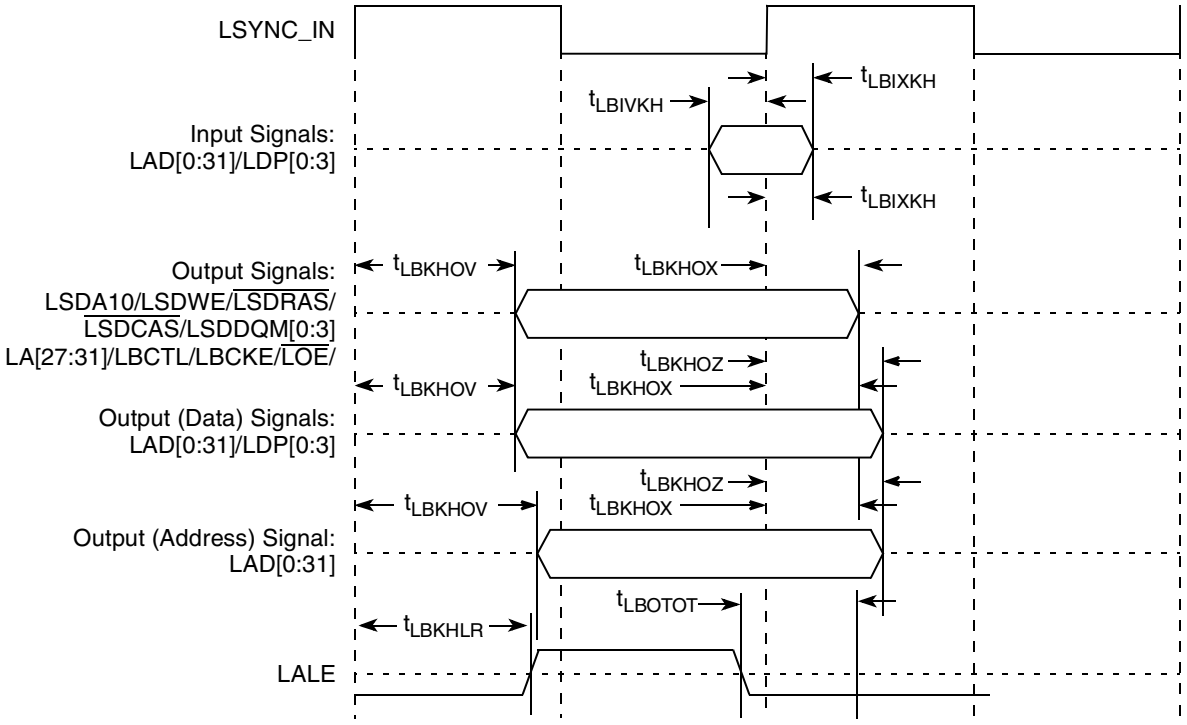

Figure 22. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)

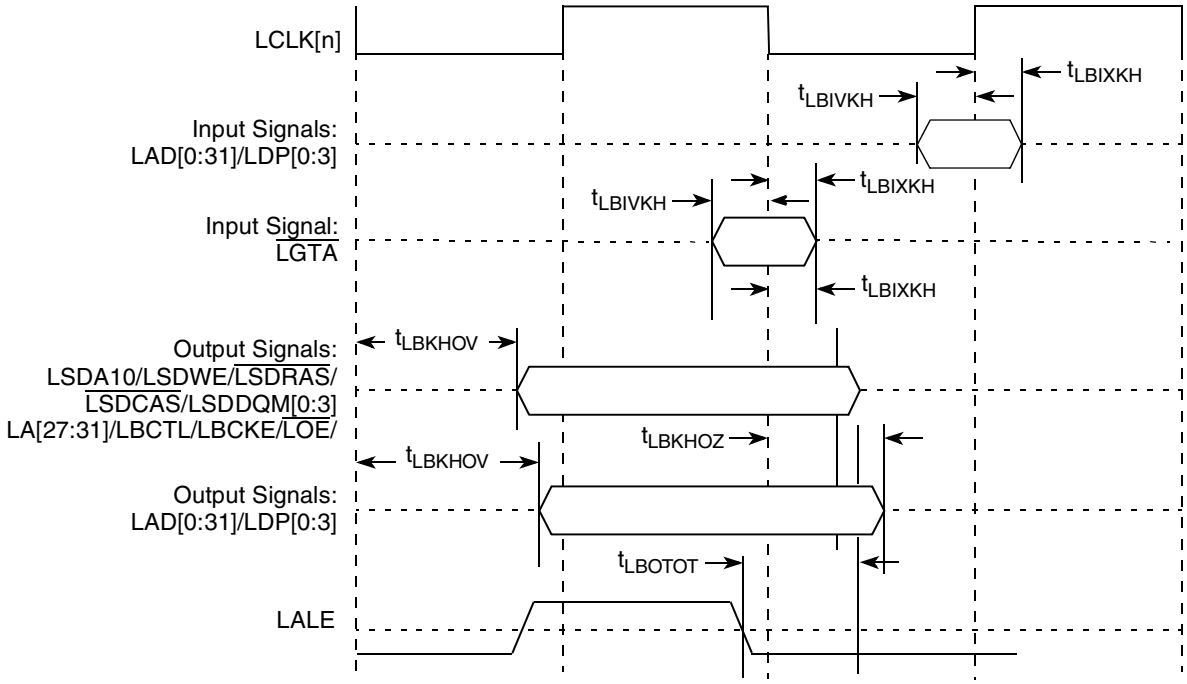

Figure 23. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)

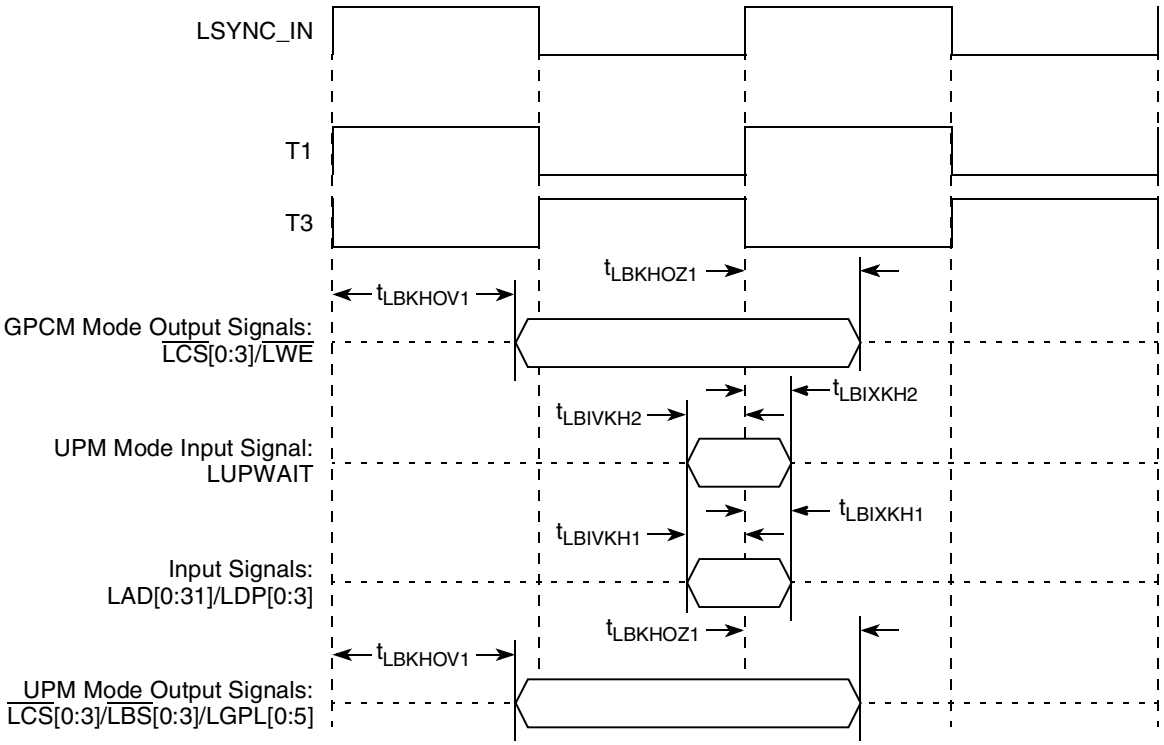

Figure 24. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (DLL Enabled)

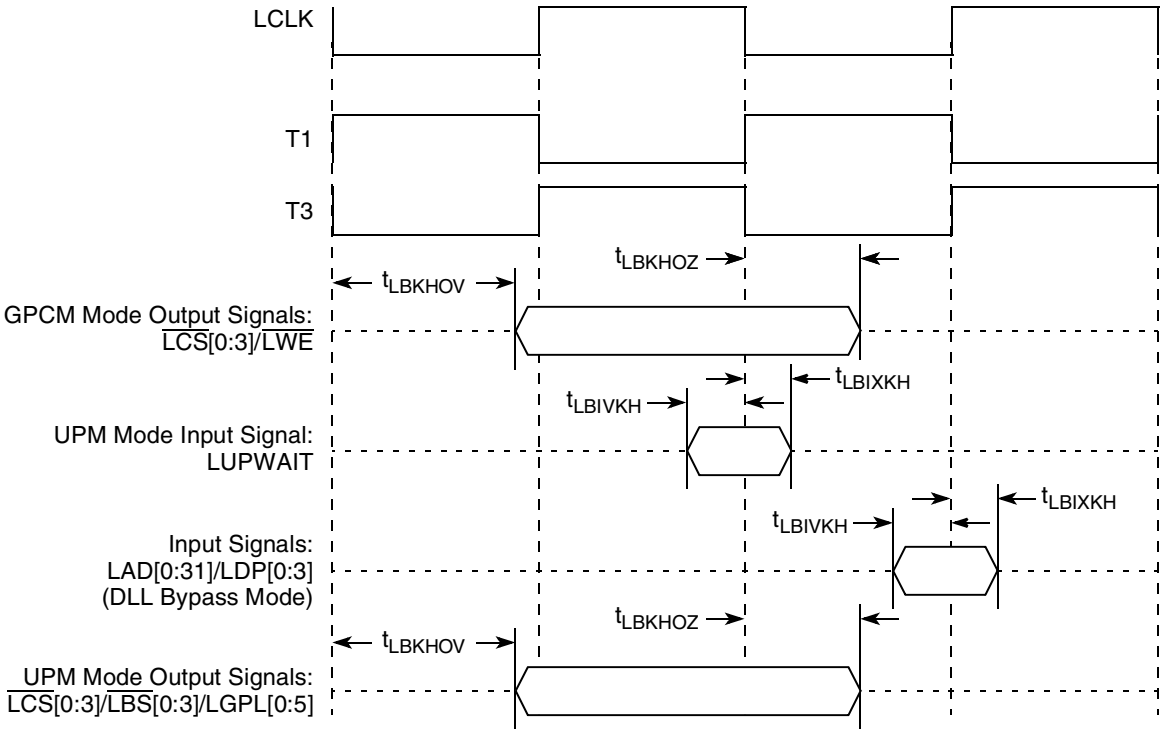

Figure 25. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (DLL Bypass Mode)

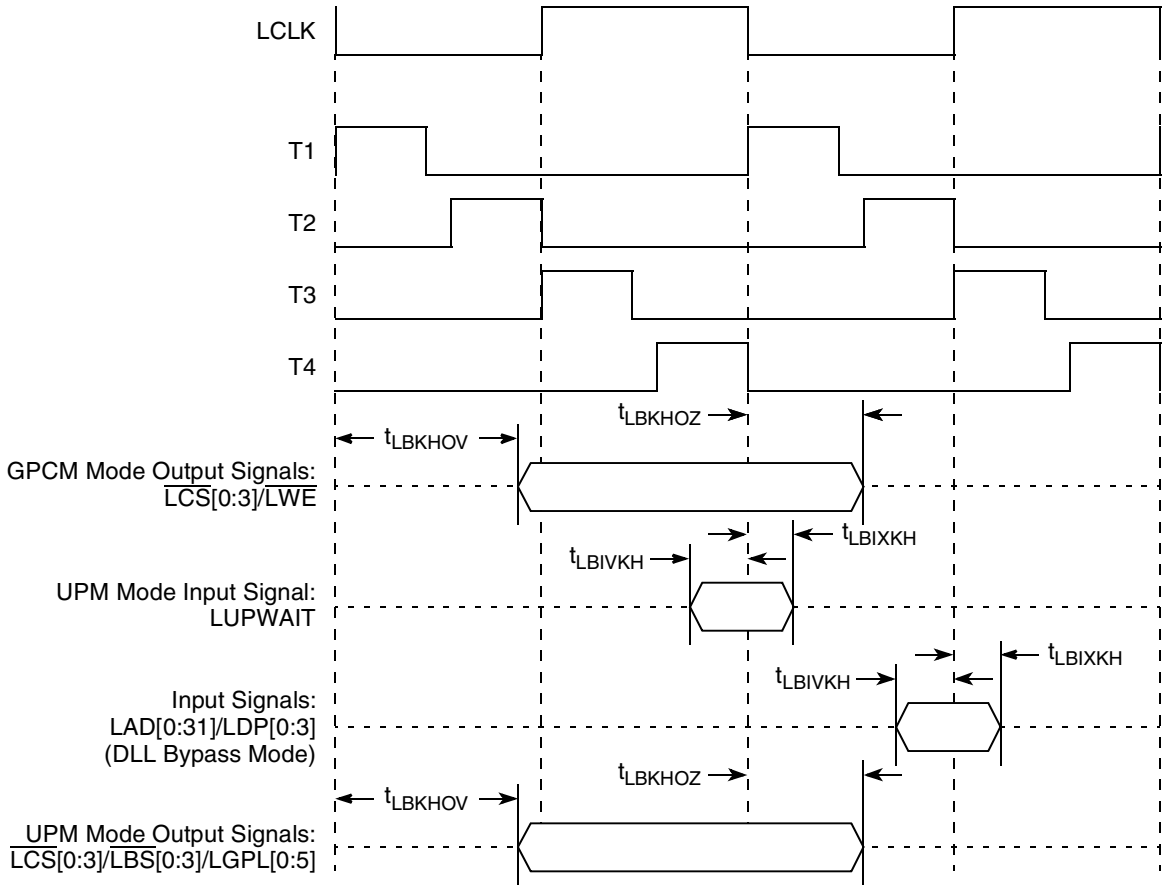

Figure 26. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (DLL Bypass Mode)

Figure 32 provides the test access port timing diagram.

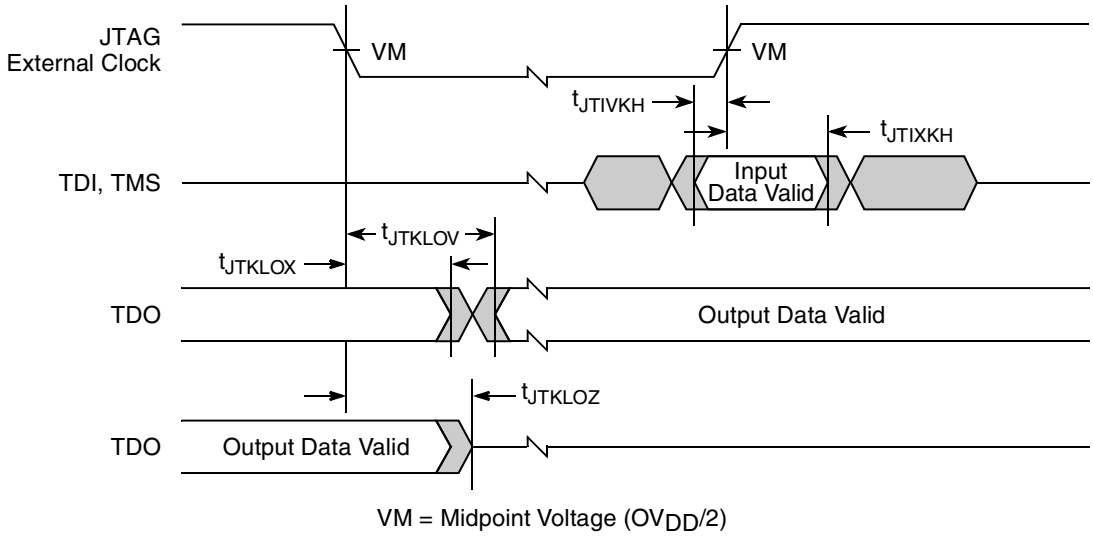

Figure 32. Test Access Port Timing Diagram

Figure 38 provides the AC test load for the timers.

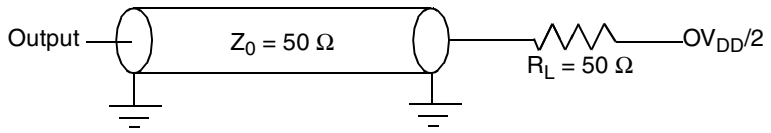

Figure 38. Timers AC Test Load

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8358E.

14.1 GPIO DC Electrical Characteristics

Table 50 provides the DC electrical characteristics for the device GPIO.

Table 50. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±10	μA	—

Note: This specification applies when operating from 3.3-V supply.

14.2 GPIO AC Timing Specifications

Table 51 provides the GPIO input and output AC timing specifications.

Table 51. GPIO Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Typ	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement must exclude any effect of mark on top surface of package.
6. Distance from the seating plane to the encapsulant material.

21.3 Pinout Listings

Refer to AN3097, “MPC8360/MPC8358E PowerQUICC Design Checklist,” for proper pin termination and usage.

Table 65 shows the pin list of the MPC8358E PBGA package.

Table 65. MPC8358E PBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Controller Interface				
MEMC_MDQ[0:63]	AD20, AG24, AF24, AH24, AF23, AE22, AH26, AD21, AH25, AD22, AF27, AB24, AG25, AC22, AE25, AC24, AD25, AB25, AC25, AG28, AD26, AE23, AG26, AC26, AD27, V25, AA28, AA25, Y26, W27, U24, W24, E28, H24, E26, D25, G27, H25, G26, F26, F27, F25, D26, F24, G25, E27, D27, C28, C27, F22, B26, F21, B28, E22, D24, C24, A25, E20, F20, D20, A23, C21, C23, E19	I/O	GV_{DD}	—
MEMC_MECC[0:7]	N26, N24, J26, H28, N28, P24, L26, K24	I/O	GV_{DD}	—
MEMC_MDM[0:8]	AG23, AD23, AE26, V28, G28, D28, D23, B24, U27	O	GV_{DD}	—
MEMC_MDQS[0:8]	AH23, AH27, AF28, T28, H26, E25, B25, A24, R28	I/O	GV_{DD}	—
MEMC_MBA[0:2]	V26, W28, Y28	O	GV_{DD}	—
MEMC_MA[0:14]	L25, M25, M24, K28, P28, T24, M27, R25, P25, L28, U26, M28, L27, K27, H27	O	GV_{DD}	—
MEMC_MODT[0:3]	AE21, AC19, E23, B23	—	GV_{DD}	6
$\overline{\text{MEMC\_MWE}}$	R27	O	GV_{DD}	—
$\overline{\text{MEMC\_MRAS}}$	W25	O	GV_{DD}	—
$\overline{\text{MEMC\_MCAS}}$	R24	O	GV_{DD}	—
$\overline{\text{MEMC\_MCS}}$[0:3]	T26, U28, J25, F28	O	GV_{DD}	—
MEMC_MCKE[0:1]	AD24, AE28	O	GV_{DD}	—
MEMC_MCK[0:5]	AG22, AG27, A26, C26, P26, E21	O	GV_{DD}	—
$\overline{\text{MEMC\_MCK}}$[0:5]	AF22, AF26, A27, B27, N27, D22	O	GV_{DD}	—
MDIC[0:1]	F19, AA27	I/O	GV_{DD}	11
PCI				
$\overline{\text{PCI\_INTA}}$/ PF[5]	R3	I/O	$LV_{DD}2$	2
$\overline{\text{PCI\_RESET\_OUT}}$/ PF[6]	P6	I/O	$LV_{DD}2$	—
PCI_AD[0:31]/ PG[0:31]	AB5, AC5, AG1, AA5, AF2, AD4, Y6, AF1, AE2, AC4, AD3, AE1, Y4, AC3, AD2, AD1, AB2, Y3, AA1, Y1, W1, V6, W3, V4, T5, W2, V5, V1, U4, V2, U2, T2	I/O	$LV_{DD}2$	—
$\overline{\text{PCI\_C\_BE}}$[0:3]/ PF[7:10]	Y5, AC2, Y2, U5	I/O	OV_{DD}	—

Table 72. QUICC Engine Block PLL Multiplication Factors (continued)

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF])
00101	0	× 5
00110	0	× 6
00111	0	× 7
01000	0	× 8
01001	0	× 9
01010	0	× 10
01011	0	× 11
01100	0	× 12
01101	0	× 13
01110	0	× 14
01111	0	× 15
10000	0	× 16
10001	0	× 17
10010	0	× 18
10011	0	× 19
10100	0	× 20
10101	0	× 21
10110	0	× 22
10111	0	× 23
11000	0	× 24
11001	0	× 25
11010	0	× 26
11011	0	× 27
11100	0	× 28
11101	0	× 29
11110	0	× 30
11111	0	× 31
00011	1	× 1.5
00101	1	× 2.5
00111	1	× 3.5
01001	1	× 4.5

Table 76 shows heat sinks and junction-to-ambient thermal resistance for PBGA package.

Table 76. Heat Sinks and Junction-to-Ambient Thermal Resistance of PBGA Package

Heat Sink Assuming Thermal Grease	Air Flow	29 × 29 mm PBGA
		Thermal Resistance
AAVID 30 × 30 × 9.4 mm Pin Fin	Natural Convection	12.6
AAVID 30 × 30 × 9.4 mm Pin Fin	1 m/s	8.2
AAVID 30 × 30 × 9.4 mm Pin Fin	2 m/s	7.0
AAVID 31 × 35 × 23 mm Pin Fin	Natural Convection	10.5
AAVID 31 × 35 × 23 mm Pin Fin	1 m/s	6.6
AAVID 31 × 35 × 23 mm Pin Fin	2 m/s	6.1
Wakefield, 53 × 53 × 25 mm Pin Fin	Natural Convection	9.0
Wakefield, 53 × 53 × 25 mm Pin Fin	1 m/s	5.6
Wakefield, 53 × 53 × 25 mm Pin Fin	2 m/s	5.1
MEI, 75 × 85 × 12 no adjacent board, extrusion	Natural Convection	9.0
MEI, 75 × 85 × 12 no adjacent board, extrusion	1 m/s	5.7
MEI, 75 × 85 × 12 no adjacent board, extrusion	2 m/s	5.1

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
473 Sapena Ct. #15
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

Figure 54 shows the PLL power supply filter circuit.

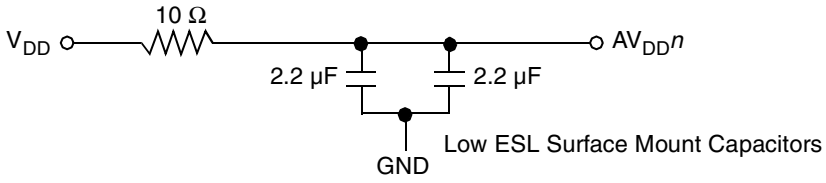

Figure 54. PLL Power Supply Filter Circuit

24.3 Decoupling Recommendations

Due to large address and data buses as well as high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the device system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pins of the device. These decoupling capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

24.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}, GV_{DD}, or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, and GND pins of the device.

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