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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	668-BBGA Exposed Pad
Supplier Device Package	668-PBGA-PGE (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8358ezqagdga

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) ± 5%.

Parameter[8]	Symbol[1]	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDKHME}	–0.6	0.9	ns	7

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. In the source synchronous mode, MCK/$\overline{\text{MCK}}$ can be shifted in ¼ applied cycle increments through the clock control register. For the skew measurements referenced for t_{AOSKEW} it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.
4. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.
5. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. In source synchronous mode, this will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *MPC8360E PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
6. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the device.
7. All outputs are referenced to the rising edge of MCK(n) at the pins of the device. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
8. AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.

Figure 6 shows the DDR SDRAM output timing for address skew with respect to any MCK.

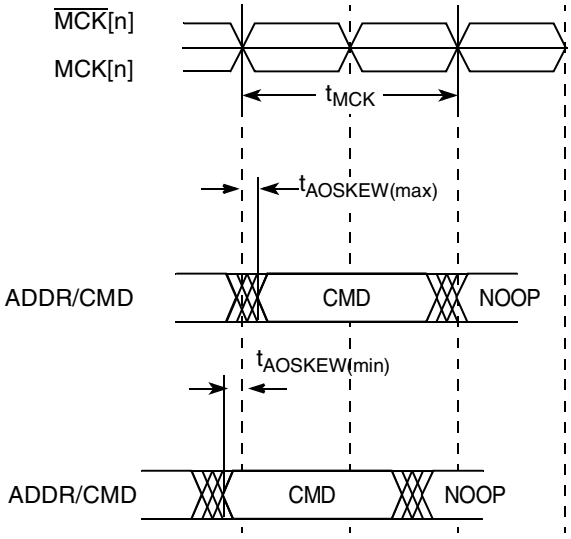


Figure 6. Timing Diagram for t_{AOSKEW} Measurement

Table 25. RGMII/RTBI DC Electrical Characteristics (when operating at 2.5 V)

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DD} = Min	2.00	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD} = Min	GND – 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DD} = Min	1.7	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	LV_{DD} = Min	–0.3	0.70	V
Input current	I_{IN}	$0 V \le V_{IN} \le LV_{DD}$		—	±10	μA

8.2 GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1 GMII Timing Specifications

This sections describe the GMII transmit and receive AC timing specifications.

8.2.1.1 GMII Transmit AC Timing Specifications

Table 26 provides the GMII transmit AC timing specifications.

Table 26. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns	—
GTX_CLK duty cycle	t_{GTXH}/t_{GTX}	40	—	60	%	—
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX} t_{GTKHDV}	0.5 —	—	— 5.0	ns	—
GTX_CLK clock rise time, (20% to 80%)	t_{GTXR}	—	—	1.0	ns	—
GTX_CLK clock fall time, (80% to 20%)	t_{GTXF}	—	—	1.0	ns	—
GTX_CLK125 clock period	t_{G125}	—	8.0	—	ns	2
GTX_CLK125 reference clock duty cycle measured at $LV_{DD/2}$	t_{G125H}/t_{G125}	45	—	55	%	2

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This symbol is used to represent the external GTX_CLK125 signal and does not follow the original symbol naming convention.

Figure 11 shows the MII transmit AC timing diagram.

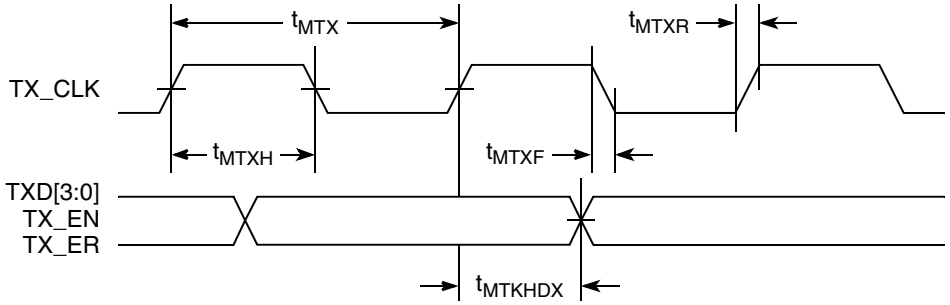


Figure 11. MII Transmit AC Timing Diagram

8.2.2.2 MII Receive AC Timing Specifications

Table 29 provides the MII receive AC timing specifications.

Table 29. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise time, (20% to 80%)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time, (80% to 20%)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 12 provides the AC test load.

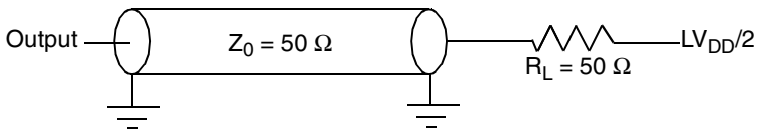


Figure 12. AC Test Load

Figure 17 shows the TBI transmit AC timing diagram.

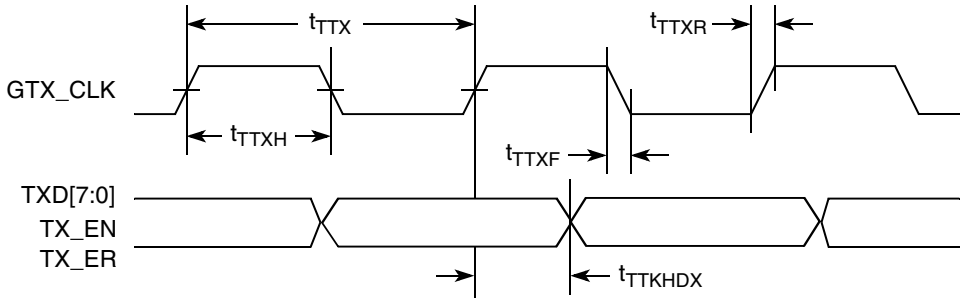


Figure 17. TBI Transmit AC Timing Diagram

8.2.4.2 TBI Receive AC Timing Specifications

Table 33 provides the TBI receive AC timing specifications.

Table 33. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
PMA_RX_CLK clock period	t_{TRX}	—	16.0	—	ns	—
PMA_RX_CLK skew	t_{SKTRX}	7.5	—	8.5	ns	—
RX_CLK duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%	—
RCG[9:0] setup time to rising PMA_RX_CLK	t_{TRDVKH}	2.5	—	—	ns	2
RCG[9:0] hold time to rising PMA_RX_CLK	t_{TRDXKH}	1.0	—	—	ns	2
RX_CLK clock rise time, V_{IL}(min) to V_{IH}(max)	t_{TRXR}	0.7	—	2.4	ns	—
RX_CLK clock fall time, V_{IH}(max) to V_{IL}(min)	t_{TRXF}	0.7	—	2.4	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. Setup and hold time of even numbered RCG are measured from riding edge of PMA_RX_CLK1. Setup and hold time of odd numbered RCG are measured from riding edge of PMA_RX_CLK0.

Figure 18 shows the TBI receive AC timing diagram.

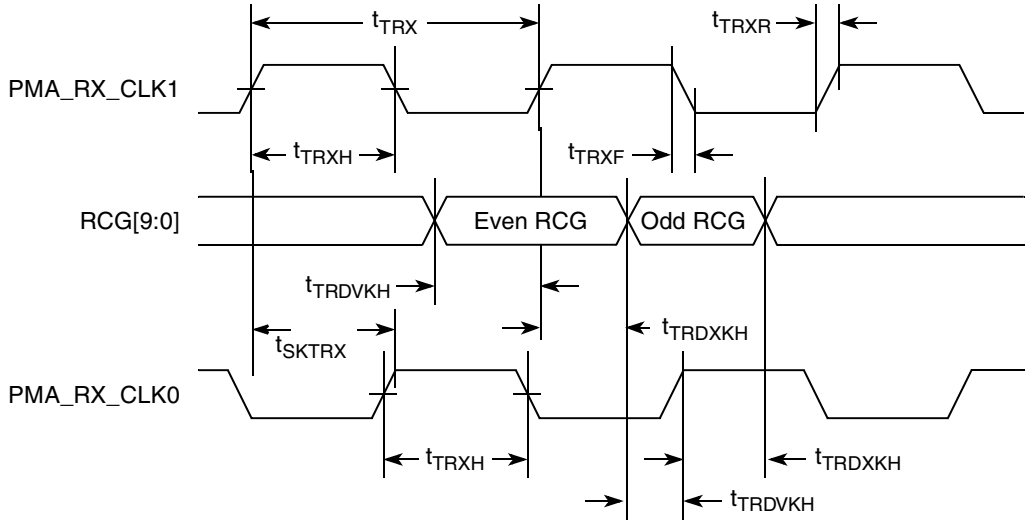


Figure 18. TBI Receive AC Timing Diagram

8.2.5 RGMII and RTBI AC Timing Specifications

Table 34 presents the RGMII and RTBI AC timing specifications.

Table 34. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	$t_{SKRGTKHDX}$ $t_{SKRGTKHDV}$	–0.5 —	—	— 0.5	ns	
Data to clock input skew (at receiver)	$t_{SKRGDXKH}$ $t_{SKRGDVKH}$	1.1 —	—	— 2.6	ns	2
Clock cycle duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 1000Base-T	t_{RGTH}/t_{RGT}	45	50	55	%	4, 5
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 5
Rise time (20–80%)	t_{RGTR}	—	—	0.75	ns	—
Fall time (20–80%)	t_{RGTF}	—	—	0.75	ns	—
GTX_CLK125 reference clock period	t_{G125}	—	8.0	—	ns	6

Figure 22 through Figure 27 show the local bus signals.

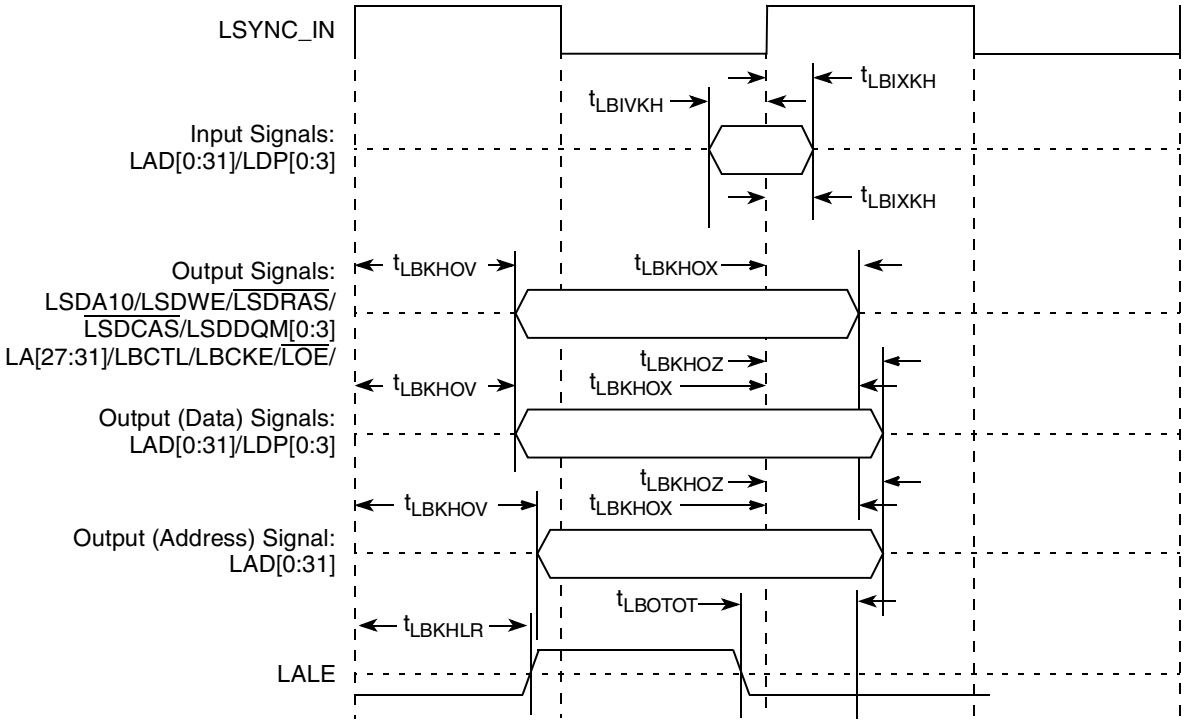


Figure 22. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)

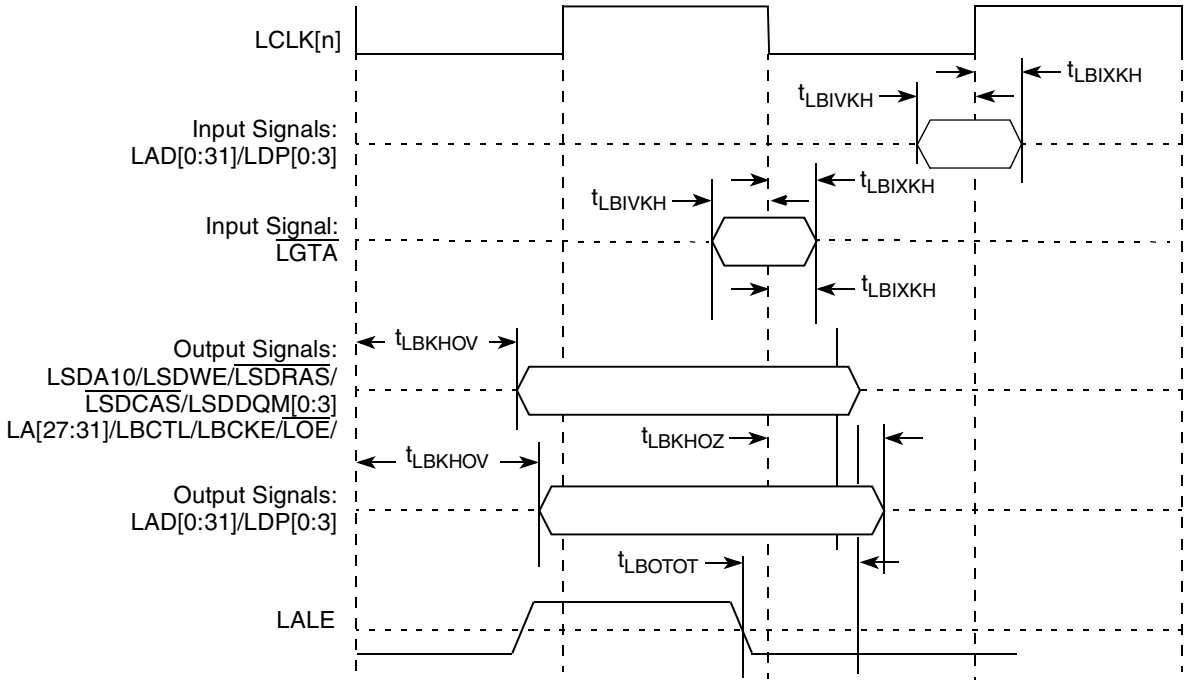


Figure 23. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)

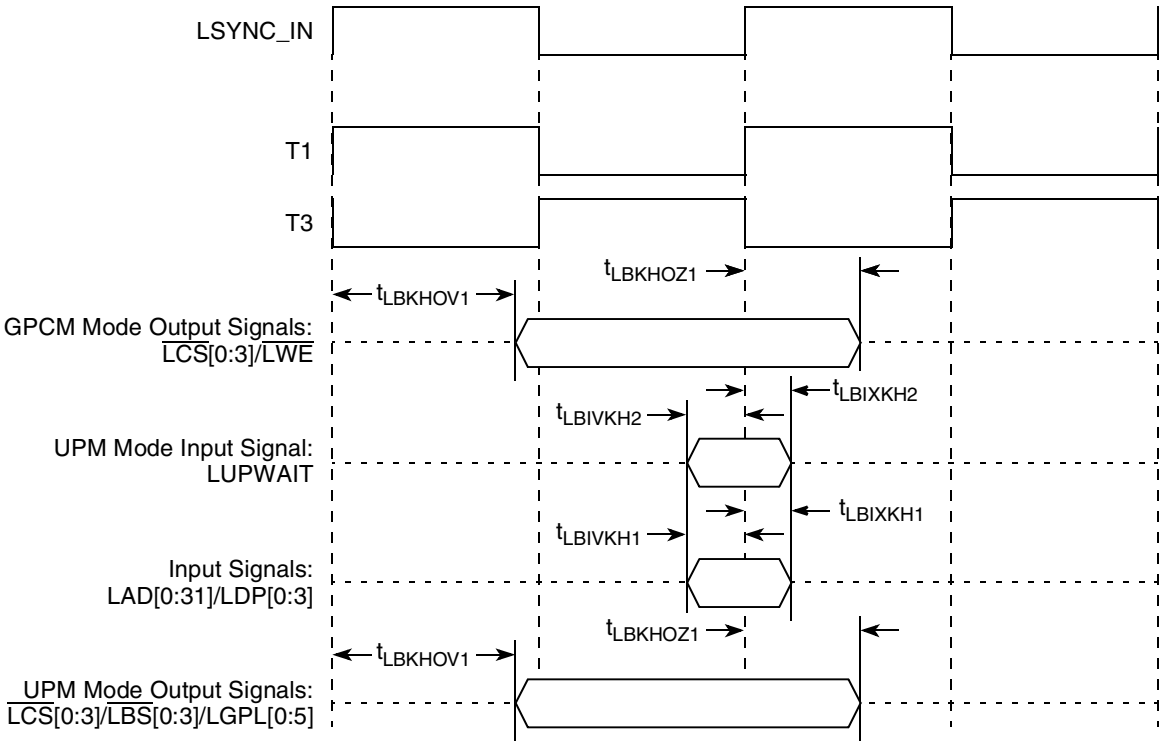


Figure 24. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (DLL Enabled)

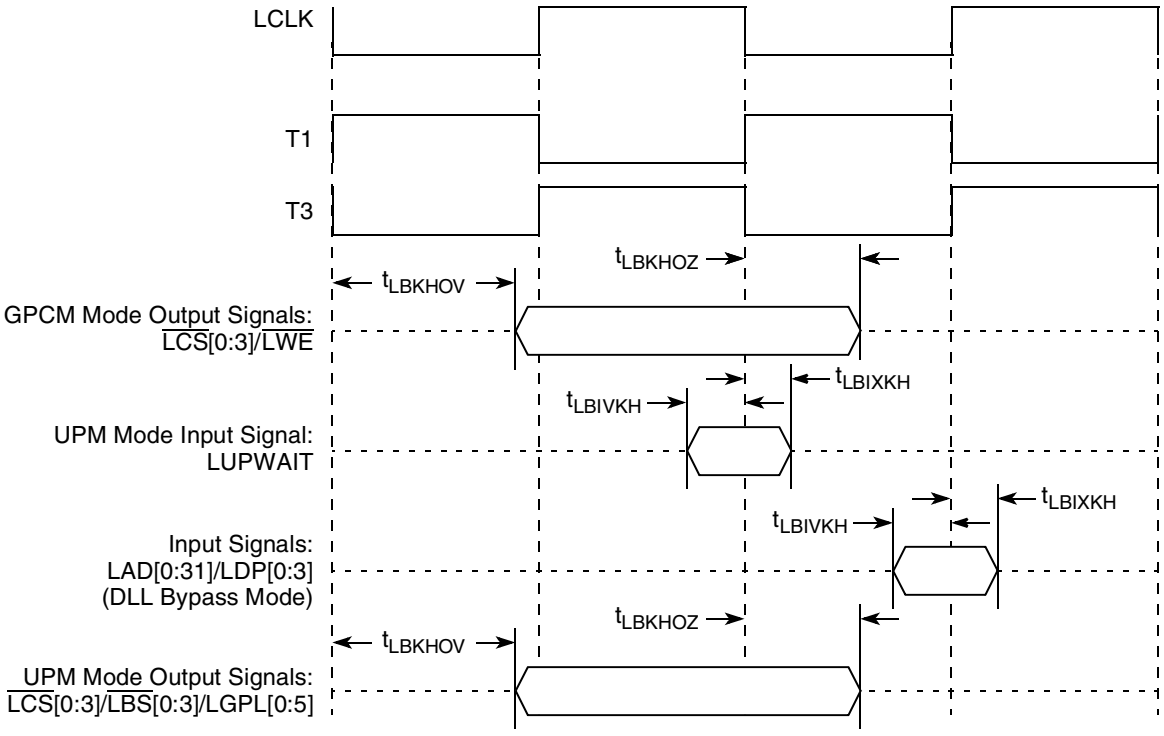


Figure 25. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (DLL Bypass Mode)

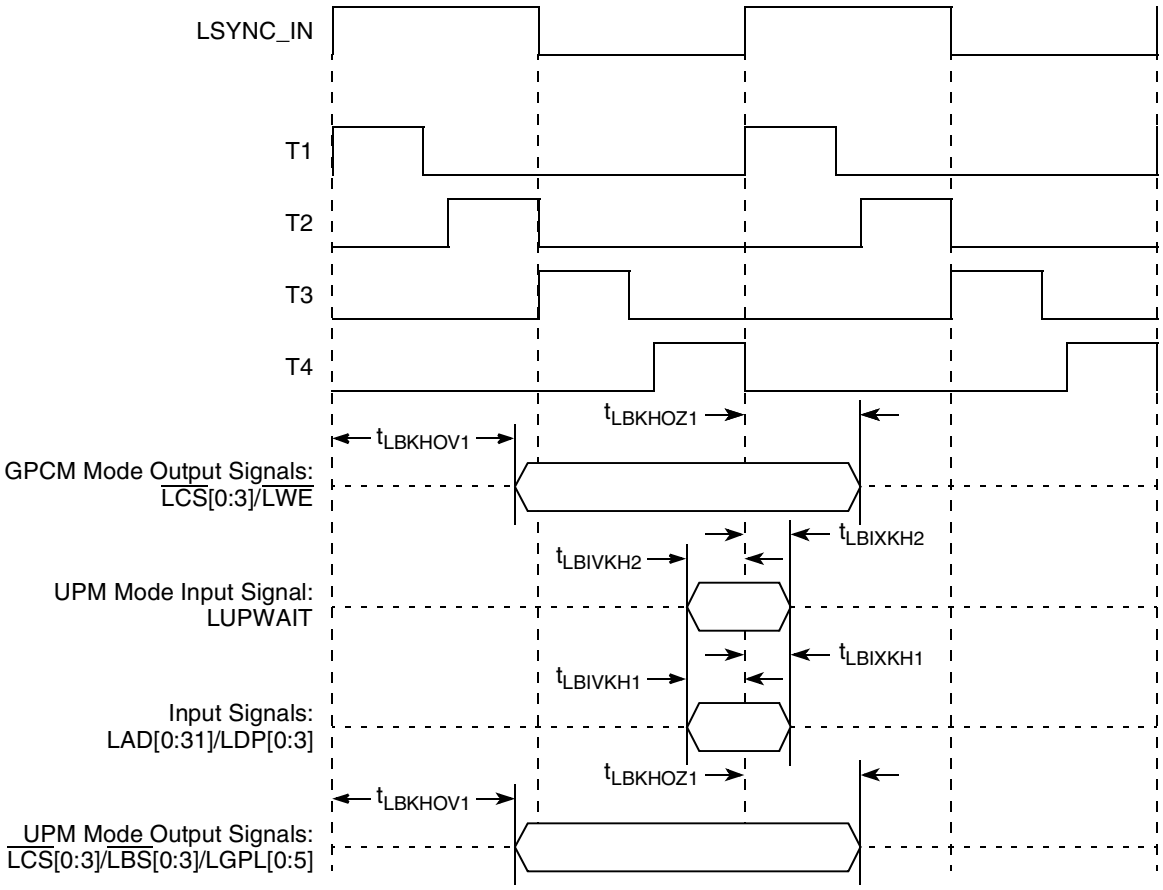


Figure 27. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (DLL Enabled)

10 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8358E.

10.1 JTAG DC Electrical Characteristics

Table 41 provides the DC electrical characteristics for the IEEE 1149.1 (JTAG) interface of the device.

Table 41. JTAG interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.5	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±10	μA

11 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8358E.

11.1 I²C DC Electrical Characteristics

Table 43 provides the DC electrical characteristics for the I²C interface of the device.

Table 43. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	0.4	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current ($0 V \le V_{IN} \le OV_{DD}$)	I_{IN}	—	±10	µA	4

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8360E Integrated Communications Processor Family Reference Manual* for information on the digital filter used.
4. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

11.2 I²C AC Electrical Specifications

Table 44 provides the AC timing parameters for the I²C interface of the device.

Table 44. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 43).

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	µs
High period of the SCL clock	t_{I2CH}	0.6	—	µs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	µs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	µs
Data setup time	t_{I2DVKH}	100	—	ns

Table 44. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 43).

Parameter	Symbol[1]	Min	Max	Unit
Data hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0[2]	 — 0.9[3]	µs
Rise time of both SDA and SCL signals	t_{I2CR}	20 + 0.1 C_b[4]	300	ns
Fall time of both SDA and SCL signals	t_{I2CF}	20 + 0.1 C_b[4]	300	ns
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The device provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.

Figure 33 provides the AC test load for the I²C.

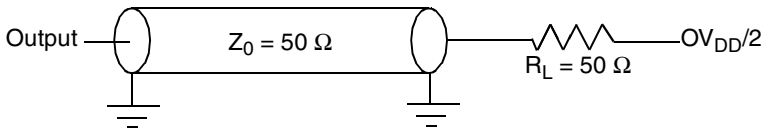


Figure 33. I²C AC Test Load

Figure 34 shows the AC timing diagram for the I²C bus.

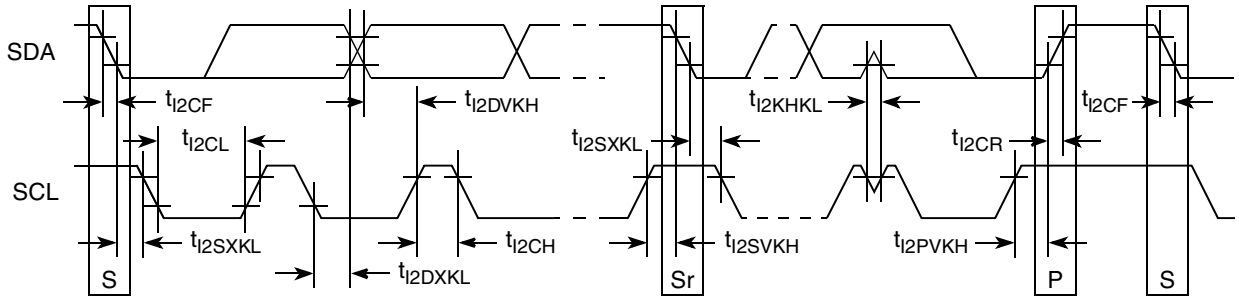


Figure 34. I²C Bus AC Timing Diagram

Figure 38 provides the AC test load for the timers.

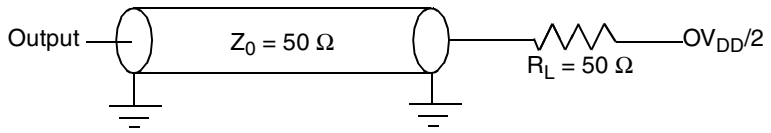


Figure 38. Timers AC Test Load

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8358E.

14.1 GPIO DC Electrical Characteristics

Table 50 provides the DC electrical characteristics for the device GPIO.

Table 50. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±10	μA	—

Note: This specification applies when operating from 3.3-V supply.

14.2 GPIO AC Timing Specifications

Table 51 provides the GPIO input and output AC timing specifications.

Table 51. GPIO Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Typ	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Figure 39 provides the AC test load for the GPIO.

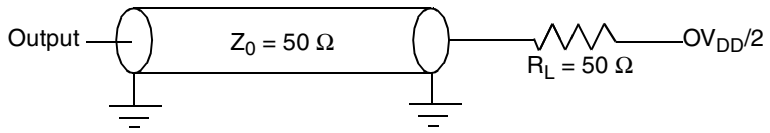


Figure 39. GPIO AC Test Load

15 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8358E.

15.1 IPIC DC Electrical Characteristics

Table 52 provides the DC electrical characteristics for the external interrupt pins of the IPIC.

Table 52. IPIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±10	μA
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:
1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ\_OUT}}$, $\overline{\text{MCP\_OUT}}$, and CE ports Interrupts.
2. $\overline{\text{IRQ\_OUT}}$ and $\overline{\text{MCP\_OUT}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

15.2 IPIC AC Timing Specifications

Table 53 provides the IPIC input and output AC timing specifications.

Table 53. IPIC Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

16 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8358E.

16.1 SPI DC Electrical Characteristics

Table 54 provides the DC electrical characteristics for the device SPI.

Table 54. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±10	μA

16.2 SPI AC Timing Specifications

Table 55 and provide the SPI input and output AC timing specifications.

Table 55. SPI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	t_{NIKHOX} t_{NIKHOV}	0.4 —	— 8	ns
SPI outputs—Slave mode (external clock) delay	t_{NEKHOX} t_{NEKHOV}	2 —	— 8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	8	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

Figure 40 provides the AC test load for the SPI.

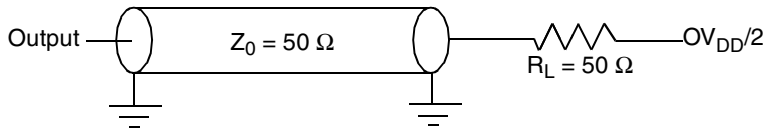


Figure 40. SPI AC Test Load

Table 56. TDM/SI DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±10	μA

17.2 TDM/SI AC Timing Specifications

Table 57 provides the TDM/SI input and output AC timing specifications.

Table 57. TDM/SI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max[3]	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	10	ns
TDM/SI outputs—External clock high impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
3. Timings are measured from the positive or negative edge of the clock, according to SIxMR [CE] and SITXCEI[TXCEIx]. See the *MPC8360E Integrated Communications Processor Family Reference Manual* for more details.

Figure 43 provides the AC test load for the TDM/SI.

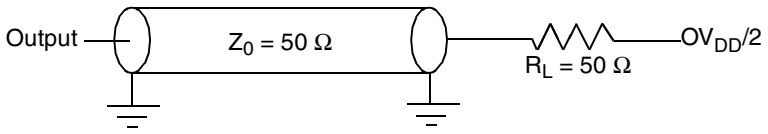


Figure 43. TDM/SI AC Test Load

Figure 44 represents the AC timing from Table 55. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 47 shows the UTOPIA timing with internal clock.

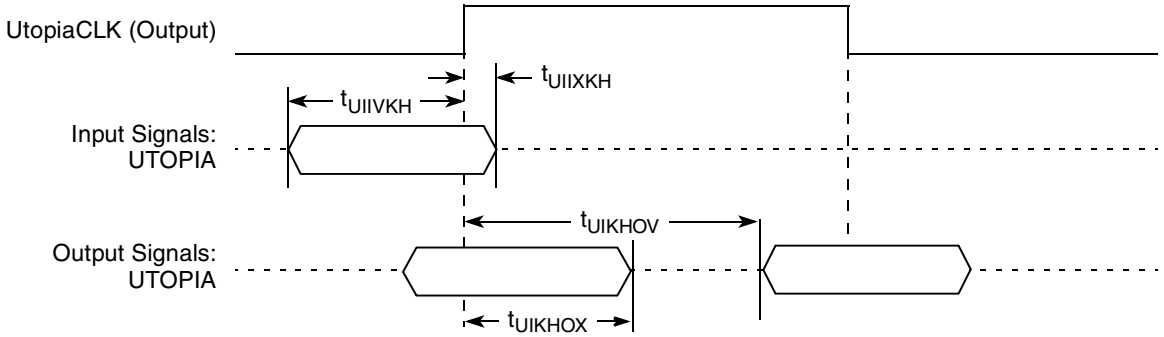


Figure 47. UTOPIA AC Timing (Internal Clock) Diagram

19 HDLC, BISYNC, Transparent, and Synchronous UART

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), BISYNC, transparent, and synchronous UART protocols of the MPC8358E.

19.1 HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

Table 60 provides the DC electrical characteristics for the device HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 60. HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±10	μA

19.2 HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

Table 61 and Table 62 provide the input and output AC timing specifications for HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 61. HDLC, BISYNC, and Transparent AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—Internal clock delay	t_{HIKHOV}	0	11.2	ns
Outputs—External clock delay	t_{HEKHOV}	1	10.8	ns
Outputs—Internal clock high impedance	t_{HIKHOX}	-0.5	5.5	ns
Outputs—External clock high impedance	t_{HEKHOX}	1	8	ns
Inputs—Internal clock input setup time	t_{HIIVKH}	8.5	—	ns
Inputs—External clock input setup time	t_{HEIVKH}	4	—	ns
Inputs—Internal clock input hold time	t_{HIIXKH}	1.4	—	ns
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Table 62. Synchronous UART AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—Internal clock delay	$t_{UAIKHOV}$	0	11.3	ns
Outputs—External clock delay	$t_{UAEKHOV}$	1	14	ns
Outputs—Internal clock high impedance	$t_{UAIKHOX}$	0	11	ns
Outputs—External clock high impedance	$t_{UAEKHOX}$	1	14	ns
Inputs—Internal clock input setup time	$t_{UAIIVKH}$	6	—	ns
Inputs—External clock input setup time	$t_{UAEIVKH}$	8	—	ns
Inputs—Internal clock input hold time	$t_{UAIIXKH}$	1	—	ns
Inputs—External clock input hold time	$t_{UAEIXKH}$	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 48 provides the AC test load.

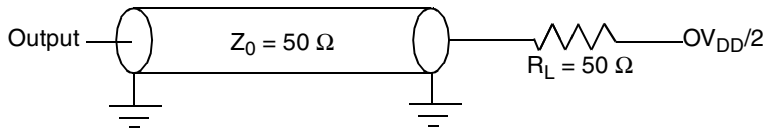
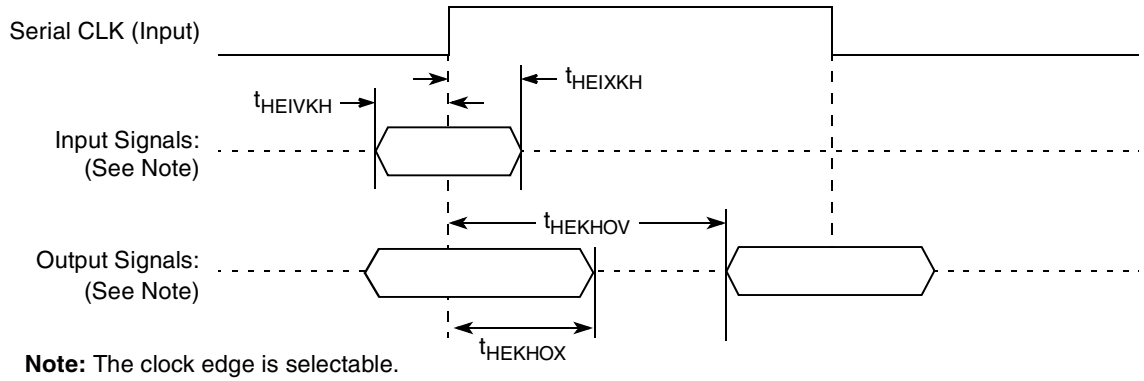


Figure 48. AC Test Load

19.3 AC Test Load

Figure 49 and Figure 50 represent the AC timing from Table 61 and Table 62. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

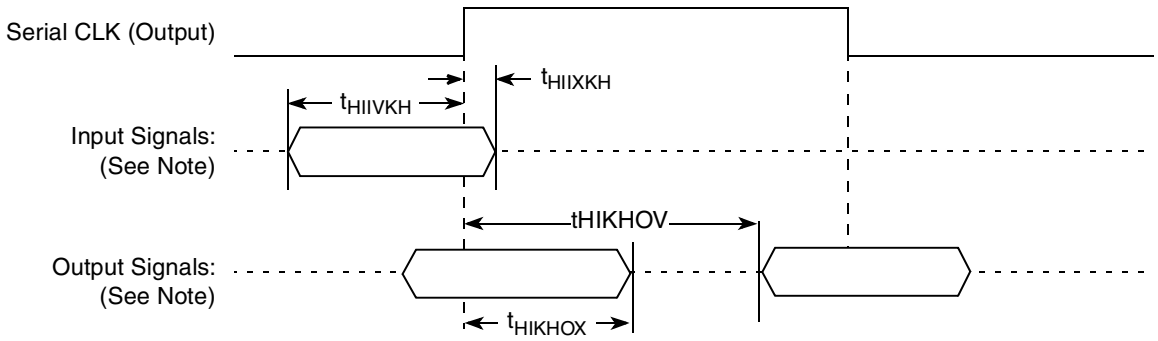
Figure 49 shows the timing with external clock.



Note: The clock edge is selectable.

Figure 49. AC Timing (External Clock) Diagram

Figure 50 shows the timing with internal clock.



Note: The clock edge is selectable.

Figure 50. AC Timing (Internal Clock) Diagram

Note that *lb_clk* is not the external local bus or DDRC2 frequency; *lb_clk* passes through the a LB clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK[0:2]). The LB clock divider ratio is controlled by LCRR[CLKDIV].

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 66 specifies which units have a configurable clock frequency.

Table 66. Configurable Clock Units

Unit	Default Frequency	Options
Security core	*csb_clk*/3	Off, *csb_clk*[1], *csb_clk*/2, *csb_clk*/3
PCI and DMA complex	csb_clk	Off, *csb_clk*

1 With limitation, only for slow csb_clk rates, up to 166 MHz.

Table 67 provides the operating frequencies for the PBGA package under recommended operating conditions (see Table 2). All frequency combinations shown in the table below may not be available. Maximum operating frequencies depend on the part ordered, see Section 25.1, "Part Numbers Fully Addressed by this Document," for part ordering details and contact your Freescale sales representative or authorized distributor for more information.

Table 67. Operating Frequencies for the PBGA Package

Characteristic[1]	400 MHz	Unit
e300 core frequency (*core_clk*)	266–400	MHz
Coherent system bus frequency (*csb_clk*)	133–266	MHz
QUICC Engine frequency (*ce_clk*)	266–400	MHz
DDR and DDR2 memory bus frequency (MCLK)[2]	100–133	MHz
Local bus frequency (LCLK*n*)[3]	16.67–133	MHz
PCI input frequency (CLKIN or PCI_CLK)	25–66.67	MHz
Security core maximum internal operating frequency	133	MHz

1 The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.

2 The DDR data rate is 2x the DDR memory bus frequency.

3 The local bus frequency is 1/2, 1/4, or 1/8 of the *lb_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBCM]).

- To configure the device with CSB clock rate of 266 MHz, core rate of 400 MHz, and QUICC Engine clock rate 300 MHz while the input clock rate is 33 MHz. Conf No. ‘s10’ and ‘c1’ are selected from Table 74. SPMF is 1000, CORPLL is 0000011, CEPMF is 01001, and CEPDF is 0.

23 Thermal

This section describes the thermal specifications of the MPC8358E.

23.1 Thermal Characteristics

Table 75 provides the package thermal characteristics for the 668 29 mm x 29 mm PBGA package.

Table 75. Package Thermal Characteristics for the PBGA Package

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection on single layer board (1s)	$R_{\theta JA}$	20	°C/W	1, 2
Junction-to-ambient Natural Convection on four layer board (2s2p)	$R_{\theta JA}$	14	°C/W	1, 2, 3
Junction-to-ambient (@1 m/s) on single layer board (1s)	$R_{\theta JMA}$	15	°C/W	1, 3
Junction-to-ambient (@ 1 m/s) on four layer board (2s2p)	$R_{\theta JMA}$	11	•C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	6	•C/W	4
Junction-to-case thermal	$R_{\theta JC}$	4	•C/W	5
Junction-to-Package Natural Convection on Top	Ψ_{JT}	4	•C/W	6

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 and JEDEC JESD51-9 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal. 1 m/sec is approximately equal to 200 linear feet per minute (LFM).
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

23.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers. See Table 5 for typical power dissipations values.

23.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)
T_T = thermocouple temperature on top of package (°C)
Ψ_{JT} = junction-to-ambient thermal resistance (°C/W)
P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

23.2.4 Heat Sinks and Junction-to-Ambient Thermal Resistance

In some application environments, a heat sink will be required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, airflow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.