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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	668-BBGA Exposed Pad
Supplier Device Package	668-PBGA-PGE (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8358zqagdda

— Advanced encryption standard unit (AESU)
— Implements the Rinjdael symmetric key cipher
— Key lengths of 128, 192, and 256 bits, two key
  – ECB, CBC, CCM, and counter modes
— ARC four execution unit (AFEU)
  – Implements a stream cipher compatible with the RC4 algorithm
  – 40- to 128-bit programmable key
— Message digest execution unit (MDEU)
  – SHA with 160-, 224-, or 256-bit message digest
  – MD5 with 128-bit message digest
  – HMAC with either SHA or MD5 algorithm
— Random number generator (RNG)
— Four crypto-channels, each supporting multi-command descriptor chains
  – Static and/or dynamic assignment of crypto-execution units via an integrated controller
  – Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
— Storage/NAS XOR parity generation accelerator for RAID applications

- DDR SDRAM memory controller on the MPC8358E

— Programmable timing supporting both DDR1 and DDR2 SDRAM
— On the MPC8358E, the DDR bus can be configured as a 32- or 64-bit bus
— 32- or 64-bit data interface, up to 266 MHz (for the MPC8358E) data rate
— Four banks of memory, each up to 1 Gbyte
— DRAM chip configurations from 64 Mbits to 1 Gigabit with ×8/×16 data ports
— Full ECC support
— Page mode support (up to 16 simultaneous open pages for DDR1, up to 32 simultaneous open pages for DDR2)
— Contiguous or discontiguous memory mapping
— Read-modify-write support
— Sleep mode support for self refresh SDRAM
— Supports auto refreshing
— Supports source clock mode
— On-the-fly power management using CKE
— Registered DIMM support
— 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2
— External driver impedance calibration
— On-die termination (ODT)

- PCI interface

— PCI Specification Revision 2.3 compatible

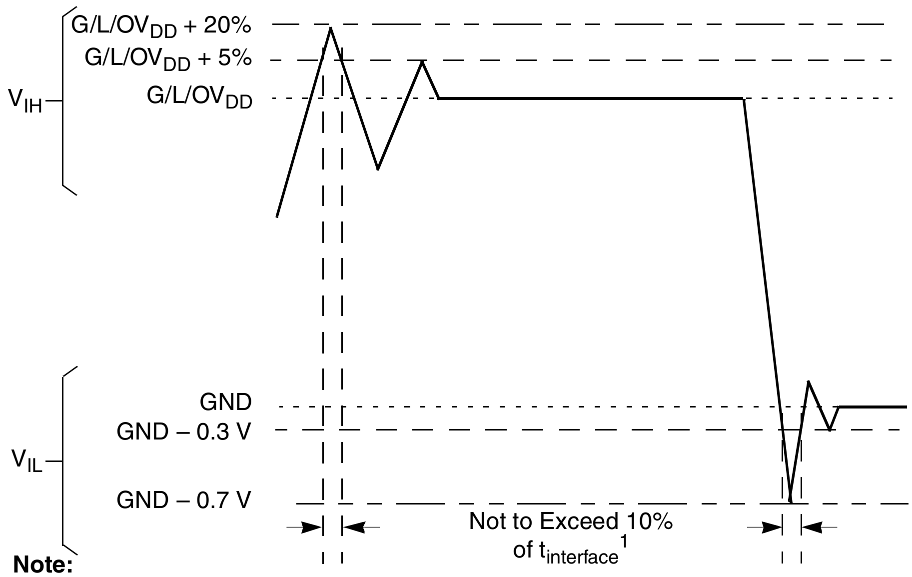
- Multiple master support
- Master or slave I^2C mode support
- On-chip digital filtering rejects spikes on the bus
- System initialization data is optionally loaded from I^2C-1 EPROM by boot sequencer embedded hardware

- DMA controller
  - Four independent virtual channels
  - Concurrent execution across multiple channels with programmable bandwidth control
  - All channels accessible by local core and remote PCI masters
  - Misaligned transfer capability
  - Data chaining and direct mode
  - Interrupt on completed segment and chain
  - DMA external handshake signals: $\overline{\text{DMA\_DREQ}}$[0:3]/$\overline{\text{DMA\_DACK}}$[0:3]/$\overline{\text{DMA\_DONE}}$[0:3]. There is one set for each DMA channel. The pins are multiplexed to the parallel IO pins with other QE functions.
- DUART
  - Two 4-wire interfaces (RxD, TxD, RTS, CTS)
  - Programming model compatible with the original 16450 UART and the PC16550D
- System timers
  - Periodic interrupt timer
  - Real-time clock
  - Software watchdog timer
  - Eight general-purpose timers
- IEEE Std. 1149.1™-compliant, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8358E. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the device.



Note:
1. Note that $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the device for the 3.3-V signals, respectively.

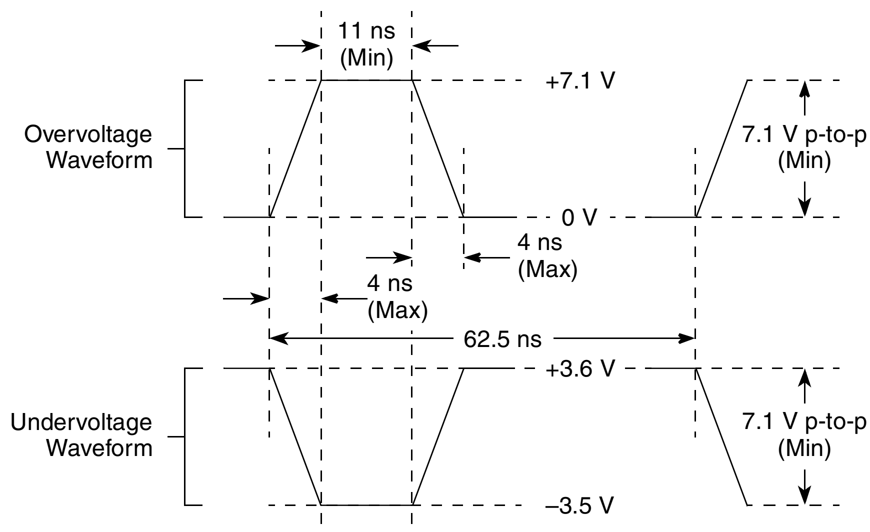


Figure 3. Maximum AC Waveforms on PCI interface for 3.3-V Signaling

Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications Mode

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
MDQS—MDQ/MECC input skew per byte 266 MHz 200 MHz	t_{DISKEW}	 –1125 –1250	 1125 1250	ps	1, 2

Notes:

1. AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.
2. Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 ≤ n ≤ 7) or ECC (MECC[{0...7}] if n = 8).

Figure 5 shows the input timing diagram for the DDR controller.

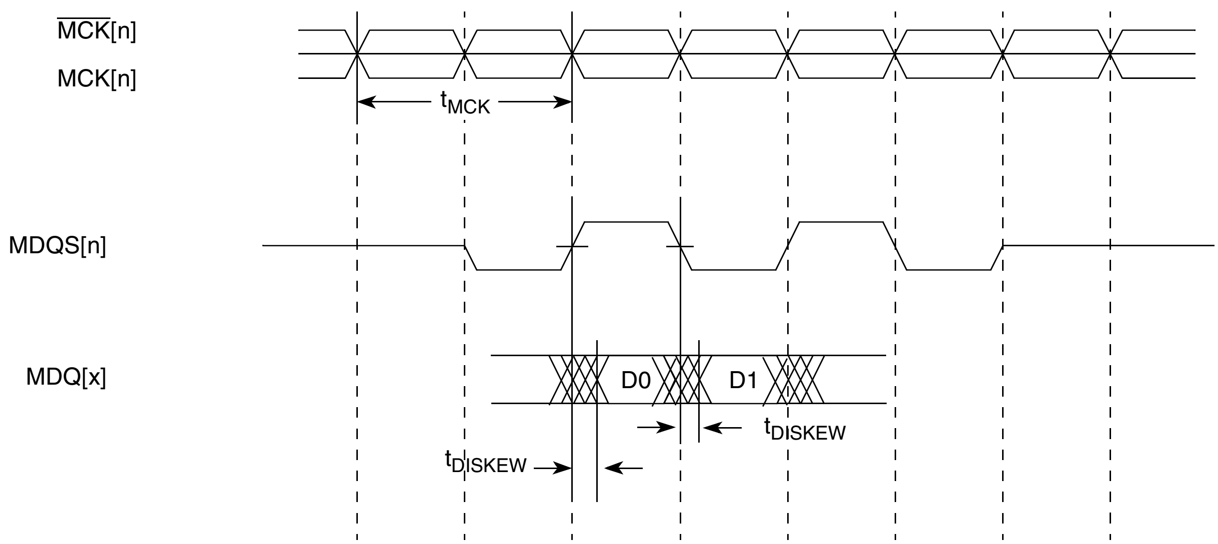


Figure 5. DDR Input Timing Diagram

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20 and Table 21 provide the output AC timing specifications and measurement conditions for the DDR and DDR2 SDRAM interface.

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) ± 5%.

Parameter[8]	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time, (MCK[n]/$\overline{MCK}$[n] crossing)	t_{MCK}	6	10	ns	2
Skew between any MCK to ADDR/CMD 266 MHz 200 MHz	t_{AOSKEW}	 –1.1 –1.2	 0.3 0.4	ns	3

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) ± 5%.

Parameter[8]	Symbol[1]	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDKHME}	–0.6	0.9	ns	7

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. In the source synchronous mode, MCK/$\overline{\text{MCK}}$ can be shifted in ¼ applied cycle increments through the clock control register. For the skew measurements referenced for t_{AOSKEW} it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.
4. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.
5. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. In source synchronous mode, this will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *MPC8360E PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
6. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the device.
7. All outputs are referenced to the rising edge of MCK(n) at the pins of the device. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
8. AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.

Figure 6 shows the DDR SDRAM output timing for address skew with respect to any MCK.

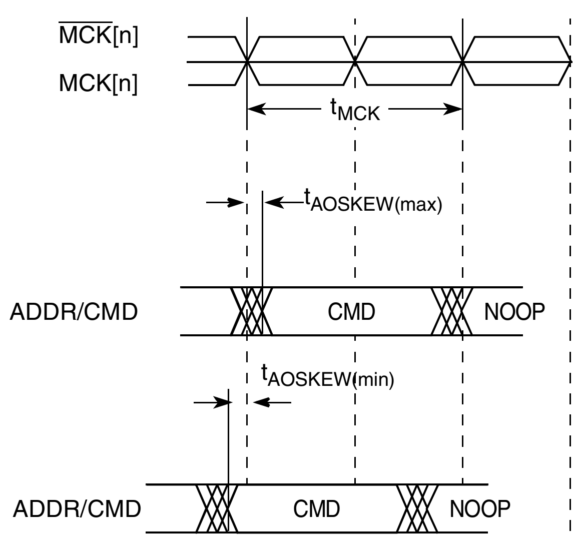


Figure 6. Timing Diagram for t_{AOSKEW} Measurement

8.1 Three-Speed Ethernet Controller (10/100/1000 Mbps)—GMII/MII/RMII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), MII (media independent interface), RMII (reduced media independent interface), TBI (ten-bit interface), RGMII (reduced gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The MII, RMII, GMII, and TBI interfaces are only defined for 3.3 V, while the RGMII and RTBI interfaces are only defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for the MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

8.1.1 10/100/1000 Ethernet DC Electrical Characteristics

The electrical characteristics specified here apply to media independent interface (MII), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), reduced media independent interface (RMII) signals, management data input/output (MDIO) and management data clock (MDC).

The MII and RMII interfaces are defined for 3.3 V, while the RGMII and RTBI interfaces can be operated at 2.5 V. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3*. The RMII interface follows the *RMII Consortium RMII Specification Version 1.2*.

Table 24. RGMII/RTBI, GMII, TBI, MII, and RMII DC Electrical Characteristics (when operating at 3.3 V)

Parameter	Symbol	Conditions		Min	Max	Unit	Notes
Supply voltage 3.3 V	LV_{DD}	—		2.97	3.63	V	1
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	LV_{DD} = Min	2.40	LV_{DD} + 0.3	V	—
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	LV_{DD} = Min	GND	0.50	V	—
Input high voltage	V_{IH}	—	—	2.0	LV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	—	—	–0.3	0.90	V	—
Input current	I_{IN}	$0 V \le V_{IN} \le LV_{DD}$		—	±10	μA	—

Note:

1. GMII/MII pins that are not needed for RGMII, RMII, or RTBI operation are powered by the OV_{DD} supply.

Table 25. RGMII/RTBI DC Electrical Characteristics (when operating at 2.5 V)

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0$ mA	LV_{DD} = Min	2.00	$LV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0$ mA	LV_{DD} = Min	GND – 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DD} = Min	1.7	$LV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	LV_{DD} = Min	–0.3	0.70	V
Input current	I_{IN}	$0\ V \le V_{IN} \le LV_{DD}$		—	±10	μA

8.2 GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1 GMII Timing Specifications

This sections describe the GMII transmit and receive AC timing specifications.

8.2.1.1 GMII Transmit AC Timing Specifications

Table 26 provides the GMII transmit AC timing specifications.

Table 26. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns	—
GTX_CLK duty cycle	$t_{GTXH/tGTX}$	40	—	60	%	—
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX} t_{GTKHDV}	0.5 —	—	— 5.0	ns	—
GTX_CLK clock rise time, (20% to 80%)	t_{GTXR}	—	—	1.0	ns	—
GTX_CLK clock fall time, (80% to 20%)	t_{GTXF}	—	—	1.0	ns	—
GTX_CLK125 clock period	t_{G125}	—	8.0	—	ns	2
GTX_CLK125 reference clock duty cycle measured at $LV_{DD/2}$	t_{G125H}/t_{G125}	45	—	55	%	2

Notes:

1. The symbols used for timing specifications follow the pattern $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This symbol is used to represent the external GTX_CLK125 signal and does not follow the original symbol naming convention.

Figure 9 shows the GMII transmit AC timing diagram.

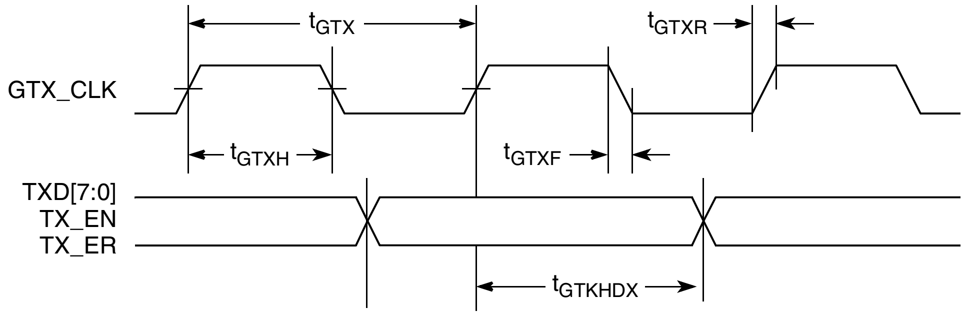


Figure 9. GMII Transmit AC Timing Diagram

8.2.1.2 GMII Receive AC Timing Specifications

Table 27 provides the GMII receive AC timing specifications.

Table 27. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
RX_CLK clock period	t_{GRX}	—	8.0	—	ns	—
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	%	—
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns	—
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.3	—	—	ns	—
RX_CLK clock rise time, (20% to 80%)	t_{GRXR}	—	—	1.0	ns	—
RX_CLK clock fall time, (80% to 20%)	t_{GRXF}	—	—	1.0	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 14 shows the RMII transmit AC timing diagram.

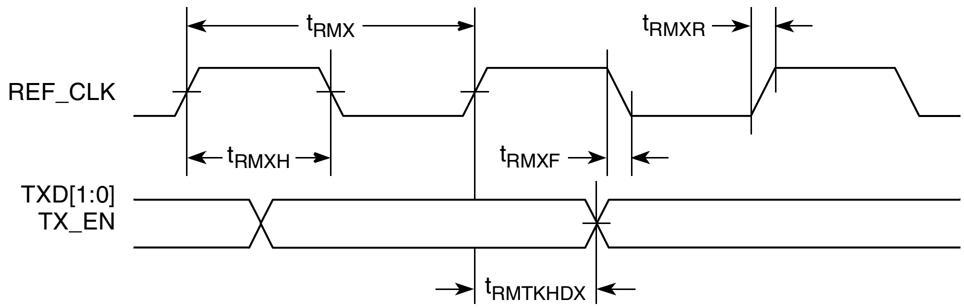


Figure 14. RMII Transmit AC Timing Diagram

8.2.3.2 RMII Receive AC Timing Specifications

Table 31 provides the RMII receive AC timing specifications.

Table 31. RMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise time	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 15 provides the AC test load.

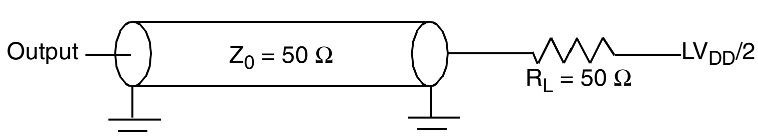


Figure 15. AC Test Load

Figure 18 shows the TBI receive AC timing diagram.

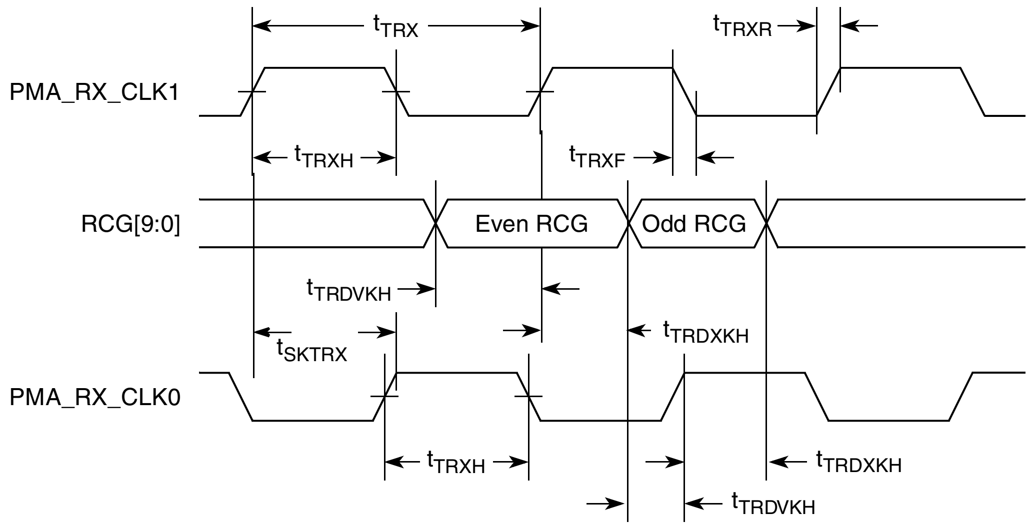


Figure 18. TBI Receive AC Timing Diagram

8.2.5 RGMII and RTBI AC Timing Specifications

Table 34 presents the RGMII and RTBI AC timing specifications.

Table 34. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	$t_{SKRGTKHDX}$ $t_{SKRGTKHDV}$	–0.5 —	—	— 0.5	ns	
Data to clock input skew (at receiver)	$t_{SKRGDXKH}$ $t_{SKRGDVKH}$	1.1 —	—	— 2.6	ns	2
Clock cycle duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 1000Base-T	t_{RGTH}/t_{RGT}	45	50	55	%	4, 5
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 5
Rise time (20–80%)	t_{RGTR}	—	—	0.75	ns	—
Fall time (20–80%)	t_{RGTF}	—	—	0.75	ns	—
GTX_CLK125 reference clock period	t_{G125}	—	8.0	—	ns	6

Table 36. MII Management AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} is 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC fall time	t_{MDHF}	—	—	10	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, $t_{MDRDVKH}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
3. This parameter is dependent on the ce_clk speed (that is, for a ce_clk of 200 MHz, the delay is 90 ns and for a ce_clk of 300 MHz, the delay is 63 ns).

Figure 20 shows the MII management AC timing diagram.

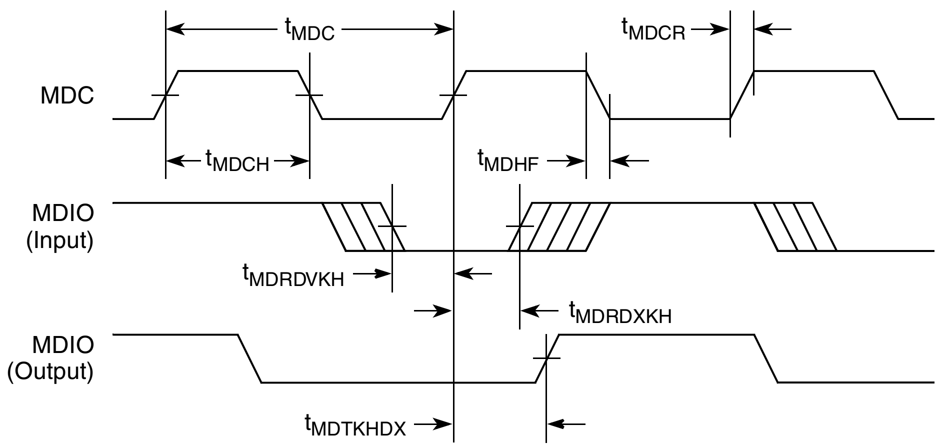


Figure 20. MII Management Interface Timing Diagram

8.3.3 IEEE 1588 Timer AC Specifications

Table 37 provides the IEEE 1588 timer AC specifications.

Table 37. IEEE 1588 Timer AC Specifications

Parameter	Symbol	Min	Max	Unit	Notes
Timer clock frequency	t_{TMRCK}	0	70	MHz	1
Input setup to timer clock	t_{TMRCKS}	—	—	—	2, 3
Input hold from timer clock	t_{TMRCKH}	—	—	—	2, 3
Output clock to output valid	t_{GCLKNV}	0	6	ns	—

Table 47. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	7.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0.3	—	ns	2, 4

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Figure 35 provides the AC test load for PCI.

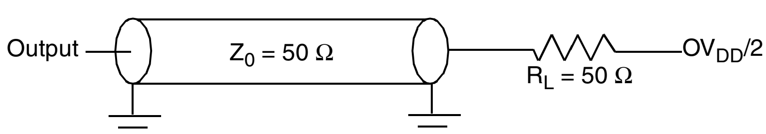


Figure 35. PCI AC Test Load

Figure 36 shows the PCI input AC timing conditions.

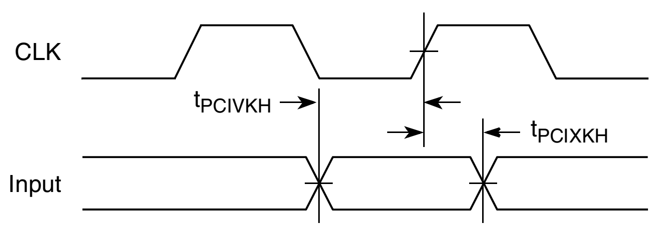


Figure 36. PCI Input AC Timing Measurement Conditions

Figure 39 provides the AC test load for the GPIO.

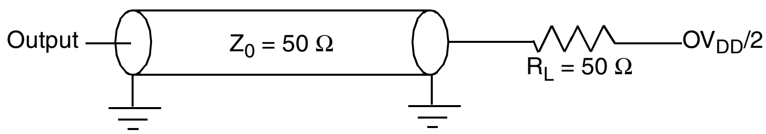


Figure 39. GPIO AC Test Load

15 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8358E.

15.1 IPIC DC Electrical Characteristics

Table 52 provides the DC electrical characteristics for the external interrupt pins of the IPIC.

Table 52. IPIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±10	μA
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:
1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ\_OUT}}$, $\overline{\text{MCP\_OUT}}$, and CE ports Interrupts.
2. $\overline{\text{IRQ\_OUT}}$ and $\overline{\text{MCP\_OUT}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

15.2 IPIC AC Timing Specifications

Table 53 provides the IPIC input and output AC timing specifications.

Table 53. IPIC Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

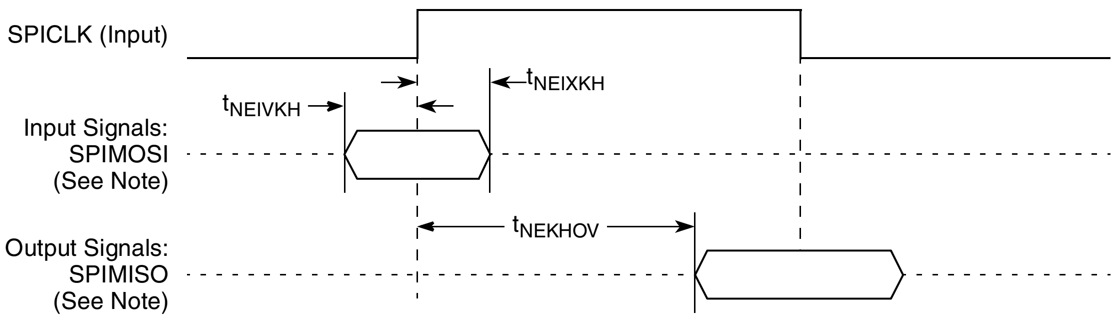
Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

16 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8358E.

Figure 41 and Figure 42 represent the AC timing from Table 55. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

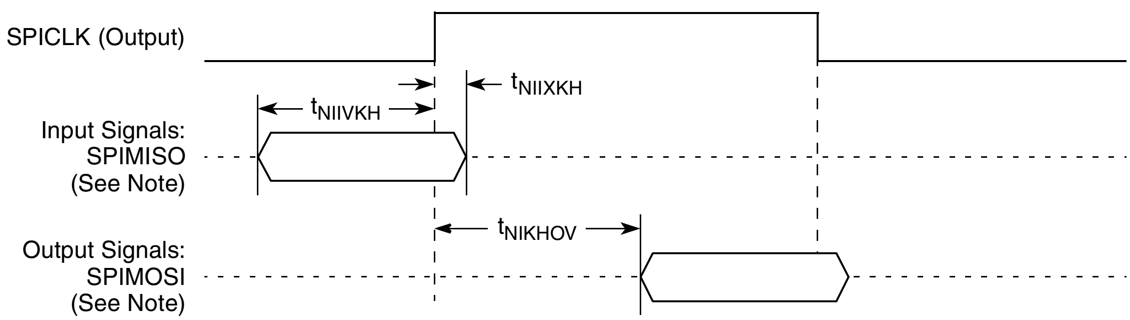
Figure 41 shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 41. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 42 shows the SPI timing in Master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 42. SPI AC Timing in Master Mode (Internal Clock) Diagram

17 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8358E.

17.1 TDM/SI DC Electrical Characteristics

Table 56 provides the DC electrical characteristics for the device TDM/SI.

Table 56. TDM/SI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V

21 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8358E is available in a plastic ball grid array (PBGA), see Section 21.1, “Package Parameters for the PBGA Package,” and Section 21.2, “Mechanical Dimensions of the PBGA Package,” for information on the package.

21.1 Package Parameters for the PBGA Package

The package parameters for rev 2.0 silicon are as provided in the following list. The package type is **29** mm x 29 mm, 668 plastic ball grid array (PBGA).

Package outline	**29 mm x 29 mm**
Interconnects	**668**
Pitch	**1.00 mm**
Module height (typical)	1.46 mm
Solder Balls	62 Sn/36 Pb/2 Ag *(*ZQ package)
	95.5 Sn/0.5 Cu/4Ag (VR package)
Ball diameter (typical)	0.64 mm

22 Clocking

Figure 53 shows the internal distribution of clocks within the MPC8358E.

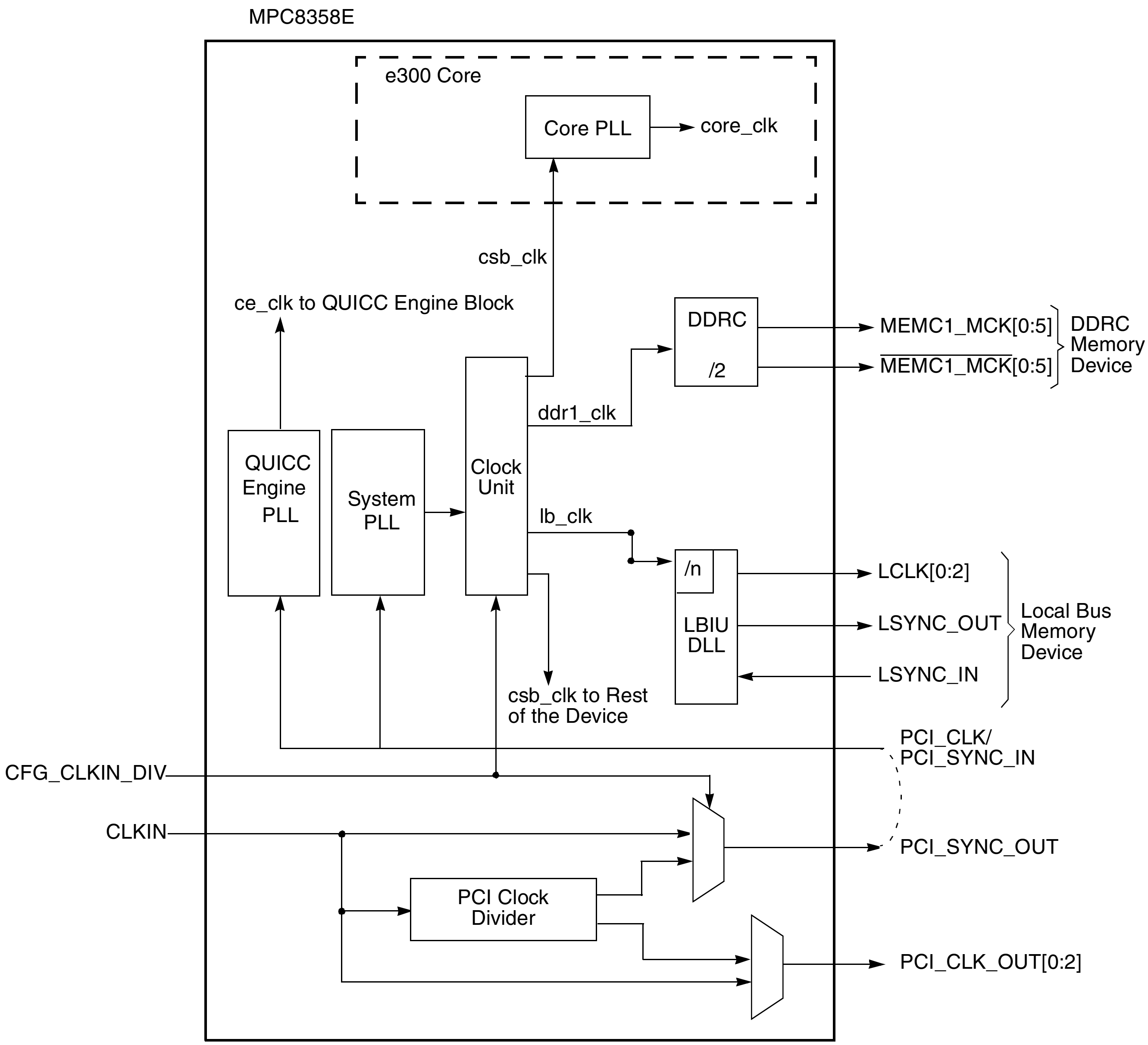


Figure 53. MPC8358E Clock Subsystem

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Note that in PCI host mode, the primary clock input also depends on whether PCI clock outputs are selected with RCWH[PCICKDRV]. When the device is configured as a PCI host device (RCWH[PCIHOST] = 1) and PCI clock output is selected (RCWH[PCICKDRV] = 1), CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration

Table 70. CSB Frequency Options (continued)

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk*: Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
High	0110	6:1			200	
High	0111	7:1			233	
High	1000	8:1				
High	1001	9:1				
High	1010	10:1				
High	1011	11:1				
High	1100	12:1				
High	1101	13:1				
High	1110	14:1				
High	1111	15:1				
High	0000	16:1				

1 CFG_CLKIN_DIV is only used for host mode; CLKIN must be tied low and CFG_CLKIN_DIV must be pulled down (low) in agent mode.
2 CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

22.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 71 shows the encodings for RCWL[COREPLL]. COREPLL values not listed in Table 71 should be considered reserved.

Table 71. e300 Core PLL Configuration

RCWL[COREPLL]			*core_clk*:*csb_clk* Ratio	VCO divider
0–1	2–5	6		
nn	**0000**	n	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
00	**0001**	0	1:1	÷2
01	**0001**	0	1:1	÷4
10	**0001**	0	1:1	÷8
11	**0001**	0	1:1	÷8
00	**0001**	1	1.5:1	÷2
01	**0001**	1	1.5:1	÷4
10	**0001**	1	1.5:1	÷8

Table 76 shows heat sinks and junction-to-ambient thermal resistance for PBGA package.

Table 76. Heat Sinks and Junction-to-Ambient Thermal Resistance of PBGA Package

Heat Sink Assuming Thermal Grease	Air Flow	29 × 29 mm PBGA
		Thermal Resistance
AAVID 30 × 30 × 9.4 mm Pin Fin	Natural Convection	12.6
AAVID 30 × 30 × 9.4 mm Pin Fin	1 m/s	8.2
AAVID 30 × 30 × 9.4 mm Pin Fin	2 m/s	7.0
AAVID 31 × 35 × 23 mm Pin Fin	Natural Convection	10.5
AAVID 31 × 35 × 23 mm Pin Fin	1 m/s	6.6
AAVID 31 × 35 × 23 mm Pin Fin	2 m/s	6.1
Wakefield, 53 × 53 × 25 mm Pin Fin	Natural Convection	9.0
Wakefield, 53 × 53 × 25 mm Pin Fin	1 m/s	5.6
Wakefield, 53 × 53 × 25 mm Pin Fin	2 m/s	5.1
MEI, 75 × 85 × 12 no adjacent board, extrusion	Natural Convection	9.0
MEI, 75 × 85 × 12 no adjacent board, extrusion	1 m/s	5.7
MEI, 75 × 85 × 12 no adjacent board, extrusion	2 m/s	5.1

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
473 Sapena Ct. #15
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

includes an application modifier, which may specify special application conditions. Each part number also contains a revision code that refers to the die mask revision number.

Table 78. Part Numbering Nomenclature[1]

MPC	*nnnn*	*e*	*t*	*pp*	*aa*	*a*	*a*	*A*
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature Range**	**Package[2]**	**Processor Frequency[3]**	**Platform Frequency**	**QUICC Engine Frequency**	**Die Revision**
MPC	8358	Blank = Not included E = included	Blank = 0 °C T_A to 105 °C T_J C= –40°C T_A to 105°C T_J	ZQ = PBGA VR = PBGA (no lead)	e300 core speed AD = 266 MHz AG = 400 MHz	D = 266 MHz	D = 266 MHz G = 400 MHz	A = revision 2.1 silicon

1 Not all processor, platform, and QUICC Engine block frequency combinations are supported. For available frequency combinations, contact your local Freescale sales office or authorized distributor.
2 See Section 21, "Package and Pin Listings," for more information on available package types.
3 Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

Table 79 shows the SVR settings by device and package type.

Table 79. SVR Settings

Device	Package	SVR (Rev. 2.1)
MPC8358E	PBGA	0x804E_0021
MPC8358	PBGA	0x804F_0021

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