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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	-
Number of Cores/Bus Width	-
Speed	-
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-
Security Features	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8358cvragdda

- Multiple master support
- Master or slave I²C mode support
- On-chip digital filtering rejects spikes on the bus
- System initialization data is optionally loaded from I²C-1 EPROM by boot sequencer embedded hardware
- DMA controller
 - Four independent virtual channels
 - Concurrent execution across multiple channels with programmable bandwidth control
 - All channels accessible by local core and remote PCI masters
 - Misaligned transfer capability
 - Data chaining and direct mode
 - Interrupt on completed segment and chain
 - DMA external handshake signals: $\overline{\text{DMA_DREQ}}[0:3]/\overline{\text{DMA_DACK}}[0:3]/\overline{\text{DMA_DONE}}[0:3]$. There is one set for each DMA channel. The pins are multiplexed to the parallel IO pins with other QE functions.
- DUART
 - Two 4-wire interfaces (RxD, TxD, RTS, CTS)
 - Programming model compatible with the original 16450 UART and the PC16550D
- System timers
 - Periodic interrupt timer
 - Real-time clock
 - Software watchdog timer
 - Eight general-purpose timers
- IEEE Std. 1149.1TM-compliant, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8358E. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the device. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	$1.2\text{ V} \pm 60\text{ mV}$	V	1
PLL supply voltage	AV_{DD}	$1.2\text{ V} \pm 60\text{ mV}$	V	1
DDR and DDR2 DRAM I/O supply voltage	GV_{DD}	$2.5\text{ V} \pm 125\text{ mV}$ $1.8\text{ V} \pm 90\text{ mV}$	V	—
Three-speed Ethernet I/O supply voltage	LV_{DD0}	$3.3\text{ V} \pm 330\text{ mV}$ $2.5\text{ V} \pm 125\text{ mV}$	V	—
Three-speed Ethernet I/O supply voltage	LV_{DD1}	$3.3\text{ V} \pm 330\text{ mV}$ $2.5\text{ V} \pm 125\text{ mV}$	V	—
Three-speed Ethernet I/O supply voltage	LV_{DD2}	$3.3\text{ V} \pm 330\text{ mV}$ $2.5\text{ V} \pm 125\text{ mV}$	V	—
PCI, local bus, DUART, system control and power management, I ² C, SPI, and JTAG I/O voltage	OV_{DD}	$3.3\text{ V} \pm 330\text{ mV}$	V	—
Junction temperature	T_J	0 to 105 –40 to 105	°C	—

Notes:

1. GV_{DD} , LV_{DD} , OV_{DD} , AV_{DD} , and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	$OV_{DD} = 3.3\text{ V}$
PCI signals	25	
PCI output clocks (including PCI_SYNC_OUT)	42	
DDR signal	20 36 (half-strength mode) ¹	$GV_{DD} = 2.5\text{ V}$
DDR2 signal	18 36 (half-strength mode) ¹	$GV_{DD} = 1.8\text{ V}$
10/100/1000 Ethernet signals	42	$LV_{DD} = 2.5/3.3\text{ V}$
DUART, system control, I ² C, SPI, JTAG	42	$OV_{DD} = 3.3\text{ V}$
GPIO signals	42	$OV_{DD} = 3.3\text{ V}$ $LV_{DD} = 2.5/3.3\text{ V}$

¹ DDR output impedance values for half strength mode are verified by design and not tested.

2.2 Power Sequencing

This section details the power sequencing considerations for the MPC8358E.

2.2.1 Power-Up Sequencing

MPC8358E does not require the core supply voltage (V_{DD} and AV_{DD}) and I/O supply voltages (GV_{DD} , LV_{DD} , and OV_{DD}) to be applied in any particular order. During the power ramp up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there may be a period of time that all input and output pins will actively be driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD} , LV_{DD} , and OV_{DD}) and assert $\overline{PORESET}$ before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V, see Figure 4.

Table 12. QUICC Engine Block Operating Frequency Limitations (continued)

Interface	Interface Operating Frequency (MHz)	Max Interface Bit Rate (Mbps)	Min QUICC Engine Operating Frequency ¹ (MHz)	Notes
UART/async HDLC	3.68 (max internal ref clock)	115 (Kbps)	20	—
BISYNC	2 (max)	2	20	—
USB	48 (ref clock)	12	96	—

Notes:

1. The QUICC Engine module needs to run at a frequency higher than or equal to what is listed in this table.
2. 'F' is the actual interface operating frequency.
3. The bit rate limit is independent of the data bus width (that is, the same for serial, nibble, or octal interfaces).
4. TDM in high-speed mode for serial data interface.

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR and DDR2 SDRAM interface of the MPC8358E.

6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

Table 13 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the device when $GV_{DD}(\text{typ}) = 1.8 \text{ V}$.

Table 13. DDR2 SDRAM DC Electrical Characteristics for $GV_{DD}(\text{typ}) = 1.8 \text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	$MV_{REF} - 0.125$	V	—
Output leakage current	I_{OZ}	—	± 10	μA	4
Output high current ($V_{OUT} = 1.420 \text{ V}$)	I_{OH}	-13.4	—	mA	—
Output low current ($V_{OUT} = 0.280 \text{ V}$)	I_{OL}	13.4	—	mA	—
MV_{REF} input leakage current	I_{VREF}	—	± 10	μA	—

Table 16 provides the DDR capacitance when $GV_{DD}(typ) = 2.5\text{ V}$.

Table 16. DDR SDRAM Capacitance for $GV_{DD}(typ) = 2.5\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 2.5\text{ V} \pm 0.125\text{ V}$, $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR2 SDRAM interface when $GV_{DD}(typ) = 1.8\text{ V}$.

Table 17. DDR2 SDRAM Input AC Timing Specifications for $GV_{DD}(typ) = 1.8\text{ V}$

At recommended operating conditions with GV_{DD} of $1.8\text{ V} \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.25$	V	—
AC input high voltage	V_{IH}	$MV_{REF} + 0.25$	—	V	—

Table 18 provides the input AC timing specifications for the DDR SDRAM interface when $GV_{DD}(typ) = 2.5\text{ V}$.

Table 18. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of $2.5\text{ V} \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.31$	V	—
AC input high voltage	V_{IH}	$MV_{REF} + 0.31$	—	V	—

Note:

1. Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if $0 \leq n \leq 7$ or ECC (MECC[{0...7}] if $n = 8$).

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) $\pm 5\%$.

Parameter ⁸	Symbol ¹	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDKHME}	-0.6	0.9	ns	7

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All $MCK/\overline{MCK}$ referenced measurements are made from the crossing of the two signals ± 0.1 V.
3. In the source synchronous mode, $MCK/\overline{MCK}$ can be shifted in $\frac{1}{4}$ applied cycle increments through the clock control register. For the skew measurements referenced for t_{AOSKEW} it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.
4. ADDR/CMD includes all DDR SDRAM output signals except $MCK/\overline{MCK}$, $\overline{MCS}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by $\frac{1}{2}$ applied cycle.
5. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. In source synchronous mode, this will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *MPC8360E PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
6. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the device.
7. All outputs are referenced to the rising edge of MCK(n) at the pins of the device. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
8. AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.

Figure 6 shows the DDR SDRAM output timing for address skew with respect to any MCK.

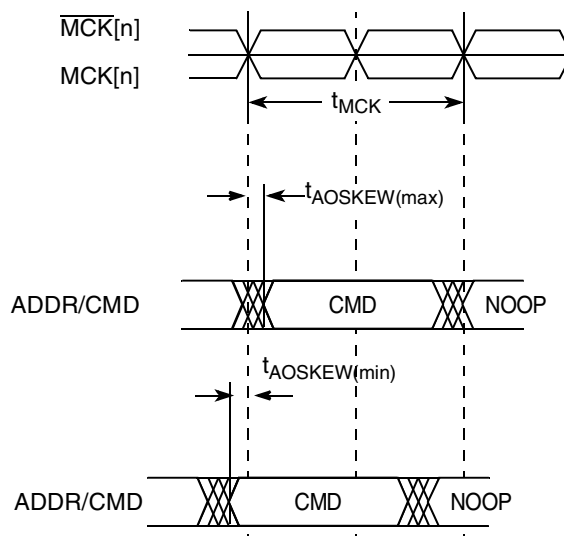


Figure 6. Timing Diagram for t_{AOSKEW} Measurement

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8358E.

7.1 DUART DC Electrical Characteristics

Table 22 provides the DC electrical characteristics for the DUART interface of the device.

Table 22. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V	—
Low-level input voltage OV_{DD}	V_{IL}	-0.3	0.8	V	—
High-level output voltage, $I_{OH} = -100 \mu A$	V_{OH}	$OV_{DD} - 0.4$	—	V	—
Low-level output voltage, $I_{OL} = 100 \mu A$	V_{OL}	—	0.2	V	—
Input current ($0 V \leq V_{IN} \leq OV_{DD}$)	I_{IN}	—	± 10	μA	1

Note:

- Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

Table 23 provides the AC timing parameters for the DUART interface of the device.

Table 23. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	—
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16	—	2

Notes:

- Actual attainable baud rate will be limited by the latency of interrupt processing.
- The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each sixteenth sample.

8 UCC Ethernet Controller: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

Table 25. RGMII/RTBI DC Electrical Characteristics (when operating at 2.5 V)

Parameters	Symbol	Conditions	Min	Max	Unit
Supply voltage 2.5 V	V_{DD}	—	2.37	2.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0 \text{ mA}$ $V_{DD} = \text{Min}$	2.00	$V_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0 \text{ mA}$ $V_{DD} = \text{Min}$	$\text{GND} - 0.3$	0.40	V
Input high voltage	V_{IH}	— $V_{DD} = \text{Min}$	1.7	$V_{DD} + 0.3$	V
Input low voltage	V_{IL}	— $V_{DD} = \text{Min}$	-0.3	0.70	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq V_{DD}$	—	± 10	μA

8.2 GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1 GMII Timing Specifications

This sections describe the GMII transmit and receive AC timing specifications.

8.2.1.1 GMII Transmit AC Timing Specifications

Table 26 provides the GMII transmit AC timing specifications.

Table 26. GMII Transmit AC Timing Specifications

At recommended operating conditions with V_{DD}/OV_{DD} of $3.3 \text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns	—
GTX_CLK duty cycle	t_{GTXH}/t_{GTX}	40	—	60	%	—
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX} t_{GTKHDV}	0.5 —	—	— 5.0	ns	—
GTX_CLK clock rise time, (20% to 80%)	t_{GTXR}	—	—	1.0	ns	—
GTX_CLK clock fall time, (80% to 20%)	t_{GTXF}	—	—	1.0	ns	—
GTX_CLK125 clock period	t_{G125}	—	8.0	—	ns	2
GTX_CLK125 reference clock duty cycle measured at $V_{DD}/2$	t_{G125H}/t_{G125}	45	—	55	%	2

Notes:

- The symbols used for timing specifications follow the pattern $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- This symbol is used to represent the external GTX_CLK125 signal and does not follow the original symbol naming convention.

Table 37. IEEE 1588 Timer AC Specifications (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Timer alarm to output valid	t_{TMRAL}	—	—	—	2

Notes:

1. The timer can operate on rtc_clock or tmr_clock. These clocks get muxed and any one of them can be selected. The minimum and maximum requirement for both rtc_clock and tmr_clock are the same.
2. These are asynchronous signals.
3. Inputs need to be stable at least one TMR clock.

9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8358E.

9.1 Local Bus DC Electrical Characteristics

Table 38 provides the DC electrical characteristics for the local bus interface.

Table 38. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	−0.3	0.8	V
High-level output voltage, $I_{OH} = -100 \mu A$	V_{OH}	$OV_{DD} - 0.4$	—	V
Low-level output voltage, $I_{OL} = 100 \mu A$	V_{OL}	—	0.2	V
Input current	I_{IN}	—	± 10	μA

9.2 Local Bus AC Electrical Specifications

Table 39 describes the general timing parameters of the local bus interface of the device.

Table 39. Local Bus General Timing Parameters—DLL Enabled

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	—	ns	2
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	1.7	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.9	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3.0	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7

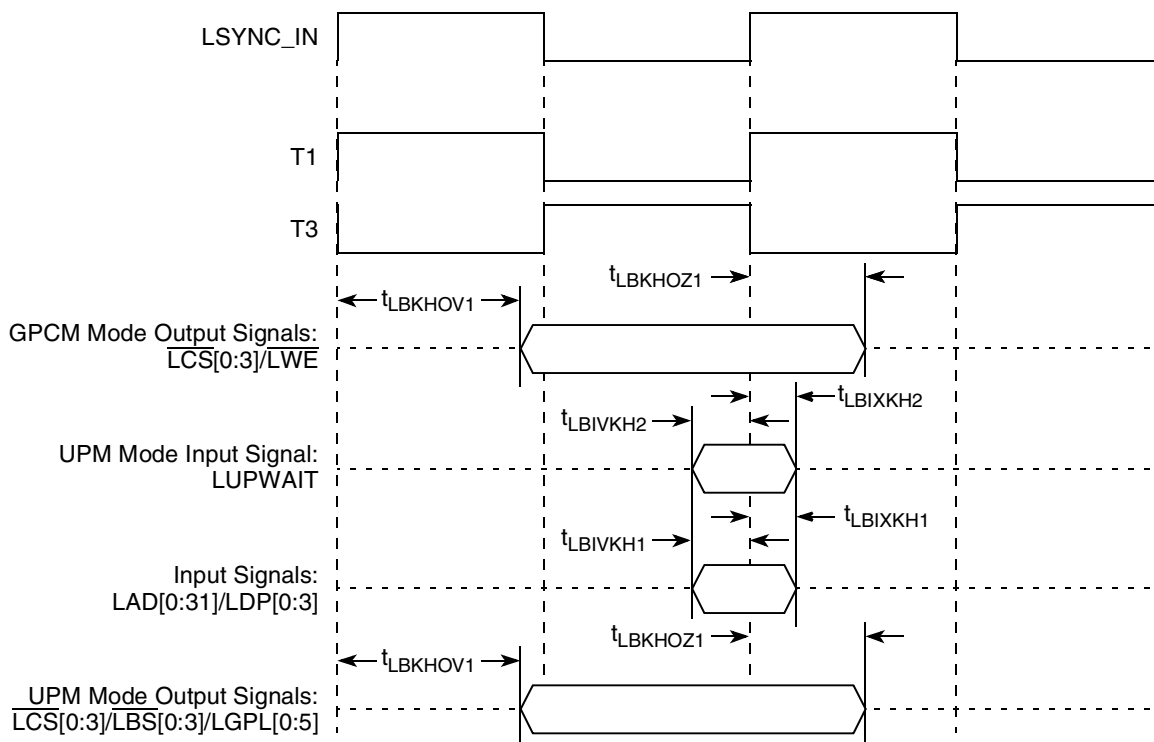


Figure 24. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (DLL Enabled)

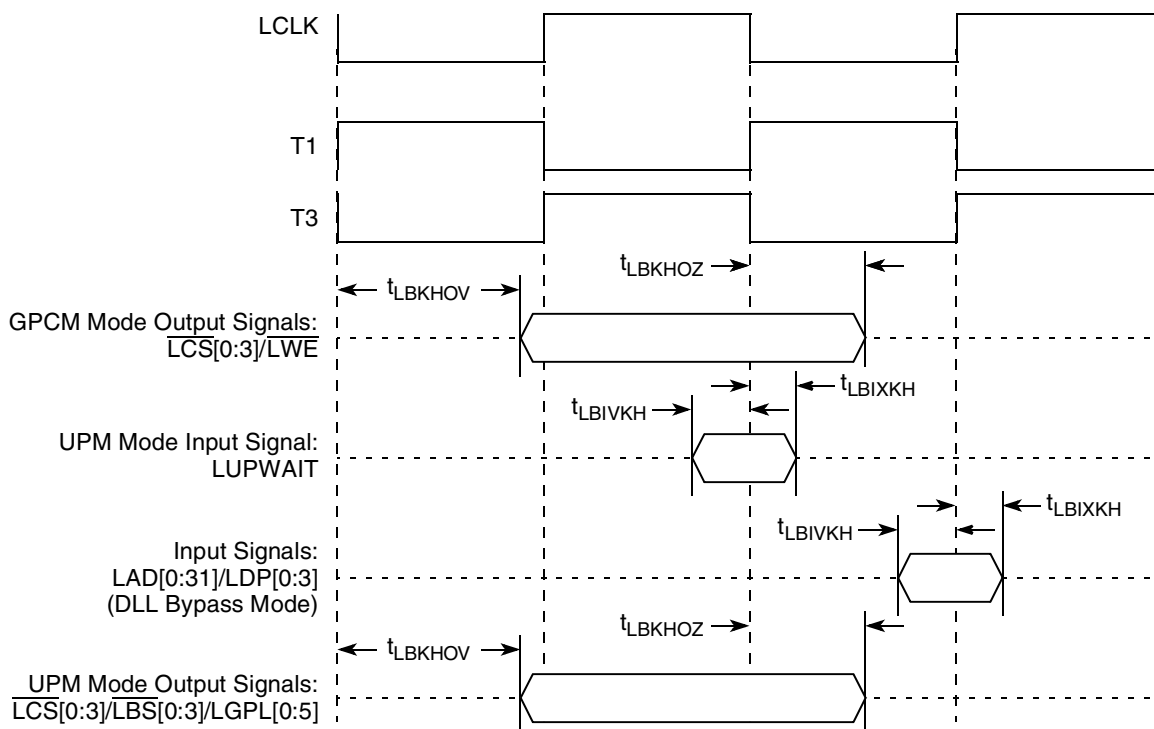


Figure 25. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (DLL Bypass Mode)

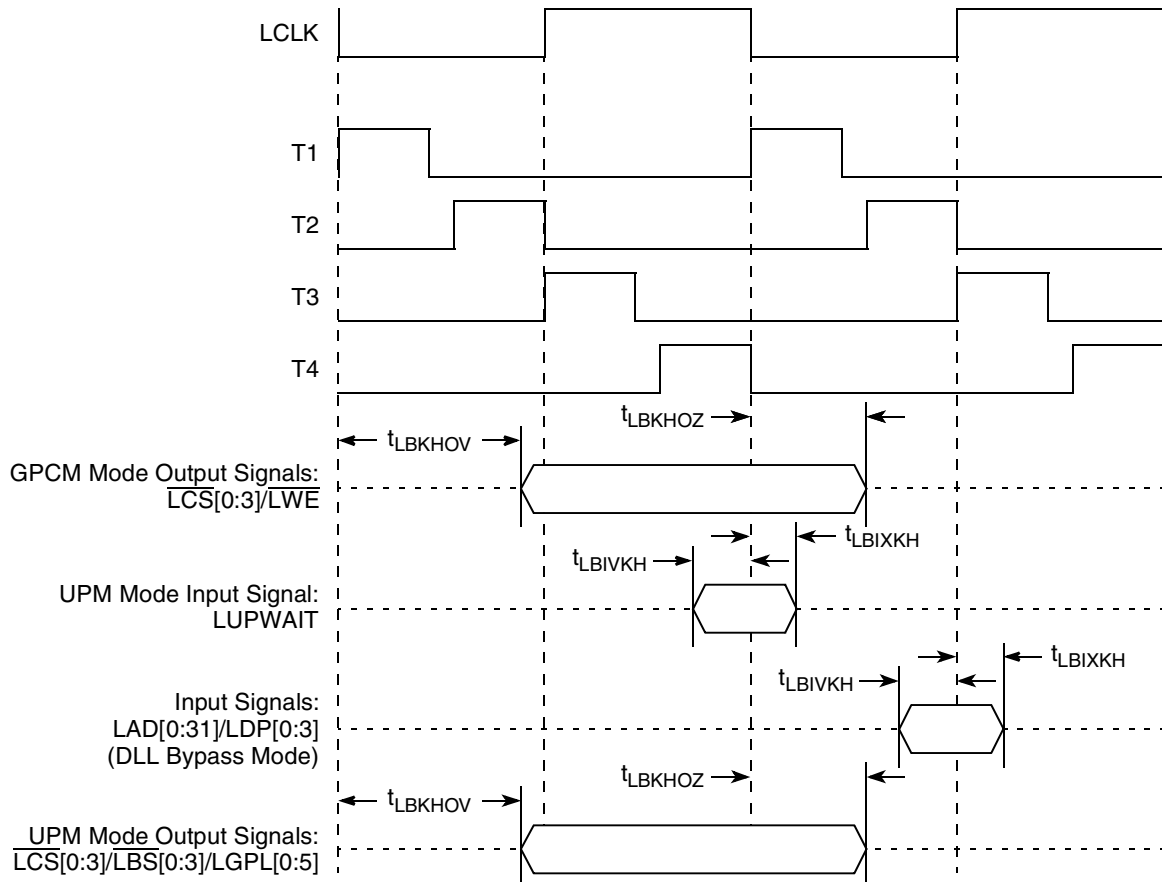


Figure 26. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (DLL Bypass Mode)

12 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8358E.

12.1 PCI DC Electrical Characteristics

Table 45 provides the DC electrical characteristics for the PCI interface of the device.

Table 45. PCI DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH} \text{ (min) or } V_{OUT} \leq V_{OL} \text{ (max)}$	$0.5 \times OV_{DD}$	$OV_{DD} + 0.5$	V
Low-level input voltage	V_{IL}		-0.5	$0.3 \times OV_{DD}$	V
High-level output voltage	V_{OH}	$I_{OH} = -500 \mu A$	$0.9 \times OV_{DD}$	—	V
Low-level output voltage	V_{OL}	$I_{OL} = 1500 \mu A$	—	$0.1 \times OV_{DD}$	V
Input current	I_{IN}	$0 V \leq V_{IN}^1 \leq OV_{DD}$	—	± 10	μA

Note:

- Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

12.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the device. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. Table 46 provides the PCI AC timing specifications at 66 MHz.

Table 46. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from clock	t_{PCKHOX}	1	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0.3	—	ns	2, 4

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS} , reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
- See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
- For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- Input timings are measured at the pin.

19.2 HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

Table 61 and Table 62 provide the input and output AC timing specifications for HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 61. HDLC, BISYNC, and Transparent AC Timing Specifications¹

Characteristic	Symbol ²	Min	Max	Unit
Outputs—Internal clock delay	t_{HIKHOV}	0	11.2	ns
Outputs—External clock delay	t_{HEKHOV}	1	10.8	ns
Outputs—Internal clock high impedance	t_{HIKHOX}	-0.5	5.5	ns
Outputs—External clock high impedance	t_{HEKHOX}	1	8	ns
Inputs—Internal clock input setup time	t_{HIIVKH}	8.5	—	ns
Inputs—External clock input setup time	t_{HEIVKH}	4	—	ns
Inputs—Internal clock input hold time	t_{HIIXKH}	1.4	—	ns
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:

- Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Table 62. Synchronous UART AC Timing Specifications¹

Characteristic	Symbol ²	Min	Max	Unit
Outputs—Internal clock delay	$t_{UAIKHOV}$	0	11.3	ns
Outputs—External clock delay	$t_{UAEKHOV}$	1	14	ns
Outputs—Internal clock high impedance	$t_{UAIKHOX}$	0	11	ns
Outputs—External clock high impedance	$t_{UAEKHOX}$	1	14	ns
Inputs—Internal clock input setup time	$t_{UAIIVKH}$	6	—	ns
Inputs—External clock input setup time	$t_{UAEIVKH}$	8	—	ns
Inputs—Internal clock input hold time	$t_{UAIIXKH}$	1	—	ns
Inputs—External clock input hold time	$t_{UAEIXKH}$	1	—	ns

Notes:

- Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Table 65. MPC8358E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_PAR/ PF[11]	AA4	I/O	OV _{DD}	—
PCI_FRAME/ PF[12]	W4	I/O	OV _{DD}	5
PCI_TRDY/ PF[13]	W5	I/O	OV _{DD}	5
PCI_IRDY/ PF[14]	AB3	I/O	OV _{DD}	5
PCI_STOP/ PF[15]	AB1	I/O	OV _{DD}	5
PCI_DEVSEL/ PF[16]	AA2	I/O	OV _{DD}	5
PCI_IDSEL/ PF[17]	U6	I/O	OV _{DD}	—
PCI_SERR/ PF[18]	AC1	I/O	OV _{DD}	5
PCI_PERR/ PF[19]	W6	I/O	OV _{DD}	5
PCI_REQ[0:2]/ PF[20:22]	R2, T4, U1	I/O	LV _{DD2}	—
PCI_GNT[0:2]/ PF[23:25]	T3, R5, T1	I/O	LV _{DD2}	—
PCI_MODE	AE5	I	OV _{DD}	—
M66EN/ CE_PF[4]	AH3	I/O	OV _{DD}	—
Local Bus Controller Interface				
LAD[0:31]	AC11, AE10, AD10, AD11, AE11, AG11, AH11, AH12, AG12, AF12, AD12, AE12, AC12, AH13, AG13, AF13, AE13, AH14, AD13, AG14, AF14, AH15, AE14, AG15, AC13, AD14, AC14, AH16, AC15, AG16, AE15, AF16	I/O	OV _{DD}	—
LDP[0:3]	AD15, AG17, AC16, AF17	I/O	OV _{DD}	—
LA[27:31]	AH17, AD16, AH18, AG18, AE17	O	OV _{DD}	—
LCS[0:5]	AD18, AH20, AG20, AE19, AC18, AH21	O	OV _{DD}	—
LWE[0:3]	AG21, AH22, AC20, AD19	O	OV _{DD}	—
LBCTL	AF18	O	OV _{DD}	—
LALE	AF10	O	OV _{DD}	—
LGPL0/ LSDA10/ cfg_reset_source0	AC17	I/O	OV _{DD}	—
LGPL1/ LSDWE/ cfg_reset_source1	AD17	I/O	OV _{DD}	—

Table 65. MPC8358E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LGPL2/ LSDRAS/ LOE	AH19	O	OV _{DD}	—
LGPL3/ LSDCAS/ cfg_reset_source2	AE18	I/O	OV _{DD}	—
LGPL4/ LGTA/ LUPWAIT/ LPBSE	AG19	I/O	OV _{DD}	—
LGPL5/ cfg_clkin_div	AF19	I/O	OV _{DD}	—
LCKE	AD8	O	OV _{DD}	—
LCLK[0]	AC9	O	OV _{DD}	—
LCLK[1]/ LCS[6]	AG6	O	OV _{DD}	—
LCLK[2]/ LCS[7]	AE7	O	OV _{DD}	—
LSYNC_OUT	AG4	O	OV _{DD}	—
LSYNC_IN	AC8	I	OV _{DD}	—
Programmable Interrupt Controller				
MCP_OUT	AG3	O	OV _{DD}	2
IRQ0/ MCP_IN	AH4	I	OV _{DD}	—
IRQ[1:2]	AG5, AH5	I/O	OV _{DD}	—
IRQ[3]/ CORE_SRESET	AD7	I/O	OV _{DD}	—
IRQ[4:5]	AC7, AD6	I/O	OV _{DD}	—
IRQ[6:7]	AC6, AC10	I/O	OV _{DD}	—
DUART				
UART1_SOUT	AE3	O	OV _{DD}	—
UART1_SIN	AE4	I/O	OV _{DD}	—
UART1_CTS	AG2	I/O	OV _{DD}	—
UART1_RTS	AA6	O	OV _{DD}	—
I²C Interface				
IIC1_SDA	AB6	I/O	OV _{DD}	2
IIC1_SCL	AD5	I/O	OV _{DD}	2
IIC2_SDA	AF3	I/O	OV _{DD}	2
IIC2_SCL	AH2	I/O	OV _{DD}	2
QUICC Engine				
CE_PA[0]	F6	I/O	LV _{DD0}	—

input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCIOEN n] parameters enable the PCI_CLK_OUT n , respectively.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock. When the device is configured as a PCI agent device the CLKIN and the CFG_CLKIN_DIV signals should be tied to GND.

When the device is configured as a PCI host device (RCWH[PCIHOST] = 1) and PCI clock output is disabled (RCWH[PCICKDRV] = 0), clock distribution and balancing done externally on the board. Therefore, PCI_SYNC_IN is the primary input clock.

As shown in [Figure 53](#), the primary clock input (frequency) is multiplied by the QUICC Engine block phase-locked loop (PLL), the system PLL, and the clock unit to create the QUICC Engine clock (*ce_clk*), the coherent system bus clock (*csb_clk*), the internal DDRC1 controller clock (*ddr1_clk*), and the internal clock for the local bus interface unit and DDR2 memory controller (*lb_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb_clk = \{PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)\} \times SPMF$$

In PCI host mode, $PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)$ is the CLKIN frequency; in PCI agent mode, CFG_CLKIN_DIV must be pulled down (low), so $PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)$ is the PCI_CLK frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, “Reset, Clocking, and Initialization,” in the *MPC8360E PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for more information on the clock subsystem.

The *ce_clk* frequency is determined by the QUICC Engine PLL multiplication factor (RCWL[CEPMF]) and the QUICC Engine PLL division factor (RCWL[CEPDF]) according to the following equation:

$$ce_clk = (\text{primary clock input} \times CEPMF) \div (1 + CEPDF)$$

The internal *ddr1_clk* frequency is determined by the following equation:

$$ddr1_clk = csb_clk \times (1 + RCWL[DDR1CM])$$

Note that the *lb_clk* clock frequency (for DDRC2) is determined by RCWL[LBCM]. The *internal ddr1_clk* frequency is not the external memory bus frequency; *ddr1_clk* passes through the DDRC1 clock divider ($\div 2$) to create the differential DDRC1 memory bus clock outputs (MEMC1_MCK and MEMC1_MCK). However, the data rate is the same frequency as *ddr1_clk*.

The internal *lb_clk* frequency is determined by the following equation:

$$lb_clk = csb_clk \times (1 + RCWL[LBCM])$$

Note that *lb_clk* is not the external local bus or DDRC2 frequency; *lb_clk* passes through the a LB clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK[0:2]). The LB clock divider ratio is controlled by LCRR[CLKDIV].

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 66 specifies which units have a configurable clock frequency.

Table 66. Configurable Clock Units

Unit	Default Frequency	Options
Security core	<i>csb_clk</i> /3	Off, <i>csb_clk</i> ¹ , <i>csb_clk</i> /2, <i>csb_clk</i> /3
PCI and DMA complex	<i>csb_clk</i>	Off, <i>csb_clk</i>

¹ With limitation, only for slow *csb_clk* rates, up to 166 MHz.

Table 67 provides the operating frequencies for the PBGA package under recommended operating conditions (see Table 2). All frequency combinations shown in the table below may not be available. Maximum operating frequencies depend on the part ordered, see Section 25.1, “Part Numbers Fully Addressed by this Document,” for part ordering details and contact your Freescale sales representative or authorized distributor for more information.

Table 67. Operating Frequencies for the PBGA Package

Characteristic ¹	400 MHz	Unit
e300 core frequency (<i>core_clk</i>)	266–400	MHz
Coherent system bus frequency (<i>csb_clk</i>)	133–266	MHz
QUICC Engine frequency (<i>ce_clk</i>)	266–400	MHz
DDR and DDR2 memory bus frequency (MCLK) ²	100–133	MHz
Local bus frequency (LCLK _n) ³	16.67–133	MHz
PCI input frequency (CLKIN or PCI_CLK)	25–66.67	MHz
Security core maximum internal operating frequency	133	MHz

¹ The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.

² The DDR data rate is 2x the DDR memory bus frequency.

³ The local bus frequency is 1/2, 1/4, or 1/8 of the *lb_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBCM]).

The system VCO frequency is derived from the following equations:

- $csb_clk = \{PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)\} \times SPMF$
- System VCO Frequency = $csb_clk \times$ VCO divider (if both RCWL[DDRCM] and RCWL[LBCM] are cleared)
OR
- System VCO frequency = $2 \times csb_clk \times$ VCO divider (if either RCWL[DDRCM] or RCWL[LBCM] are set).

As described in [Section 22, “Clocking,”](#) the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). [Table 70](#) shows the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

Table 70. CSB Frequency Options

CFG_CLKIN_DIV at Reset ¹	SPMF	csb_clk: Input Clock Ratio ²	Input Clock Frequency (MHz) ²			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2:1				133
Low	0011	3:1				200
Low	0100	4:1				266
Low	0101	5:1				333
Low	0110	6:1	100	150	200	
Low	0111	7:1	116	175	233	
Low	1000	8:1	133	200	266	
Low	1001	9:1	150	225	300	
Low	1010	10:1	166	250	333	
Low	1011	11:1	183	275		
Low	1100	12:1	200	300		
Low	1101	13:1	216	325		
Low	1110	14:1	233			
Low	1111	15:1	250			
Low	0000	16:1	266			
High	0010	2:1				133
High	0011	3:1				200
High	0100	4:1				266
High	0101	5:1				333

Table 72. QUICC Engine Block PLL Multiplication Factors (continued)

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF])
01011	1	× 5.5
01101	1	× 6.5
01111	1	× 7.5
10001	1	× 8.5
10011	1	× 9.5
10101	1	× 10.5
10111	1	× 11.5
11001	1	× 12.5
11011	1	× 13.5
11101	1	× 14.5

Note:

1. Reserved modes are not listed.

The RCWL[CEVCOD] denotes the QUICC Engine Block PLL VCO internal frequency as shown in [Table 73](#).

Table 73. QUICC Engine Block PLL VCO Divider

RCWL[CEVCOD]	VCO Divider
00	4
01	8
10	2
11	Reserved

NOTE

The VCO divider (RCWL[CEVCOD]) must be set properly so that the QUICC Engine block VCO frequency is in the range of 600–1400 MHz. The QUICC Engine block frequency is not restricted by the CSB and core frequencies. The CSB, core, and QUICC Engine block frequencies should be selected according to the performance requirements.

The QUICC Engine block VCO frequency is derived from the following equations:

$$ce_clk = (\text{primary clock input} \times \text{CEPMF}) \div (1 + \text{CEPDF})$$

$$\text{QE VCO Frequency} = ce_clk \times \text{VCO divider} \times (1 + \text{CEPDF})$$

- To configure the device with CSB clock rate of 266 MHz, core rate of 400 MHz, and QUICC Engine clock rate 300 MHz while the input clock rate is 33 MHz. Conf No. 's10' and 'c1' are selected from [Table 74](#). SPMF is 1000, CORPLL is 0000011, CEPMF is 01001, and CEPDF is 0.

23 Thermal

This section describes the thermal specifications of the MPC8358E.

23.1 Thermal Characteristics

[Table 75](#) provides the package thermal characteristics for the 668 29 mm x 29 mm PBGA package.

Table 75. Package Thermal Characteristics for the PBGA Package

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection on single layer board (1s)	$R_{\theta JA}$	20	°C/W	1, 2
Junction-to-ambient Natural Convection on four layer board (2s2p)	$R_{\theta JA}$	14	°C/W	1, 2, 3
Junction-to-ambient (@ 1 m/s) on single layer board (1s)	$R_{\theta JMA}$	15	°C/W	1, 3
Junction-to-ambient (@ 1 m/s) on four layer board (2s2p)	$R_{\theta JMA}$	11	°C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	6	°C/W	4
Junction-to-case thermal	$R_{\theta JC}$	4	°C/W	5
Junction-to-Package Natural Convection on Top	Ψ_{JT}	4	°C/W	6

Notes

- Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- Per JEDEC JESD51-2 and JEDEC JESD51-9 with the single layer board horizontal.
- Per JEDEC JESD51-6 with the board horizontal. 1 m/sec is approximately equal to 200 linear feet per minute (LFM).
- Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

23.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers. See [Table 5](#) for typical power dissipations values.