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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	668-BBGA Exposed Pad
Supplier Device Package	668-PBGA-PGE (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8358ezqaddda

  - Multiple master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
  - System initialization data is optionally loaded from I^2C-1 EPROM by boot sequencer embedded hardware
- DMA controller
  - Four independent virtual channels
  - Concurrent execution across multiple channels with programmable bandwidth control
  - All channels accessible by local core and remote PCI masters
  - Misaligned transfer capability
  - Data chaining and direct mode
  - Interrupt on completed segment and chain
  - DMA external handshake signals: $\overline{\text{DMA\_DREQ}}$[0:3]/$\overline{\text{DMA\_DACK}}$[0:3]/$\overline{\text{DMA\_DONE}}$[0:3]. There is one set for each DMA channel. The pins are multiplexed to the parallel IO pins with other QE functions.
- DUART
  - Two 4-wire interfaces (RxD, TxD, RTS, CTS)
  - Programming model compatible with the original 16450 UART and the PC16550D
- System timers
  - Periodic interrupt timer
  - Real-time clock
  - Software watchdog timer
  - Eight general-purpose timers
- IEEE Std. 1149.1™-compliant, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8358E. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

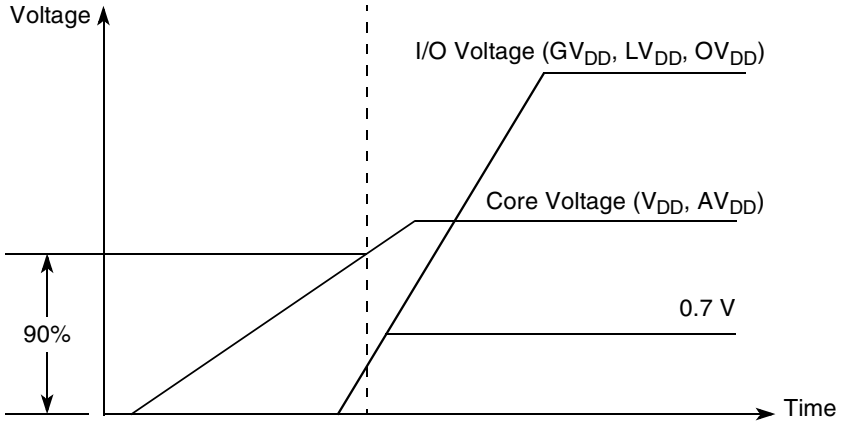


Figure 4. Power Sequencing Example

I/O voltage supplies (GV_{DD}, LV_{DD}, and OV_{DD}) do not have any ordering requirements with respect to one another.

2.2.2 Power-Down Sequencing

The MPC8358E does not require the core supply voltage and I/O supply voltages to be powered down in any particular order.

3 Power Characteristics

The estimated typical power dissipation values are shown in Table 4.

Table 4. MPC8358E PBGA Core Power Dissipation[1]

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
266	266	266	2.2	2.3	W	2, 3, 4
400	266	266	2.4	2.5	W	2, 3, 4
400	266	400	2.5	2.6	W	2, 3, 4

Notes:
1. The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see Table 5.
2. Typical power is based on a voltage of V_{DD} = 1.2 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.
3. Thermal solutions will likely need to design to a value higher than typical power on the end application, T_A target, and I/O power.
4. Maximum power is based on a voltage of V_{DD} = 1.2 V, WC process, a junction T_J = 105°C, and an artificial smoke test.

Table 12. QUICC Engine Block Operating Frequency Limitations (continued)

Interface	Interface Operating Frequency (MHz)	Max Interface Bit Rate (Mbps)	Min QUICC Engine Operating Frequency[1] (MHz)	Notes
UART/async HDLC	3.68 (max internal ref clock)	115 (Kbps)	20	—
BISYNC	2 (max)	2	20	—
USB	48 (ref clock)	12	96	—

Notes:
1. The QUICC Engine module needs to run at a frequency higher than or equal to what is listed in this table.
2. 'F' is the actual interface operating frequency.
3. The bit rate limit is independent of the data bus width (that is, the same for serial, nibble, or octal interfaces).
4. TDM in high-speed mode for serial data interface.

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR and DDR2 SDRAM interface of the MPC8358E.

6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

Table 13 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the device when GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.125$	V	—
Output leakage current	I_{OZ}	—	±10	µA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—
MV_{REF} input leakage current	I_{VREF}	—	±10	µA	—

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) ± 5%.

Parameter[8]	Symbol[1]	Min	Max	Unit	Notes
ADDR/CMD output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHAS}	 2.8 3.5	—	ns	4
ADDR/CMD output hold with respect to MCK 266 MHz—DDR1 266 MHz—DDR2 200 MHz	t_{DDKHAX}	 2.6 2.8 3.5	—	ns	4
$\overline{MCS}$(n) output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHCS}	 2.8 3.5	—	ns	4
$\overline{MCS}$(n) output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHCX}	 2.7 3.5	—	ns	4
MCK to MDQS	t_{DDKHMH}	–0.75	0.6	ns	5
MDQ/MECC/MDM output setup with respect to MDQS 266 MHz 200 MHz	t_{DDKHDS}, t_{DDKLDS}	 1.0 1.2	—	ns	6
MDQ/MECC/MDM output hold with respect to MDQS 266 MHz 200 MHz	t_{DDKHDX}, t_{DDKLDX}	 1.0 1.2	—	ns	6
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	7

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) ± 5%.

Parameter[8]	Symbol[1]	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDKHME}	–0.6	0.9	ns	7

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. In the source synchronous mode, MCK/$\overline{\text{MCK}}$ can be shifted in ¼ applied cycle increments through the clock control register. For the skew measurements referenced for t_{AOSKEW} it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.
4. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.
5. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. In source synchronous mode, this will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *MPC8360E PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
6. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the device.
7. All outputs are referenced to the rising edge of MCK(n) at the pins of the device. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
8. AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.

Figure 6 shows the DDR SDRAM output timing for address skew with respect to any MCK.

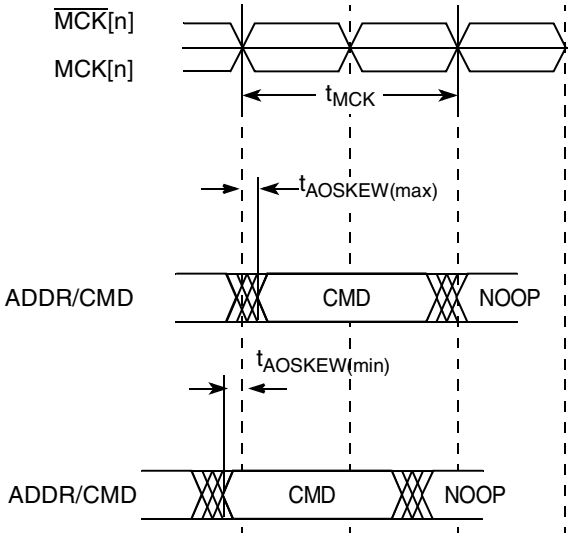


Figure 6. Timing Diagram for t_{AOSKEW} Measurement

Table 25. RGMII/RTBI DC Electrical Characteristics (when operating at 2.5 V)

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DD} = Min	2.00	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD} = Min	GND – 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DD} = Min	1.7	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	LV_{DD} = Min	–0.3	0.70	V
Input current	I_{IN}	$0 V \le V_{IN} \le LV_{DD}$		—	±10	μA

8.2 GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1 GMII Timing Specifications

This sections describe the GMII transmit and receive AC timing specifications.

8.2.1.1 GMII Transmit AC Timing Specifications

Table 26 provides the GMII transmit AC timing specifications.

Table 26. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns	—
GTX_CLK duty cycle	t_{GTXH}/t_{GTX}	40	—	60	%	—
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX} t_{GTKHDV}	0.5 —	—	— 5.0	ns	—
GTX_CLK clock rise time, (20% to 80%)	t_{GTXR}	—	—	1.0	ns	—
GTX_CLK clock fall time, (80% to 20%)	t_{GTXF}	—	—	1.0	ns	—
GTX_CLK125 clock period	t_{G125}	—	8.0	—	ns	2
GTX_CLK125 reference clock duty cycle measured at $LV_{DD/2}$	t_{G125H}/t_{G125}	45	—	55	%	2

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This symbol is used to represent the external GTX_CLK125 signal and does not follow the original symbol naming convention.

Table 34. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%	—

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (Rx) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Duty cycle reference is $LV_{DD}/2$.
6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
7. In rev. 2.1 silicon, due to errata, $t_{SKRGTKHDX}$ minimum is –0.65 ns for UCC2 option 1 and –0.9 for UCC2 option 2, and $t_{SKRGTKHDV}$ maximum is 0.75 ns for UCC1 and UCC2 option 1 and 0.85 for UCC2 option 2. UCC1 does meet $t_{SKRGTKHDX}$ minimum for rev. 2.1 silicon.

Figure 19 shows the RGMII and RTBI AC timing and multiplexing diagrams.

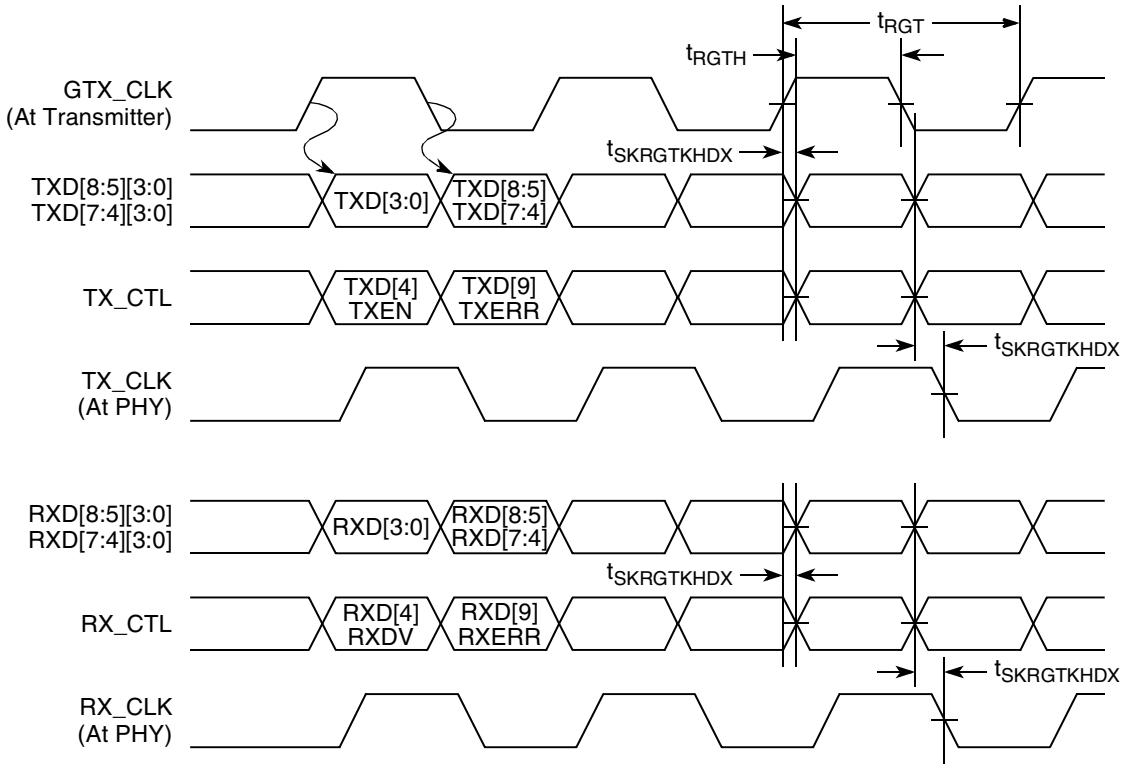


Figure 19. RGMII and RTBI AC Timing and Multiplexing Diagrams

Table 36. MII Management AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} is 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC fall time	t_{MDHF}	—	—	10	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, $t_{MDRDVKH}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
3. This parameter is dependent on the ce_clk speed (that is, for a ce_clk of 200 MHz, the delay is 90 ns and for a ce_clk of 300 MHz, the delay is 63 ns).

Figure 20 shows the MII management AC timing diagram.

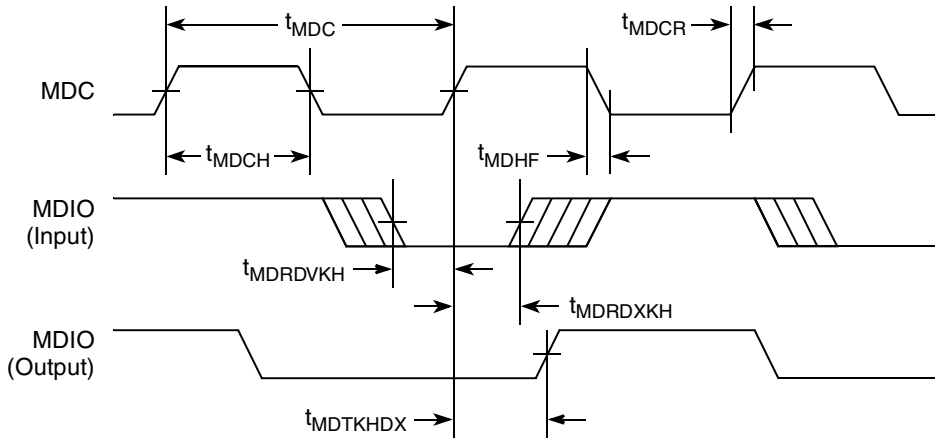


Figure 20. MII Management Interface Timing Diagram

8.3.3 IEEE 1588 Timer AC Specifications

Table 37 provides the IEEE 1588 timer AC specifications.

Table 37. IEEE 1588 Timer AC Specifications

Parameter	Symbol	Min	Max	Unit	Notes
Timer clock frequency	t_{TMRCK}	0	70	MHz	1
Input setup to timer clock	t_{TMRCKS}	—	—	—	2, 3
Input hold from timer clock	t_{TMRCKH}	—	—	—	2, 3
Output clock to output valid	t_{GCLKNV}	0	6	ns	—

Table 44. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 43).

Parameter	Symbol[1]	Min	Max	Unit
Data hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0[2]	 — 0.9[3]	µs
Rise time of both SDA and SCL signals	t_{I2CR}	20 + 0.1 C_b[4]	300	ns
Fall time of both SDA and SCL signals	t_{I2CF}	20 + 0.1 C_b[4]	300	ns
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The device provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.

Figure 33 provides the AC test load for the I²C.

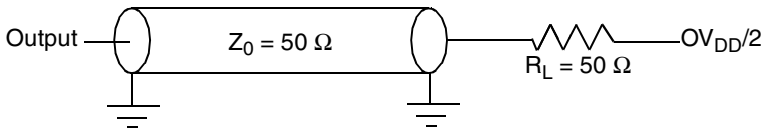


Figure 33. I²C AC Test Load

Figure 34 shows the AC timing diagram for the I²C bus.

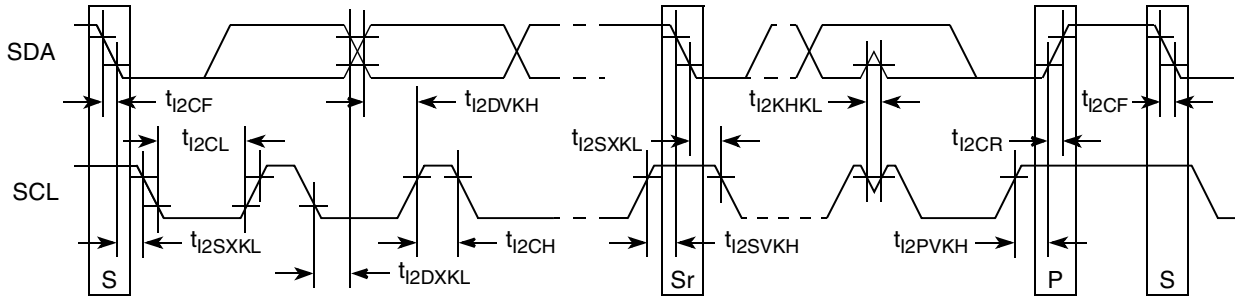


Figure 34. I²C Bus AC Timing Diagram

16.1 SPI DC Electrical Characteristics

Table 54 provides the DC electrical characteristics for the device SPI.

Table 54. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±10	μA

16.2 SPI AC Timing Specifications

Table 55 and provide the SPI input and output AC timing specifications.

Table 55. SPI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	t_{NIKHOX} t_{NIKHOV}	0.4 —	— 8	ns
SPI outputs—Slave mode (external clock) delay	t_{NEKHOX} t_{NEKHOV}	2 —	— 8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	8	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

Figure 40 provides the AC test load for the SPI.

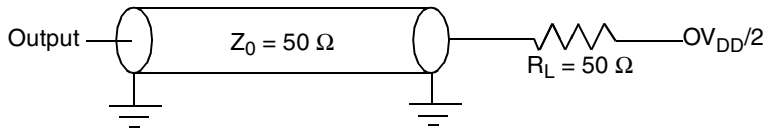
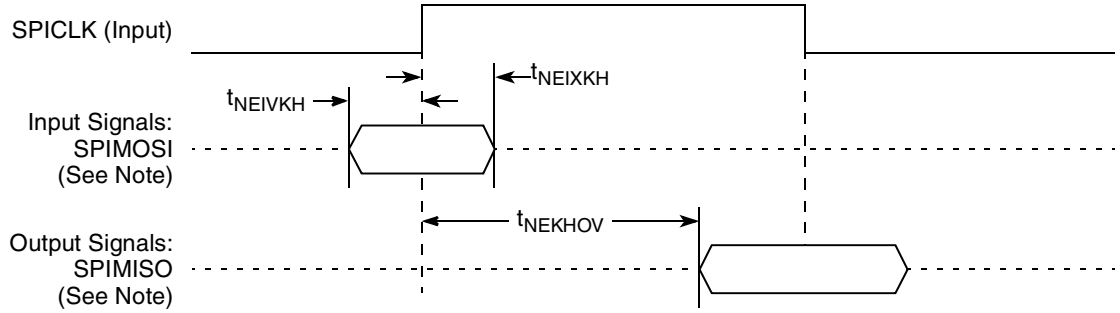


Figure 40. SPI AC Test Load

Figure 41 and Figure 42 represent the AC timing from Table 55. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

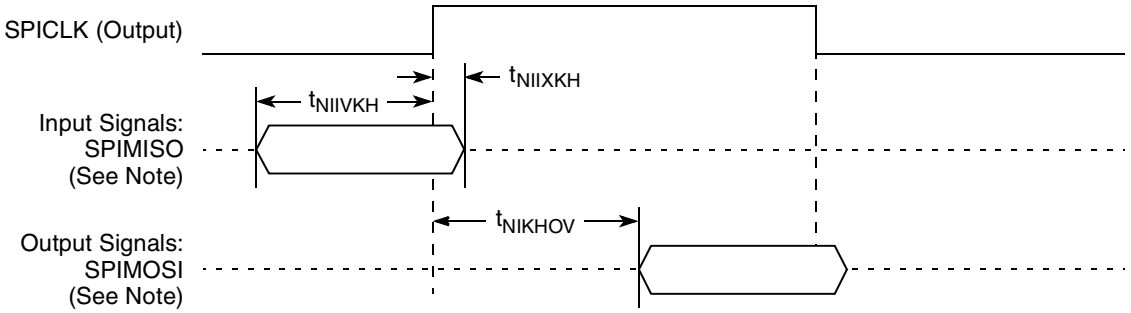
Figure 41 shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 41. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 42 shows the SPI timing in Master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 42. SPI AC Timing in Master Mode (Internal Clock) Diagram

17 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8358E.

17.1 TDM/SI DC Electrical Characteristics

Table 56 provides the DC electrical characteristics for the device TDM/SI.

Table 56. TDM/SI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V

20 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8358E.

20.1 USB DC Electrical Characteristics

Table 63 provides the DC electrical characteristics for the USB interface.

Table 63. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 µA	V_{OH}	OV_{DD} – 0.4	—	V
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current	I_{IN}	—	±10	µA

20.2 USB AC Electrical Specifications

Table 64 describes the general timing parameters of the USB interface of the device.

Table 64. USB General Timing Parameters

Parameter	Symbol[1]	Min	Max	Unit	Notes
USB clock cycle time	t_{USCK}	20.83	—	ns	Full speed 48 MHz
USB clock cycle time	t_{USCK}	166.67	—	ns	Low speed 6 MHz
Skew between TXP and TXN	t_{USTSPN}	—	5	ns	—
Skew among RXP, RXN, and RXD	$t_{USRSPND}$	—	10	ns	Full speed transitions
Skew among RXP, RXN, and RXD	t_{USRPND}	—	100	ns	Low speed transitions

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(state)(signal)}}$ for receive signals and $t_{\text{(first two letters of functional block)(state)(signal)}}$ for transmit signals. For example, $t_{USRSPND}$ symbolizes USB timing (US) for the USB receive signals skew (RS) among RXP, RXN, and RXD (PND). Also, t_{USTSPN} symbolizes USB timing (US) for the USB transmit signals skew (TS) between TXP and TXN (PN).
2. Skew measurements are done at $OV_{DD}/2$ of the rising or falling edge of the signals.

Figure 51 provide the AC test load for the USB.

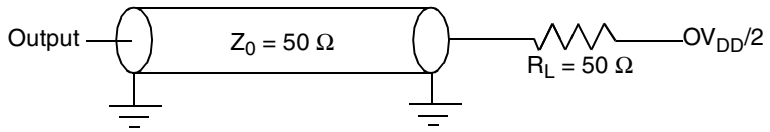


Figure 51. USB AC Test Load

Table 65. MPC8358E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_PAR/ PF[11]	AA4	I/O	OV_{DD}	—
$\overline{\text{PCI\_FRAME}}$/ PF[12]	W4	I/O	OV_{DD}	5
$\overline{\text{PCI\_TRDY}}$/ PF[13]	W5	I/O	OV_{DD}	5
$\overline{\text{PCI\_IRDY}}$/ PF[14]	AB3	I/O	OV_{DD}	5
$\overline{\text{PCI\_STOP}}$/ PF[15]	AB1	I/O	OV_{DD}	5
$\overline{\text{PCI\_DEVSEL}}$/ PF[16]	AA2	I/O	OV_{DD}	5
PCI_IDSEL/ PF[17]	U6	I/O	OV_{DD}	—
$\overline{\text{PCI\_SERR}}$/ PF[18]	AC1	I/O	OV_{DD}	5
$\overline{\text{PCI\_PERR}}$/ PF[19]	W6	I/O	OV_{DD}	5
$\overline{\text{PCI\_REQ}}$[0:2]/ PF[20:22]	R2, T4, U1	I/O	$LV_{DD}2$	—
$\overline{\text{PCI\_GNT}}$[0:2]/ PF[23:25]	T3, R5, T1	I/O	$LV_{DD}2$	—
$\overline{\text{PCI\_MODE}}$	AE5	I	OV_{DD}	—
M66EN/ CE_PF[4]	AH3	I/O	OV_{DD}	—
Local Bus Controller Interface				
LAD[0:31]	AC11, AE10, AD10, AD11, AE11, AG11, AH11, AH12, AG12, AF12, AD12, AE12, AC12, AH13, AG13, AF13, AE13, AH14, AD13, AG14, AF14, AH15, AE14, AG15, AC13, AD14, AC14, AH16, AC15, AG16, AE15, AF16	I/O	OV_{DD}	—
LDP[0:3]	AD15, AG17, AC16, AF17	I/O	OV_{DD}	—
LA[27:31]	AH17, AD16, AH18, AG18, AE17	O	OV_{DD}	—
$\overline{\text{LCS}}$[0:5]	AD18, AH20, AG20, AE19, AC18, AH21	O	OV_{DD}	—
$\overline{\text{LWE}}$[0:3]	AG21, AH22, AC20, AD19	O	OV_{DD}	—
LBCTL	AF18	O	OV_{DD}	—
LALE	AF10	O	OV_{DD}	—
LGPL0/ LSDA10/ cfg_reset_source0	AC17	I/O	OV_{DD}	—
LGPL1/ $\overline{\text{LSDWE}}$/ cfg_reset_source1	AD17	I/O	OV_{DD}	—

22 Clocking

Figure 53 shows the internal distribution of clocks within the MPC8358E.

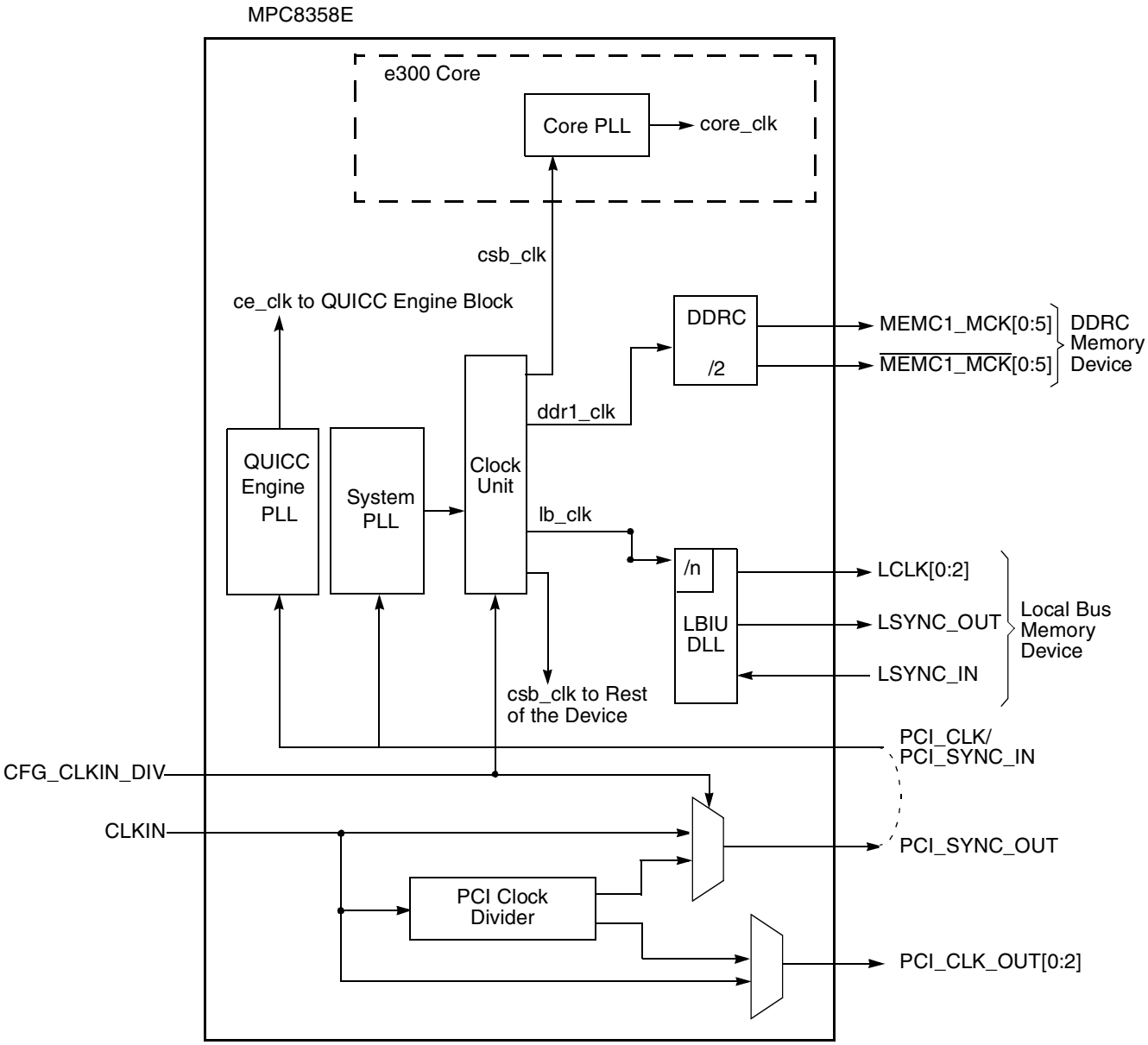


Figure 53. MPC8358E Clock Subsystem

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Note that in PCI host mode, the primary clock input also depends on whether PCI clock outputs are selected with RCWH[PCICKDRV]. When the device is configured as a PCI host device (RCWH[PCIHOST] = 1) and PCI clock output is selected (RCWH[PCICKDRV] = 1), CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration

Note that *lb_clk* is not the external local bus or DDRC2 frequency; *lb_clk* passes through the a LB clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK[0:2]). The LB clock divider ratio is controlled by LCRR[CLKDIV].

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 66 specifies which units have a configurable clock frequency.

Table 66. Configurable Clock Units

Unit	Default Frequency	Options
Security core	*csb_clk*/3	Off, *csb_clk*[1], *csb_clk*/2, *csb_clk*/3
PCI and DMA complex	csb_clk	Off, *csb_clk*

1 With limitation, only for slow csb_clk rates, up to 166 MHz.

Table 67 provides the operating frequencies for the PBGA package under recommended operating conditions (see Table 2). All frequency combinations shown in the table below may not be available. Maximum operating frequencies depend on the part ordered, see Section 25.1, "Part Numbers Fully Addressed by this Document," for part ordering details and contact your Freescale sales representative or authorized distributor for more information.

Table 67. Operating Frequencies for the PBGA Package

Characteristic[1]	400 MHz	Unit
e300 core frequency (*core_clk*)	266–400	MHz
Coherent system bus frequency (*csb_clk*)	133–266	MHz
QUICC Engine frequency (*ce_clk*)	266–400	MHz
DDR and DDR2 memory bus frequency (MCLK)[2]	100–133	MHz
Local bus frequency (LCLK*n*)[3]	16.67–133	MHz
PCI input frequency (CLKIN or PCI_CLK)	25–66.67	MHz
Security core maximum internal operating frequency	133	MHz

1 The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.

2 The DDR data rate is 2x the DDR memory bus frequency.

3 The local bus frequency is 1/2, 1/4, or 1/8 of the *lb_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBCM]).

The system VCO frequency is derived from the following equations:

- *csb_clk* = {PCI_SYNC_IN × (1 + CFG_CLKIN_DIV)} × SPMF
- System VCO Frequency = *csb_clk* × VCO divider (if both RCWL[DDRCM] and RCWL[LBCM] are cleared)
  OR
- System VCO frequency = 2 × *csb_clk* × VCO divider (if either RCWL[DDRCM] or RCWL[LBCM] are set).

As described in Section 22, "Clocking," the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 70 shows the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

Table 70. CSB Frequency Options

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk*: Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2:1				133
Low	0011	3:1			100	200
Low	0100	4:1		100	133	266
Low	0101	5:1		125	166	333
Low	0110	6:1	100	150	200	
Low	0111	7:1	116	175	233	
Low	1000	8:1	133	200	266	
Low	1001	9:1	150	225	300	
Low	1010	10:1	166	250	333	
Low	1011	11:1	183	275		
Low	1100	12:1	200	300		
Low	1101	13:1	216	325		
Low	1110	14:1	233			
Low	1111	15:1	250			
Low	0000	16:1	266			
High	0010	2:1				133
High	0011	3:1			100	200
High	0100	4:1			133	266
High	0101	5:1			166	333

22.4 Suggested PLL Configurations

To simplify the PLL configurations, the device might be separated into two clock domains. The first domain contains the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb_clk as its input clock. The second clock domain has the QUICC Engine block PLL. The clock domains are independent, and each of their PLLs are configured separately. Both of the domains has one common input clock. Table 74 shows suggested PLL configurations for 33 and 66 MHz input clocks and illustrates each of the clock domains separately. Any combination of clock domains setting with same input clock are valid. Refer to Section 22, "Clocking," for the appropriate operating frequencies for your device.

Table 74. Suggested PLL Configurations

Conf No.[1]	SPMF	CORE PLL	CEPMF	CEPDF	Input Clock Freq (MHz)	CSB Freq (MHz)	Core Freq (MHz)	QUICC Engine Freq (MHz)	400 (MHz)	533 (MHz)	667 (MHz)
33 MHz CLKIN/PCI_SYNC_IN Options											
s1	**0100**	**0000100**	æ	æ	33	133	266	—	∞	∞	∞
s2	**0100**	**0000101**	æ	æ	33	133	333	—	∞	∞	∞
s3	**0101**	**0000100**	æ	æ	33	166	333	—	∞	∞	∞
s4	**0101**	**0000101**	æ	æ	33	166	416	—	—	∞	∞
s5	**0110**	**0000100**	æ	æ	33	200	400	—	∞	∞	∞
s6	**0110**	**0000110**	æ	æ	33	200	600	—	—	—	∞
s7	**0111**	**0000011**	æ	æ	33	233	350	—	∞	∞	∞
s8	**0111**	**0000100**	æ	æ	33	233	466	—	—	∞	∞
s9	**0111**	**0000101**	æ	æ	33	233	583	—	—	—	∞
s10	**1000**	**0000011**	æ	æ	33	266	400	—	∞	∞	∞
s11	**1000**	**0000100**	æ	æ	33	266	533	—	—	∞	∞
s12	**1000**	**0000101**	æ	æ	33	266	667	—	—	—	∞
s13	**1001**	**0000010**	æ	æ	33	300	300	—	∞	∞	∞
s14	**1001**	**0000011**	æ	æ	33	300	450	—	—	∞	∞
s15	**1001**	**0000100**	æ	æ	33	300	600	—	—	—	∞
s16	**1010**	**0000010**	æ	æ	33	333	333	—	∞	∞	∞
s17	**1010**	**0000011**	æ	æ	33	333	500	—	—	∞	∞
s18	**1010**	**0000100**	æ	æ	33	333	667	—	—	—	∞
c1	æ	æ	**01001**	**0**	33	—	—	300	∞	∞	∞
c2	æ	æ	**01100**	**0**	33	—	—	400	∞	∞	∞
c3	æ	æ	**01110**	**0**	33	—	—	466	—	∞	∞
c4	æ	æ	**01111**	**0**	33	—	—	500	—	∞	∞

Table 74. Suggested PLL Configurations (continued)

Conf No.[1]	SPMF	CORE PLL	CEPMF	CEPDF	Input Clock Freq (MHz)	CSB Freq (MHz)	Core Freq (MHz)	QUICC Engine Freq (MHz)	400 (MHz)	533 (MHz)	667 (MHz)
c5	æ	æ	**10000**	**0**	33	—	—	533	—	∞	∞
c6	æ	æ	**10001**	**0**	33	—	—	566	—	—	∞
66 MHz CLKIN/PCI_SYNC_IN Options											
s1h	**0011**	**0000110**	æ	æ	66	200	400	—	∞	∞	∞
s2h	**0011**	**0000101**	æ	æ	66	200	500	—	—	∞	∞
s3h	**0011**	**0000110**	æ	æ	66	200	600	—	—	—	∞
s4h	**0100**	**0000011**	æ	æ	66	266	400	—	∞	∞	∞
s5h	**0100**	**0000100**	æ	æ	66	266	533	—	—	∞	∞
s6h	**0100**	**0000101**	æ	æ	66	266	667	—	—	—	∞
s7h	**0101**	**0000010**	æ	æ	66	333	333	—	∞	∞	∞
s8h	**0101**	**0000011**	æ	æ	66	333	500	—	—	∞	∞
s9h	**0101**	**0000100**	æ	æ	66	333	667	—	—	—	∞
c1h	æ	æ	**00101**	**0**	66	—	—	333	∞	∞	∞
c2h	æ	æ	**00110**	**0**	66	—	—	400	∞	∞	∞
c3h	æ	æ	**00111**	**0**	66	—	—	466	—	∞	∞
c4h	æ	æ	**01000**	**0**	66	—	—	533	—	∞	∞
c5h	æ	æ	**01001**	**0**	66	—	—	600	—	—	∞

[1] The Conf No. consist of prefix, an index and a postfix. The prefix “s” and “c” stands for “syset” and “ce” respectively. The postfix “h” stands for “high input clock.”The index is a serial number.

The following steps describe how to use Table 74. See Example 1.

1. Choose the up or down sections in the table according to input clock rate 33 MHz or 66 MHz.
2. Select a suitable CSB and core clock rates from Table 74. Copy the SPMF and CORE PLL configuration bits.
3. Select a suitable QUICC Engine block clock rate from Table 74. Copy the CEPMF and CEPDF configuration bits.
4. Insert the chosen SPMF, COREPLL, CEPMF and CEPDF to the RCWL fields, respectively.

Example 1. Sample Table Use

SPMF	CORE PLL	CEPMF	CEPDF	Input Clock (MHz)	CSB Freq (MHz)	Core Freq (MHz)	QUICC Engine Freq (MHz)	400 (MHz)
1000	**0000011**	**01001**	**0**	33	266	400	300	∞

23.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_J = junction temperature (°C)

T_C = case temperature of the package (°C)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

P_D = power dissipation (W)

24 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8358E. Additional information can be found in *MPC8360E/MPC8358E PowerQUICC Design Checklist* (AN3097).

24.1 System Clocking

The device includes two PLLs, as follows.

- The platform PLL ($AV_{DD}1$) generates the platform clock from the externally supplied CLKIN input. The frequency ratio between the platform and CLKIN is selected using the platform PLL ratio configuration bits as described in Section 22.1, “System PLL Configuration.”
- The e300 core PLL ($AV_{DD}2$) generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 22.2, “Core PLL Configuration.”

24.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins ($AV_{DD}1$, $AV_{DD}2$, respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in Figure 54, one to each of the five AV_{DD} pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced.

26 Document Revision History

Table 80 provides a revision history for this hardware specification.

Table 80. Revision History

Rev. Number	Date	Substantive Change(s)
3	01/2011	• Updated references to the LCRR register throughout • Removed references to DDR DLL mode in Section 6.2.2, “DDR and DDR2 SDRAM Output AC Timing Specifications.” • Changed “Junction-to-Case” to “Junction-to-Ambient” in Section 23.2.4, “Heat Sinks and Junction-to-Ambient Thermal Resistance,” and Table 76, “Heat Sinks and Junction-to-Ambient Thermal Resistance of PBGA Package,” titles.
2	03/2010	• Changed references to RCWH[PCICKEN] to RCWH[PCICKDRV]. • In Table 2, added extended temperature characteristics. • Added Figure 5, “DDR Input Timing Diagram.” • In Figure 52, “Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package,” removed watermark. • In Table 4, “MPC8358E PBGA Core Power Dissipation[1],” added row for 400/266/400 part offering. • Updated the title of Table 18,”DDR SDRAM Input AC Timing Specifications.” • In Table 19, “DDR and DDR2 SDRAM Input AC Timing Specifications Mode,” changed table subtitle. • In Table 26–Table 29, and Table 32—Table 33, changed the rise and fall time specifications to reference 20–80% and 80–20% of the voltage supply, respectively. • In Table 37, “IEEE 1588 Timer AC Specifications,” changed first parameter to “Timer clock frequency.” • In Table 44, “I2C AC Electrical Specifications,” changed units to “ns” for t_{I2DVKH}. • In Table 65 “MPC8358E PBGA Pinout Listing, added note 7: “This pin must always be tied to GND” to the TEST pin. • In Table 67, “Operating Frequencies for the PBGA Package,” and Table 78, “Part Numbering Nomenclature,” updated for 400 MHz QE part offering • In Section 4, “Clock Input Timing,” added note regarding rise/fall time on QUICC Engine block input pins. • Added Section 4.3, “Gigabit Reference Clock Input Timing.” • Updated Section 8.1.1, “10/100/1000 Ethernet DC Electrical Characteristics.” • In Section 21.3, “Pinout Listings,” added sentence stating “Refer to AN3097, ‘MPC8360/MPC8358E PowerQUICC Design Checklist,’ for proper pin termination and usage.” • In Section 22, “Clocking,” removed statement: “The OCCR[PCICDn] parameters select whether CLKIN or CLKIN/2 is driven out on the PCI_CLK_OUTn signals.” • In Section 22.1, “System PLL Configuration,” updated the system VCO frequency conditions. • In Table 78, added extended temperature characteristics.
1	12/2007	Initial release.