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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	668-BBGA Exposed Pad
Supplier Device Package	668-PBGA-PGE (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8358vraddda

1 Overview

This section describes a high-level overview including features and general operation of the MPC8358E PowerQUICC II Pro processor. A major component of this device is the e300 core, which includes 32 Kbytes of instruction and data cache and is fully compatible with the Power Architecture™ 603e instruction set. The new QUICC Engine module provides termination, interworking, and switching between a wide range of protocols including ATM, Ethernet, HDLC, and POS. The QUICC Engine module's enhanced interworking eases the transition and reduces investment costs from ATM to IP based systems. The MPC8358E has a single DDR SDRAM memory controller. The MPC8358E also offers a 32-bit PCI controller, a flexible local bus, and a dedicated security engine.

Figure 1 shows the MPC8358E block diagram.

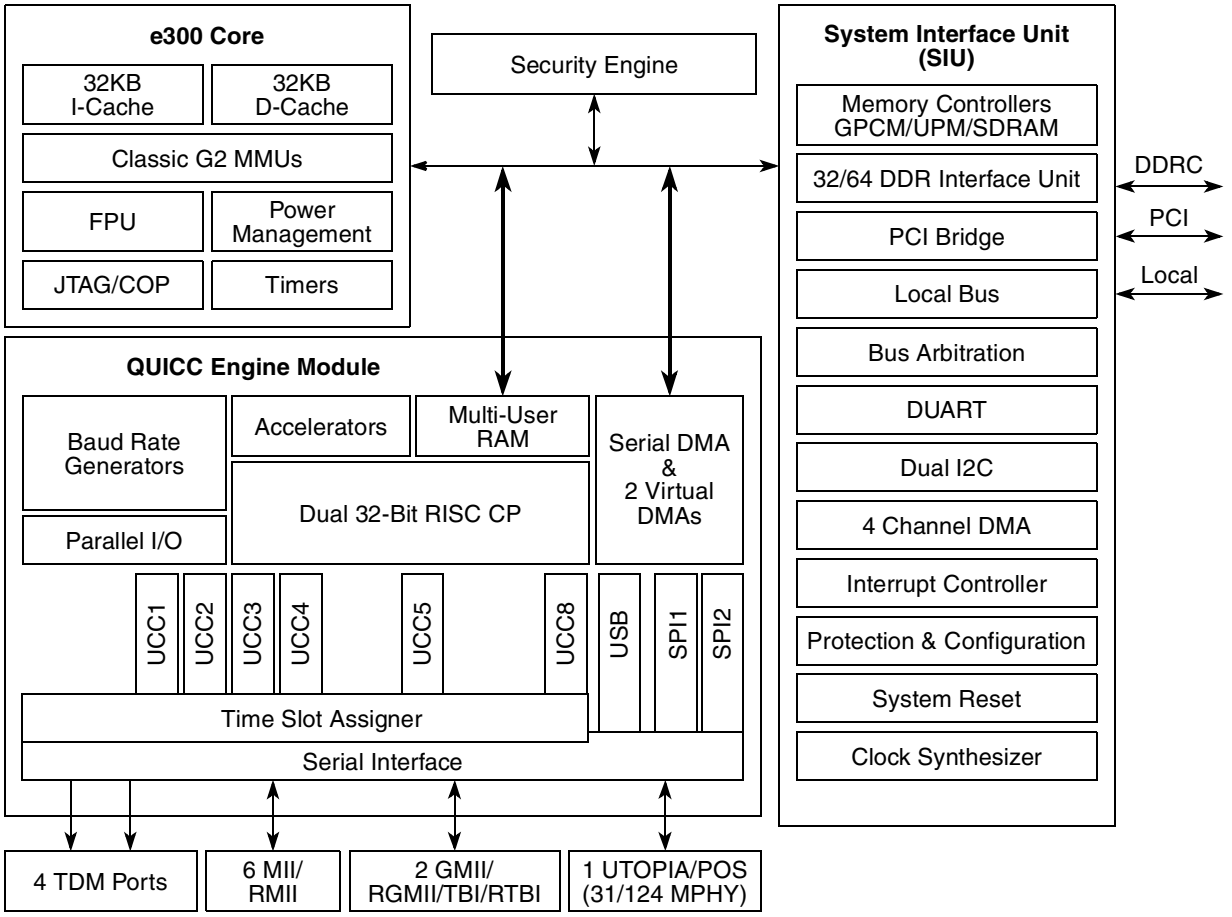
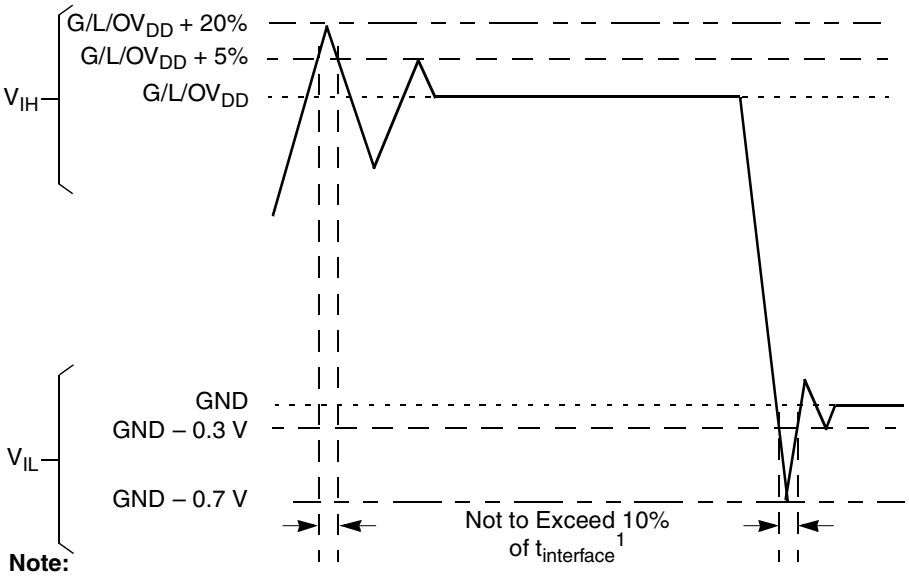


Figure 1. MPC8358E Block Diagram

Major features of the MPC8358E are as follows:

- e300 PowerPC processor core (enhanced version of the MPC603e core)
  - Operates at up to 400 MHz (for the MPC8358E)
  - High-performance, superscalar processor core
  - Floating-point, integer, load/store, system register, and branch processing units

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the device.



Note:
1. Note that $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the device for the 3.3-V signals, respectively.

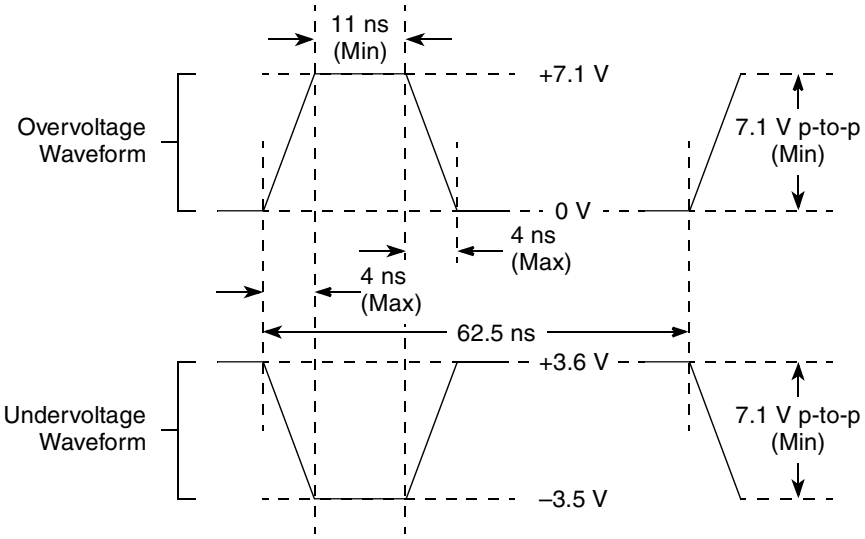


Figure 3. Maximum AC Waveforms on PCI interface for 3.3-V Signaling

Table 12. QUICC Engine Block Operating Frequency Limitations (continued)

Interface	Interface Operating Frequency (MHz)	Max Interface Bit Rate (Mbps)	Min QUICC Engine Operating Frequency[1] (MHz)	Notes
UART/async HDLC	3.68 (max internal ref clock)	115 (Kbps)	20	—
BISYNC	2 (max)	2	20	—
USB	48 (ref clock)	12	96	—

Notes:
1. The QUICC Engine module needs to run at a frequency higher than or equal to what is listed in this table.
2. 'F' is the actual interface operating frequency.
3. The bit rate limit is independent of the data bus width (that is, the same for serial, nibble, or octal interfaces).
4. TDM in high-speed mode for serial data interface.

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR and DDR2 SDRAM interface of the MPC8358E.

6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

Table 13 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the device when GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.125$	V	—
Output leakage current	I_{OZ}	—	±10	µA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—
MV_{REF} input leakage current	I_{VREF}	—	±10	µA	—

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) ± 5%.

Parameter[8]	Symbol[1]	Min	Max	Unit	Notes
ADDR/CMD output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHAS}	 2.8 3.5	—	ns	4
ADDR/CMD output hold with respect to MCK 266 MHz—DDR1 266 MHz—DDR2 200 MHz	t_{DDKHAX}	 2.6 2.8 3.5	—	ns	4
$\overline{MCS}$(n) output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHCS}	 2.8 3.5	—	ns	4
$\overline{MCS}$(n) output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHCX}	 2.7 3.5	—	ns	4
MCK to MDQS	t_{DDKHMH}	–0.75	0.6	ns	5
MDQ/MECC/MDM output setup with respect to MDQS 266 MHz 200 MHz	t_{DDKHDS}, t_{DDKLDS}	 1.0 1.2	—	ns	6
MDQ/MECC/MDM output hold with respect to MDQS 266 MHz 200 MHz	t_{DDKHDX}, t_{DDKLDX}	 1.0 1.2	—	ns	6
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	7

Table 25. RGMII/RTBI DC Electrical Characteristics (when operating at 2.5 V)

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DD} = Min	2.00	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD} = Min	GND – 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DD} = Min	1.7	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	LV_{DD} = Min	–0.3	0.70	V
Input current	I_{IN}	$0 V \le V_{IN} \le LV_{DD}$		—	±10	μA

8.2 GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1 GMII Timing Specifications

This sections describe the GMII transmit and receive AC timing specifications.

8.2.1.1 GMII Transmit AC Timing Specifications

Table 26 provides the GMII transmit AC timing specifications.

Table 26. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns	—
GTX_CLK duty cycle	t_{GTXH}/t_{GTX}	40	—	60	%	—
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX} t_{GTKHDV}	0.5 —	—	— 5.0	ns	—
GTX_CLK clock rise time, (20% to 80%)	t_{GTXR}	—	—	1.0	ns	—
GTX_CLK clock fall time, (80% to 20%)	t_{GTXF}	—	—	1.0	ns	—
GTX_CLK125 clock period	t_{G125}	—	8.0	—	ns	2
GTX_CLK125 reference clock duty cycle measured at $LV_{DD/2}$	t_{G125H}/t_{G125}	45	—	55	%	2

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This symbol is used to represent the external GTX_CLK125 signal and does not follow the original symbol naming convention.

Figure 17 shows the TBI transmit AC timing diagram.

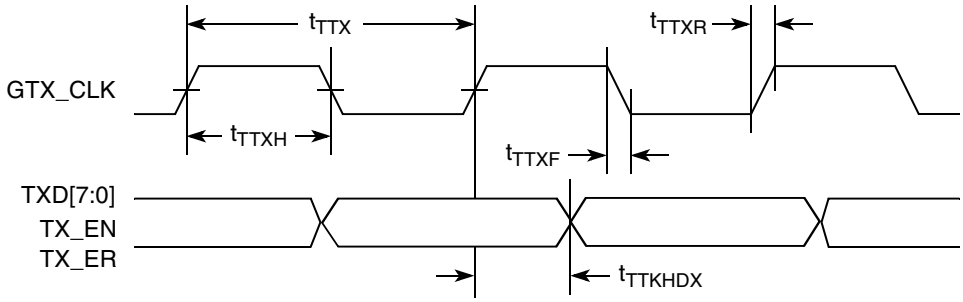


Figure 17. TBI Transmit AC Timing Diagram

8.2.4.2 TBI Receive AC Timing Specifications

Table 33 provides the TBI receive AC timing specifications.

Table 33. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
PMA_RX_CLK clock period	t_{TRX}	—	16.0	—	ns	—
PMA_RX_CLK skew	t_{SKTRX}	7.5	—	8.5	ns	—
RX_CLK duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%	—
RCG[9:0] setup time to rising PMA_RX_CLK	t_{TRDVKH}	2.5	—	—	ns	2
RCG[9:0] hold time to rising PMA_RX_CLK	t_{TRDXKH}	1.0	—	—	ns	2
RX_CLK clock rise time, V_{IL}(min) to V_{IH}(max)	t_{TRXR}	0.7	—	2.4	ns	—
RX_CLK clock fall time, V_{IH}(max) to V_{IL}(min)	t_{TRXF}	0.7	—	2.4	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. Setup and hold time of even numbered RCG are measured from riding edge of PMA_RX_CLK1. Setup and hold time of odd numbered RCG are measured from riding edge of PMA_RX_CLK0.

Figure 18 shows the TBI receive AC timing diagram.

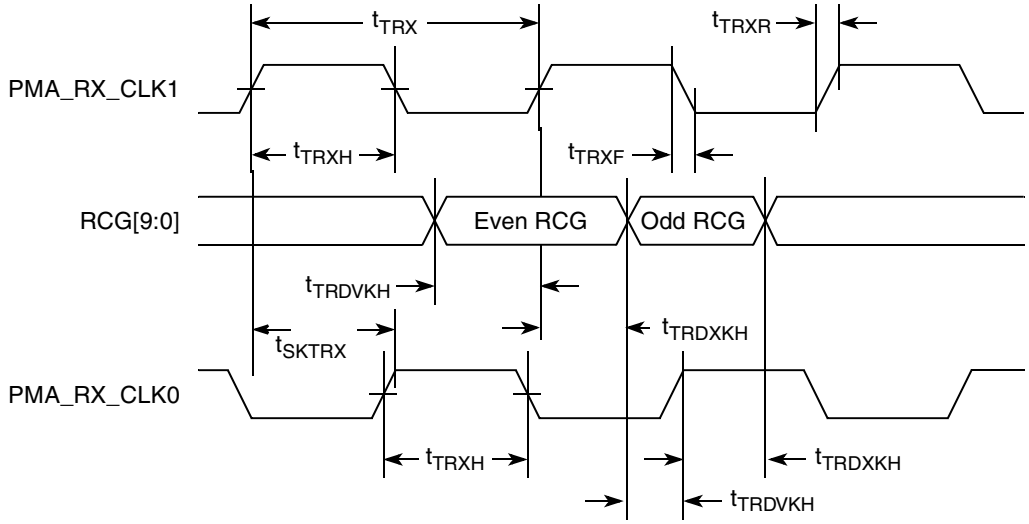


Figure 18. TBI Receive AC Timing Diagram

8.2.5 RGMII and RTBI AC Timing Specifications

Table 34 presents the RGMII and RTBI AC timing specifications.

Table 34. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	$t_{SKRGTKHDX}$ $t_{SKRGTKHDV}$	–0.5 —	—	— 0.5	ns	
Data to clock input skew (at receiver)	$t_{SKRGDXKH}$ $t_{SKRGDVKH}$	1.1 —	—	— 2.6	ns	2
Clock cycle duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 1000Base-T	t_{RGTH}/t_{RGT}	45	50	55	%	4, 5
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 5
Rise time (20–80%)	t_{RGTR}	—	—	0.75	ns	—
Fall time (20–80%)	t_{RGTF}	—	—	0.75	ns	—
GTX_CLK125 reference clock period	t_{G125}	—	8.0	—	ns	6

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, TBI, and RTBI are specified in Section 8.1, "Three-Speed Ethernet Controller (10/100/1000 Mbps)— GMII/MII/RMII/TBI/RGMII/RTBI Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 35.

Table 35. MII Management DC Electrical Characteristics When Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	OV_{DD} = Min	2.10	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	OV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±10	μA

8.3.2 MII Management AC Electrical Specifications

Table 36 provides the MII management AC timing specifications.

Table 36. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} is 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	$t_{MDTKHDX}$ $t_{MDTKHDV}$	10 —	—	— 110	ns	3
MDIO to MDC setup time	$t_{MDRDVKH}$	10	—	—	ns	—
MDIO to MDC hold time	$t_{MDRDXKH}$	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—

Figure 22 through Figure 27 show the local bus signals.

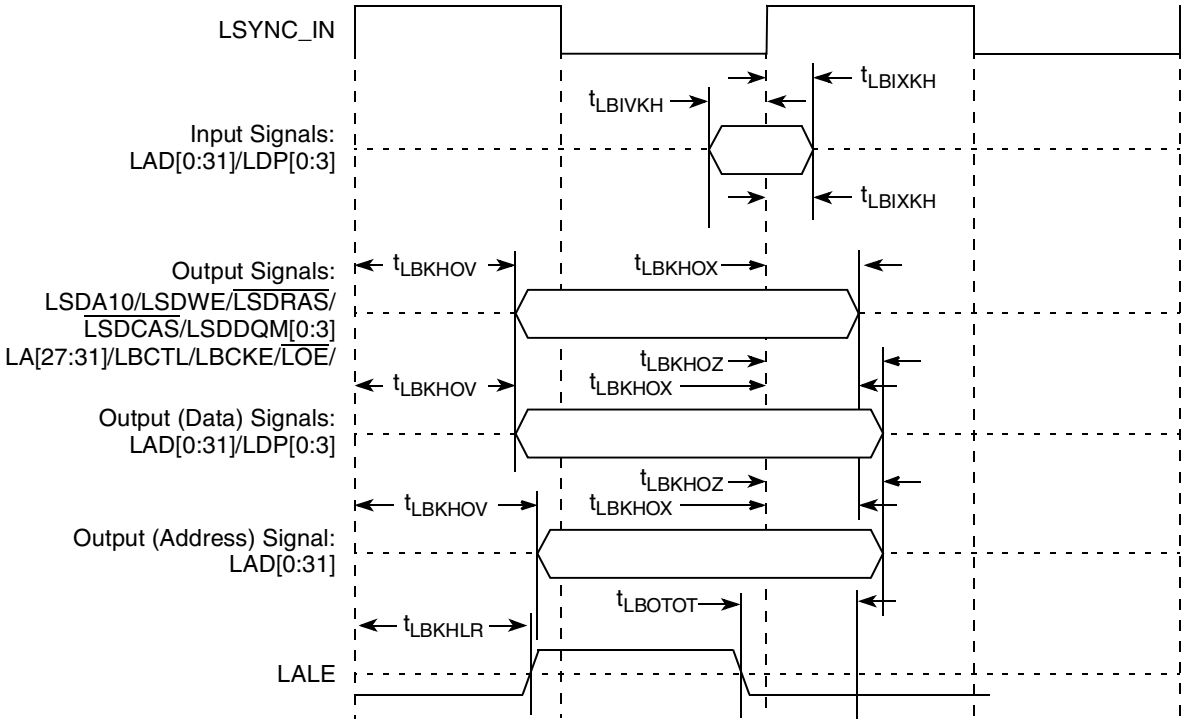


Figure 22. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)

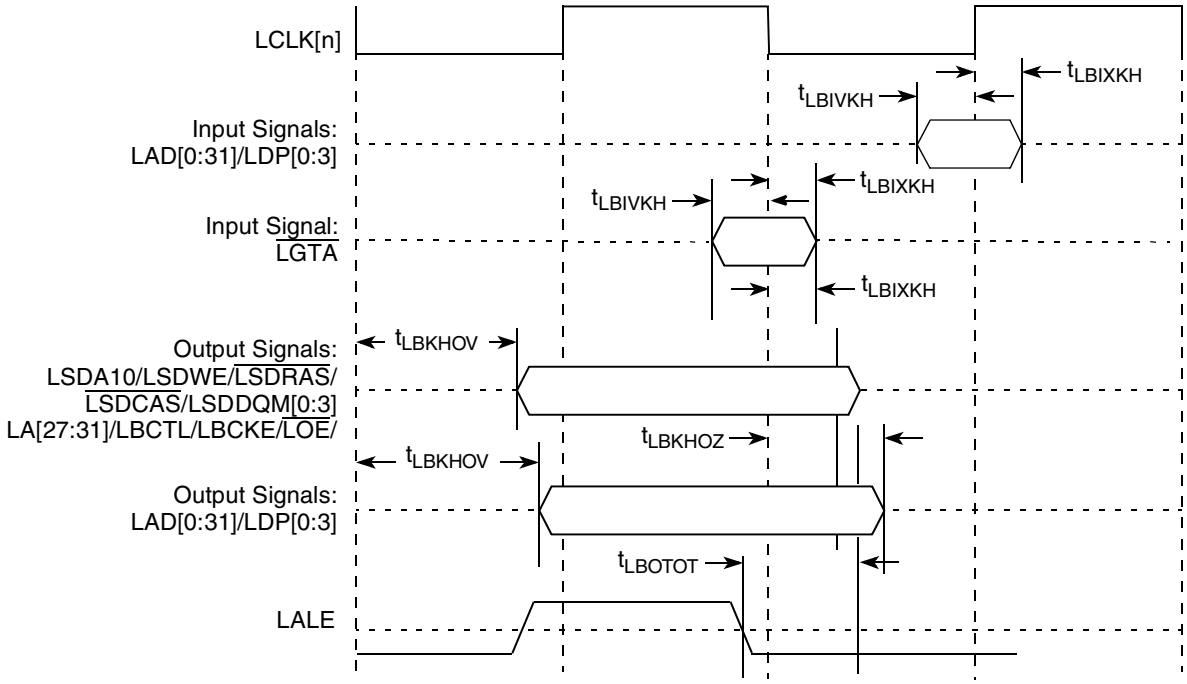


Figure 23. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)

Figure 32 provides the test access port timing diagram.

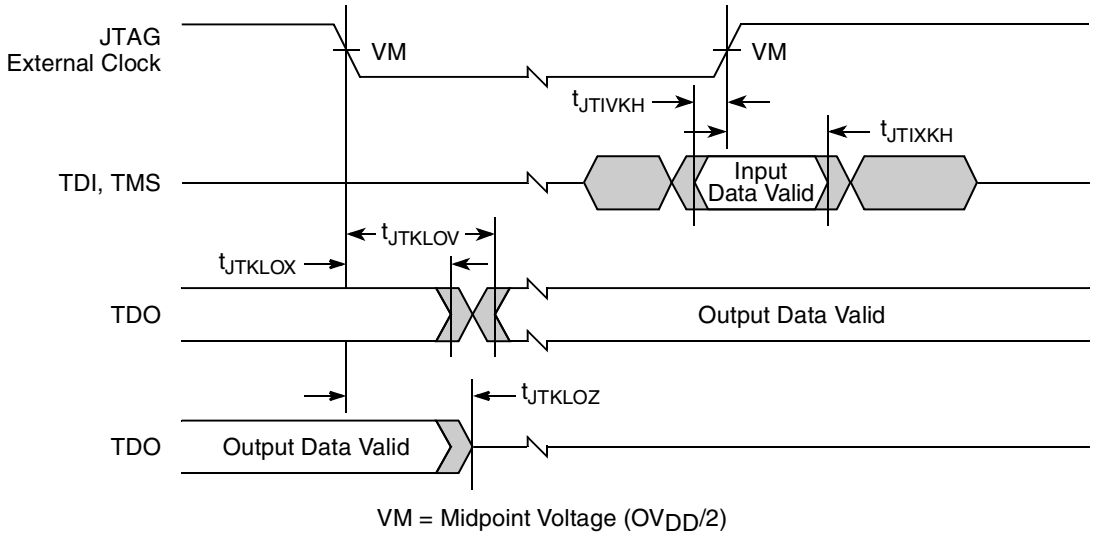


Figure 32. Test Access Port Timing Diagram

Table 47. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	7.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0.3	—	ns	2, 4

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Figure 35 provides the AC test load for PCI.

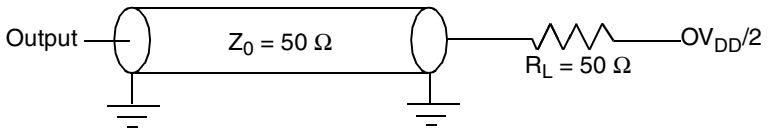


Figure 35. PCI AC Test Load

Figure 36 shows the PCI input AC timing conditions.

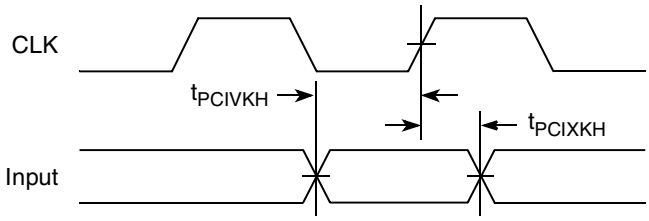


Figure 36. PCI Input AC Timing Measurement Conditions

Figure 37 shows the PCI output AC timing conditions.

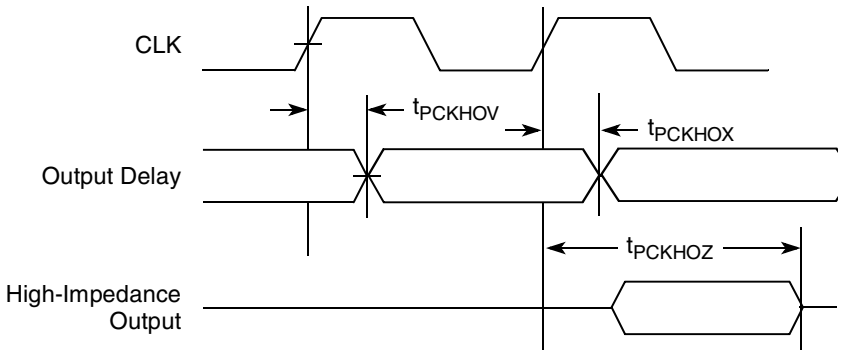


Figure 37. PCI Output AC Timing Measurement Condition

13 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8358E.

13.1 Timers DC Electrical Characteristics

Table 48 provides the DC electrical characteristics for the device timer pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 48. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±10	μA

13.2 Timers AC Timing Specifications

Table 49 provides the timer input and output AC timing specifications.

Table 49. Timers Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Typ	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

Table 59. UTOPIA AC Timing Specifications[1] (continued)

Characteristic	Symbol[2]	Min	Max	Unit	Notes
UTOPIA inputs—External clock input setup time	t_{UEIVKH}	4.2	—	ns	—
UTOPIA inputs—Internal clock input hold time	t_{UIIXKH}	2.4	—	ns	—
UTOPIA inputs—External clock input hold time	t_{UEIXKH}	1	—	ns	—

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{UIKHOX} symbolizes the UTOPIA outputs internal timing (UI) for the time t_{UTOPIA} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 45 provides the AC test load for the UTOPIA.

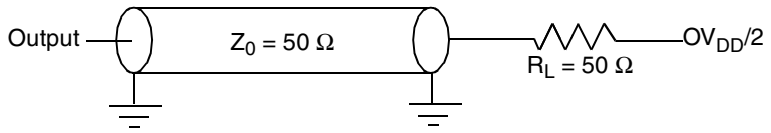


Figure 45. UTOPIA AC Test Load

Figure 46 and Figure 47 represent the AC timing from Table 55. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 46 shows the UTOPIA timing with external clock.

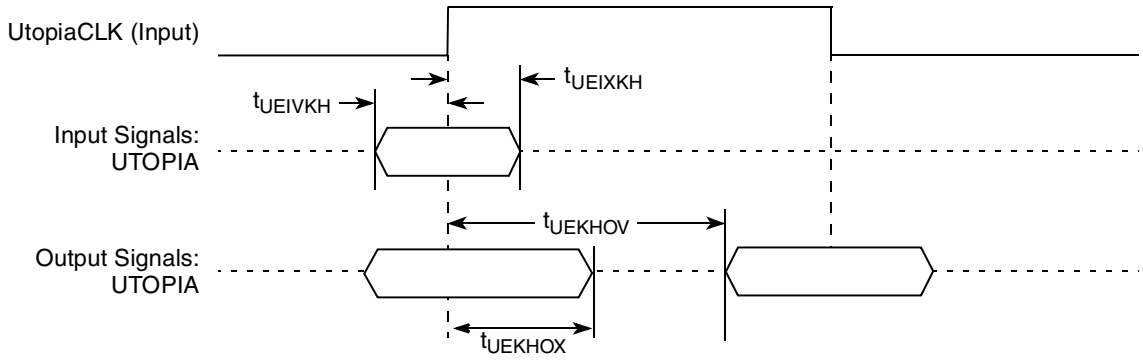


Figure 46. UTOPIA AC Timing (External Clock) Diagram

19.2 HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

Table 61 and Table 62 provide the input and output AC timing specifications for HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 61. HDLC, BISYNC, and Transparent AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—Internal clock delay	t_{HIKHOV}	0	11.2	ns
Outputs—External clock delay	t_{HEKHOV}	1	10.8	ns
Outputs—Internal clock high impedance	t_{HIKHOX}	-0.5	5.5	ns
Outputs—External clock high impedance	t_{HEKHOX}	1	8	ns
Inputs—Internal clock input setup time	t_{HIIVKH}	8.5	—	ns
Inputs—External clock input setup time	t_{HEIVKH}	4	—	ns
Inputs—Internal clock input hold time	t_{HIIXKH}	1.4	—	ns
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Table 62. Synchronous UART AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—Internal clock delay	$t_{UAIKHOV}$	0	11.3	ns
Outputs—External clock delay	$t_{UAEKHOV}$	1	14	ns
Outputs—Internal clock high impedance	$t_{UAIKHOX}$	0	11	ns
Outputs—External clock high impedance	$t_{UAEKHOX}$	1	14	ns
Inputs—Internal clock input setup time	$t_{UAIIVKH}$	6	—	ns
Inputs—External clock input setup time	$t_{UAEIVKH}$	8	—	ns
Inputs—Internal clock input hold time	$t_{UAIIXKH}$	1	—	ns
Inputs—External clock input hold time	$t_{UAEIXKH}$	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement must exclude any effect of mark on top surface of package.
6. Distance from the seating plane to the encapsulant material.

21.3 Pinout Listings

Refer to AN3097, “MPC8360/MPC8358E PowerQUICC Design Checklist,” for proper pin termination and usage.

Table 65 shows the pin list of the MPC8358E PBGA package.

Table 65. MPC8358E PBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Controller Interface				
MEMC_MDQ[0:63]	AD20, AG24, AF24, AH24, AF23, AE22, AH26, AD21, AH25, AD22, AF27, AB24, AG25, AC22, AE25, AC24, AD25, AB25, AC25, AG28, AD26, AE23, AG26, AC26, AD27, V25, AA28, AA25, Y26, W27, U24, W24, E28, H24, E26, D25, G27, H25, G26, F26, F27, F25, D26, F24, G25, E27, D27, C28, C27, F22, B26, F21, B28, E22, D24, C24, A25, E20, F20, D20, A23, C21, C23, E19	I/O	GV_{DD}	—
MEMC_MECC[0:7]	N26, N24, J26, H28, N28, P24, L26, K24	I/O	GV_{DD}	—
MEMC_MDM[0:8]	AG23, AD23, AE26, V28, G28, D28, D23, B24, U27	O	GV_{DD}	—
MEMC_MDQS[0:8]	AH23, AH27, AF28, T28, H26, E25, B25, A24, R28	I/O	GV_{DD}	—
MEMC_MBA[0:2]	V26, W28, Y28	O	GV_{DD}	—
MEMC_MA[0:14]	L25, M25, M24, K28, P28, T24, M27, R25, P25, L28, U26, M28, L27, K27, H27	O	GV_{DD}	—
MEMC_MODT[0:3]	AE21, AC19, E23, B23	—	GV_{DD}	6
$\overline{\text{MEMC\_MWE}}$	R27	O	GV_{DD}	—
$\overline{\text{MEMC\_MRAS}}$	W25	O	GV_{DD}	—
$\overline{\text{MEMC\_MCAS}}$	R24	O	GV_{DD}	—
$\overline{\text{MEMC\_MCS}}$[0:3]	T26, U28, J25, F28	O	GV_{DD}	—
MEMC_MCKE[0:1]	AD24, AE28	O	GV_{DD}	—
MEMC_MCK[0:5]	AG22, AG27, A26, C26, P26, E21	O	GV_{DD}	—
$\overline{\text{MEMC\_MCK}}$[0:5]	AF22, AF26, A27, B27, N27, D22	O	GV_{DD}	—
MDIC[0:1]	F19, AA27	I/O	GV_{DD}	11
PCI				
$\overline{\text{PCI\_INTA}}$/ PF[5]	R3	I/O	$LV_{DD}2$	2
$\overline{\text{PCI\_RESET\_OUT}}$/ PF[6]	P6	I/O	$LV_{DD}2$	—
PCI_AD[0:31]/ PG[0:31]	AB5, AC5, AG1, AA5, AF2, AD4, Y6, AF1, AE2, AC4, AD3, AE1, Y4, AC3, AD2, AD1, AB2, Y3, AA1, Y1, W1, V6, W3, V4, T5, W2, V5, V1, U4, V2, U2, T2	I/O	$LV_{DD}2$	—
$\overline{\text{PCI\_C\_BE}}$[0:3]/ PF[7:10]	Y5, AC2, Y2, U5	I/O	OV_{DD}	—

22 Clocking

Figure 53 shows the internal distribution of clocks within the MPC8358E.

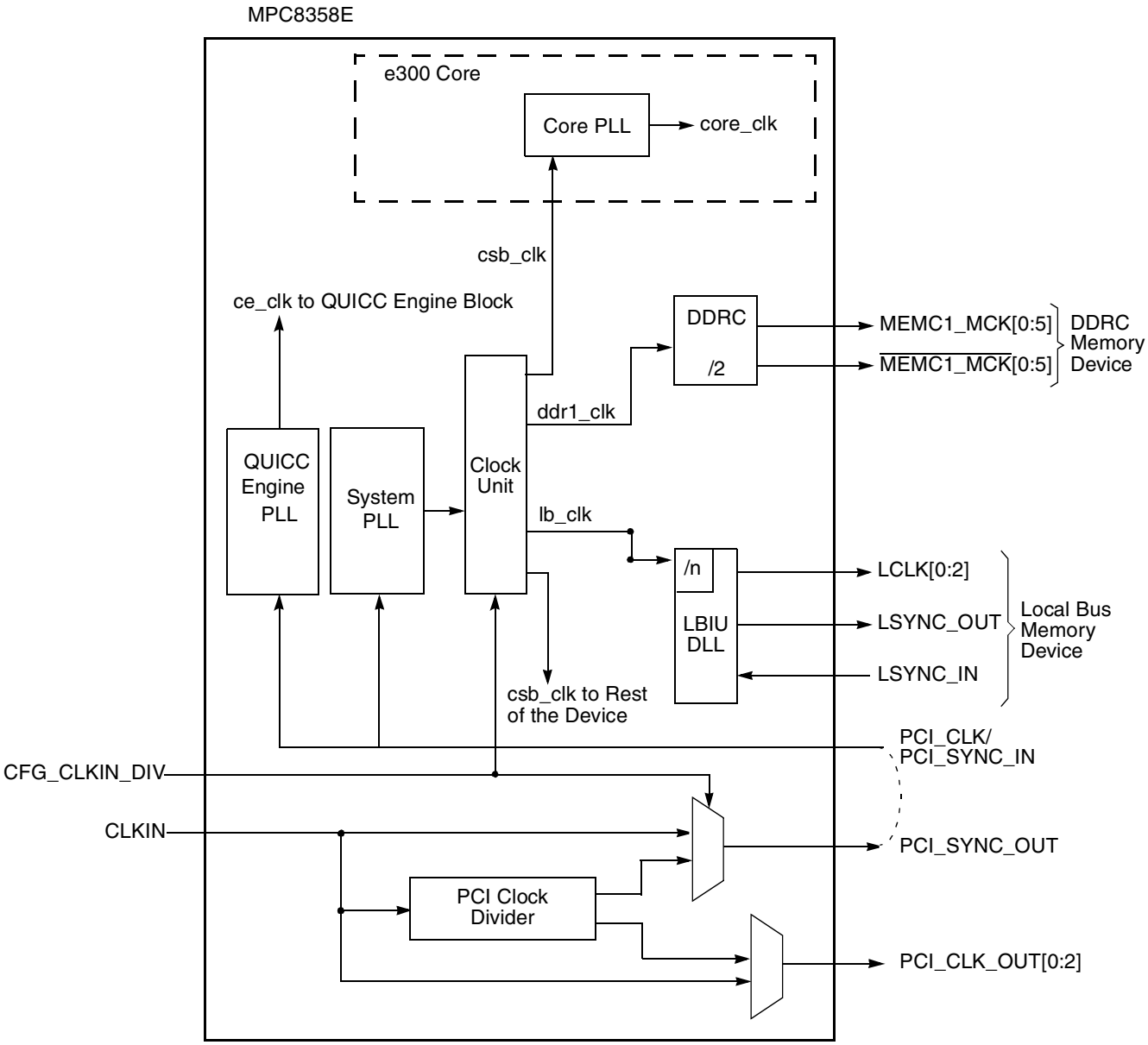


Figure 53. MPC8358E Clock Subsystem

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Note that in PCI host mode, the primary clock input also depends on whether PCI clock outputs are selected with RCWH[PCICKDRV]. When the device is configured as a PCI host device (RCWH[PCIHOST] = 1) and PCI clock output is selected (RCWH[PCICKDRV] = 1), CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration

22.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] and RCWL[SVCOD] parameters. Table 68 shows the multiplication factor encodings for the system PLL.

Table 68. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	× 16
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111	× 7
1000	× 8
1001	× 9
1010	× 10
1011	× 11
1100	× 12
1101	× 13
1110	× 14
1111	× 15

The RCWL[SVCOD] denotes the system PLL VCO internal frequency as shown in Table 69.

Table 69. System PLL VCO Divider

RCWL[SVCOD]	VCO Divider
00	4
01	8
10	2
11	Reserved

NOTE

The VCO divider must be set properly so that the system VCO frequency is in the range of 600–1400 MHz.

Table 70. CSB Frequency Options (continued)

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk*: Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
High	0110	6:1			200	
High	0111	7:1			233	
High	1000	8:1				
High	1001	9:1				
High	1010	10:1				
High	1011	11:1				
High	1100	12:1				
High	1101	13:1				
High	1110	14:1				
High	1111	15:1				
High	0000	16:1				

1 CFG_CLKIN_DIV is only used for host mode; CLKIN must be tied low and CFG_CLKIN_DIV must be pulled down (low) in agent mode.

2 CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

22.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 71 shows the encodings for RCWL[COREPLL]. COREPLL values not listed in Table 71 should be considered reserved.

Table 71. e300 Core PLL Configuration

RCWL[COREPLL]			*core_clk*:*csb_clk* Ratio	VCO divider
0–1	2–5	6		
nn	**0000**	n	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
00	**0001**	0	1:1	÷2
01	**0001**	0	1:1	÷4
10	**0001**	0	1:1	÷8
11	**0001**	0	1:1	÷8
00	**0001**	1	1.5:1	÷2
01	**0001**	1	1.5:1	÷4
10	**0001**	1	1.5:1	÷8

24.5 Output Buffer DC Impedance

The device drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 55). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

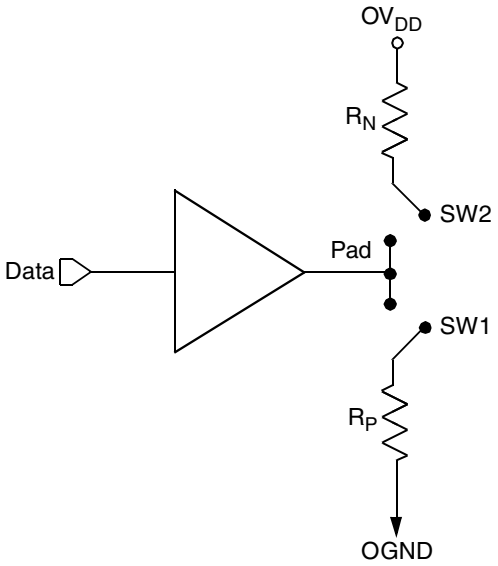


Figure 55. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 77 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 77. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	20 Target	Z_0	W
R_P	42 Target	25 Target	20 Target	Z_0	W

26 Document Revision History

Table 80 provides a revision history for this hardware specification.

Table 80. Revision History

Rev. Number	Date	Substantive Change(s)
3	01/2011	• Updated references to the LCRR register throughout • Removed references to DDR DLL mode in Section 6.2.2, “DDR and DDR2 SDRAM Output AC Timing Specifications.” • Changed “Junction-to-Case” to “Junction-to-Ambient” in Section 23.2.4, “Heat Sinks and Junction-to-Ambient Thermal Resistance,” and Table 76, “Heat Sinks and Junction-to-Ambient Thermal Resistance of PBGA Package,” titles.
2	03/2010	• Changed references to RCWH[PCICKEN] to RCWH[PCICKDRV]. • In Table 2, added extended temperature characteristics. • Added Figure 5, “DDR Input Timing Diagram.” • In Figure 52, “Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package,” removed watermark. • In Table 4, “MPC8358E PBGA Core Power Dissipation[1],” added row for 400/266/400 part offering. • Updated the title of Table 18,”DDR SDRAM Input AC Timing Specifications.” • In Table 19, “DDR and DDR2 SDRAM Input AC Timing Specifications Mode,” changed table subtitle. • In Table 26–Table 29, and Table 32—Table 33, changed the rise and fall time specifications to reference 20–80% and 80–20% of the voltage supply, respectively. • In Table 37, “IEEE 1588 Timer AC Specifications,” changed first parameter to “Timer clock frequency.” • In Table 44, “I2C AC Electrical Specifications,” changed units to “ns” for t_{I2DVKH}. • In Table 65 “MPC8358E PBGA Pinout Listing, added note 7: “This pin must always be tied to GND” to the TEST pin. • In Table 67, “Operating Frequencies for the PBGA Package,” and Table 78, “Part Numbering Nomenclature,” updated for 400 MHz QE part offering • In Section 4, “Clock Input Timing,” added note regarding rise/fall time on QUICC Engine block input pins. • Added Section 4.3, “Gigabit Reference Clock Input Timing.” • Updated Section 8.1.1, “10/100/1000 Ethernet DC Electrical Characteristics.” • In Section 21.3, “Pinout Listings,” added sentence stating “Refer to AN3097, ‘MPC8360/MPC8358E PowerQUICC Design Checklist,’ for proper pin termination and usage.” • In Section 22, “Clocking,” removed statement: “The OCCR[PCICDn] parameters select whether CLKIN or CLKIN/2 is driven out on the PCI_CLK_OUTn signals.” • In Section 22.1, “System PLL Configuration,” updated the system VCO frequency conditions. • In Table 78, added extended temperature characteristics.
1	12/2007	Initial release.