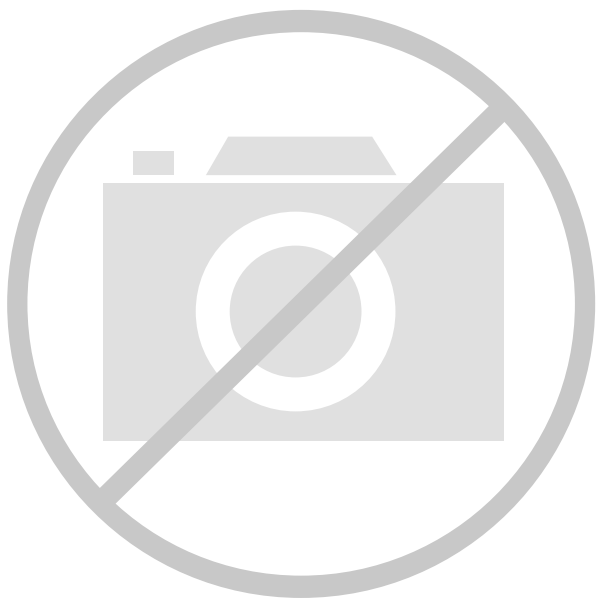




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Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	668-BBGA Exposed Pad
Supplier Device Package	668-PBGA-PGE (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8358vragdga

1 Overview

This section describes a high-level overview including features and general operation of the MPC8358E PowerQUICC II Pro processor. A major component of this device is the e300 core, which includes 32 Kbytes of instruction and data cache and is fully compatible with the Power Architecture™ 603e instruction set. The new QUICC Engine module provides termination, interworking, and switching between a wide range of protocols including ATM, Ethernet, HDLC, and POS. The QUICC Engine module's enhanced interworking eases the transition and reduces investment costs from ATM to IP based systems. The MPC8358E has a single DDR SDRAM memory controller. The MPC8358E also offers a 32-bit PCI controller, a flexible local bus, and a dedicated security engine.

Figure 1 shows the MPC8358E block diagram.

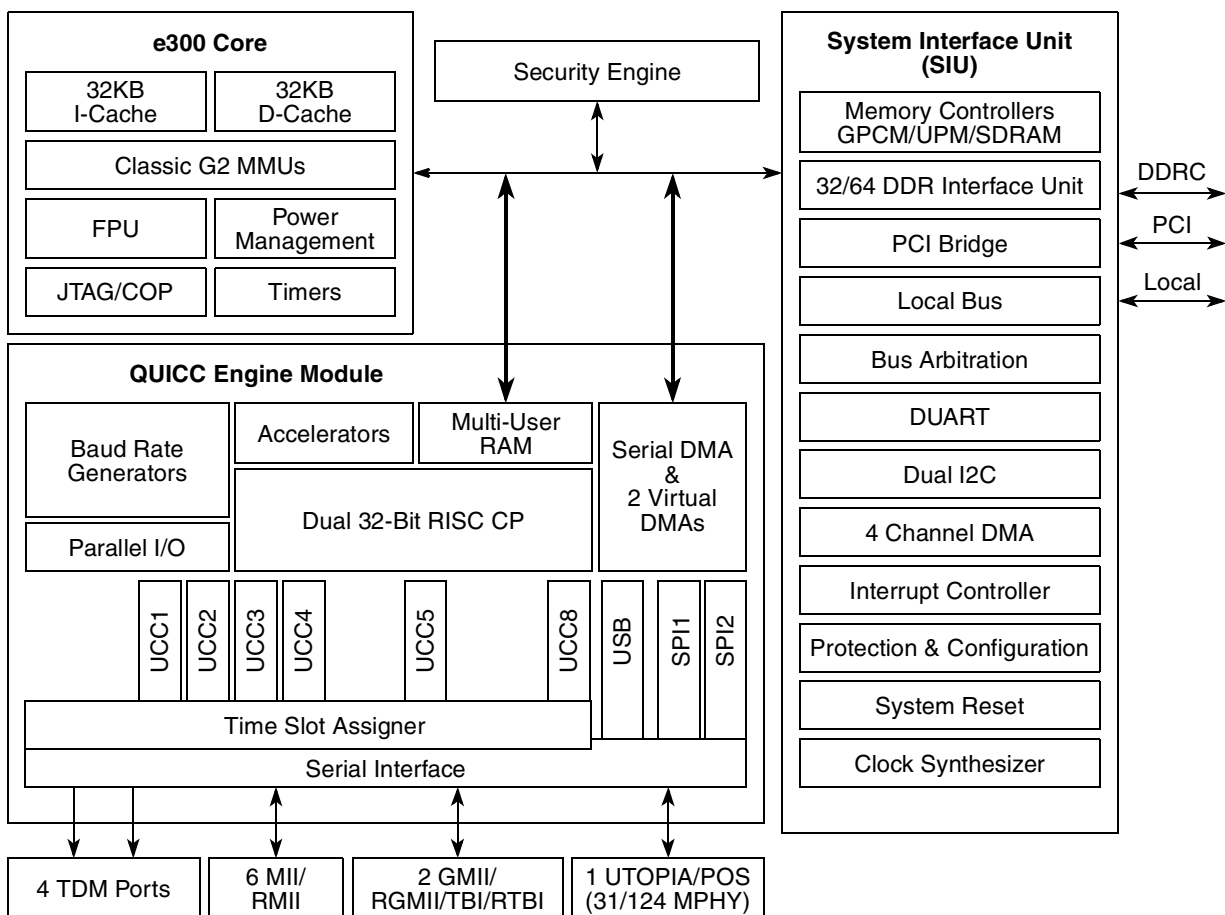


Figure 1. MPC8358E Block Diagram

Major features of the MPC8358E are as follows:

- e300 PowerPC processor core (enhanced version of the MPC603e core)
 - Operates at up to 400 MHz (for the MPC8358E)
 - High-performance, superscalar processor core
 - Floating-point, integer, load/store, system register, and branch processing units

4.1 DC Electrical Characteristics

Table 6 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the device.

Table 6. CLKIN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	$OV_{DD} + 0.3$	V
Input low voltage	—	V_{IL}	−0.3	0.4	V
CLKIN input current	$0\text{ V} \leq V_{IN} \leq OV_{DD}$	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	$0\text{ V} \leq V_{IN} \leq 0.5\text{ V}$ or $OV_{DD} - 0.5\text{ V} \leq V_{IN} \leq OV_{DD}$	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	$0.5\text{ V} \leq V_{IN} \leq OV_{DD} - 0.5\text{ V}$	I_{IN}	—	±100	μA

4.2 AC Electrical Characteristics

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 7 provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the device.

Table 7. CLKIN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
CLKIN/PCI_CLK frequency	f_{CLKIN}	—	—	66.67	MHz	1
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	—	ns	—
CLKIN/PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	±150	ps	4, 5

Notes:

- Caution:** The system, core, USB, security, and 10/100/1000 Ethernet must not exceed their respective maximum or minimum operating frequencies.
- Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 V and 2.7 V.
- Timing is guaranteed by design and characterization.
- This represents the total input jitter—short term and long term—and is guaranteed by design.
- The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at −20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.

4.3 Gigabit Reference Clock Input Timing

Table 8 provides the Gigabit reference clocks (GTX_CLK125) AC timing specifications.

Table 8. GTX_CLK125 AC Timing Specifications

At recommended operating conditions with $LV_{DD} = 2.5 \pm 0.125$ mV/ 3.3 ± 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
GTX_CLK rise and fall time $LV_{DD} = 2.5$ V $LV_{DD} = 3.3$ V	t_{G125R}/t_{G125F}	—	—	0.75 1.0	ns	1
GTX_CLK125 duty cycle GMII & TBI 1000Base-T for RGMII & RTBI	t_{G125H}/t_{G125L}	45 47	—	55 53	%	2
GTX_CLK125 jitter	—	—	—	± 150	ps	2

Notes:

1. Rise and fall times for GTX_CLK125 are measured from 0.5 and 2.0 V for $LV_{DD} = 2.5$ V and from 0.6 and 2.7 V for $LV_{DD} = 3.3$ V.
2. GTX_CLK125 is used to generate the GTX clock for the UCC Ethernet transmitter with 2% degradation. The GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by GTX_CLK. See Section 8.2.2, "MII AC Timing Specifications," Section 8.2.3, "RMII AC Timing Specifications," and Section 8.2.5, "RGMII and RTBI AC Timing Specifications" for the duty cycle for 10Base-T and 100Base-T reference clock.

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8358E.

5.1 RESET DC Electrical Characteristics

Table 9 provides the DC electrical characteristics for the RESET pins of the device.

Table 9. RESET Pins DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	−0.3	0.8	V
Input current	I_{IN}	—	—	± 10	μA
Output high voltage	V_{OH}	$I_{OH} = -8.0$ mA	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0$ mA	—	0.5	V

8.1 Three-Speed Ethernet Controller (10/100/1000 Mbps)—GMII/MII/RMII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), MII (media independent interface), RMII (reduced media independent interface), TBI (ten-bit interface), RGMII (reduced gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The MII, RMII, GMII, and TBI interfaces are only defined for 3.3 V, while the RGMII and RTBI interfaces are only defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for the MDIO and MDC are specified in [Section 8.3, “Ethernet Management Interface Electrical Characteristics.”](#)

8.1.1 10/100/1000 Ethernet DC Electrical Characteristics

The electrical characteristics specified here apply to media independent interface (MII), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), reduced media independent interface (RMII) signals, management data input/output (MDIO) and management data clock (MDC).

The MII and RMII interfaces are defined for 3.3 V, while the RGMII and RTBI interfaces can be operated at 2.5 V. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3*. The RMII interface follows the *RMII Consortium RMII Specification Version 1.2*.

Table 24. RGMII/RTBI, GMII, TBI, MII, and RMII DC Electrical Characteristics (when operating at 3.3 V)

Parameter	Symbol	Conditions		Min	Max	Unit	Notes
Supply voltage 3.3 V	V_{DD}	—		2.97	3.63	V	1
Output high voltage	V_{OH}	$I_{OH} = -4.0 \text{ mA}$	$V_{DD} = \text{Min}$	2.40	$V_{DD} + 0.3$	V	—
Output low voltage	V_{OL}	$I_{OL} = 4.0 \text{ mA}$	$V_{DD} = \text{Min}$	GND	0.50	V	—
Input high voltage	V_{IH}	—	—	2.0	$V_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	—	—	-0.3	0.90	V	—
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq V_{DD}$		—	± 10	μA	—

Note:

1. GMII/MII pins that are not needed for RGMII, RMII, or RTBI operation are powered by the OV_{DD} supply.

Figure 10 shows the GMII receive AC timing diagram.

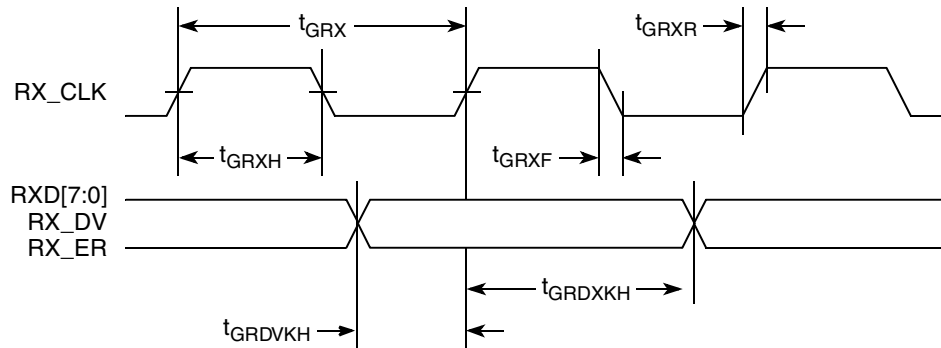


Figure 10. GMII Receive AC Timing Diagram

8.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.2.1 MII Transmit AC Timing Specifications

Table 28 provides the MII transmit AC timing specifications.

Table 28. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX} $t_{MTKHDXV}$	1 —	5	— 15	ns
TX_CLK data clock rise time, (20% to 80%)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall time, (80% to 20%)	t_{MTXF}	1.0	—	4.0	ns

Note:

- The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 18 shows the TBI receive AC timing diagram.

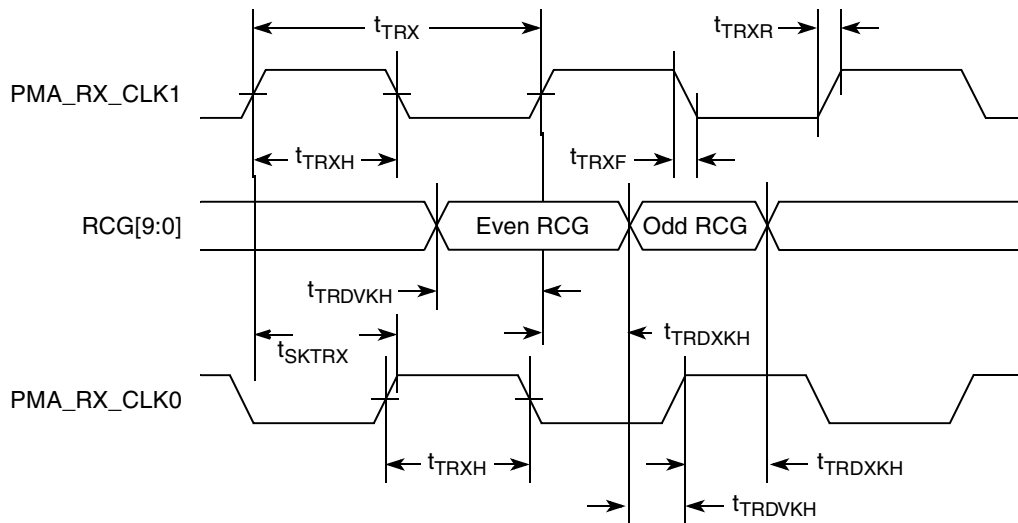


Figure 18. TBI Receive AC Timing Diagram

8.2.5 RGMII and RTBI AC Timing Specifications

Table 34 presents the RGMII and RTBI AC timing specifications.

Table 34. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with V_{DD} of 2.5 V $\pm$ 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	$t_{SKRGTKHDX}$ $t_{SKRGTKHDV}$	-0.5 —	—	— 0.5	ns	
Data to clock input skew (at receiver)	$t_{SKRGDXKH}$ $t_{SKRGDVKH}$	1.1 —	—	— 2.6	ns	2
Clock cycle duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 1000Base-T	t_{RGTH}/t_{RGT}	45	50	55	%	4, 5
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 5
Rise time (20–80%)	t_{RGTR}	—	—	0.75	ns	—
Fall time (20–80%)	t_{RGTF}	—	—	0.75	ns	—
GTX_CLK125 reference clock period	t_{G125}	—	8.0	—	ns	6

Table 37. IEEE 1588 Timer AC Specifications (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Timer alarm to output valid	t_{TMRAL}	—	—	—	2

Notes:

1. The timer can operate on rtc_clock or tmr_clock. These clocks get muxed and any one of them can be selected. The minimum and maximum requirement for both rtc_clock and tmr_clock are the same.
2. These are asynchronous signals.
3. Inputs need to be stable at least one TMR clock.

9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8358E.

9.1 Local Bus DC Electrical Characteristics

Table 38 provides the DC electrical characteristics for the local bus interface.

Table 38. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	−0.3	0.8	V
High-level output voltage, $I_{OH} = -100 \mu A$	V_{OH}	$OV_{DD} - 0.4$	—	V
Low-level output voltage, $I_{OL} = 100 \mu A$	V_{OL}	—	0.2	V
Input current	I_{IN}	—	± 10	μA

9.2 Local Bus AC Electrical Specifications

Table 39 describes the general timing parameters of the local bus interface of the device.

Table 39. Local Bus General Timing Parameters—DLL Enabled

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	—	ns	2
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	1.7	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.9	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3.0	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7

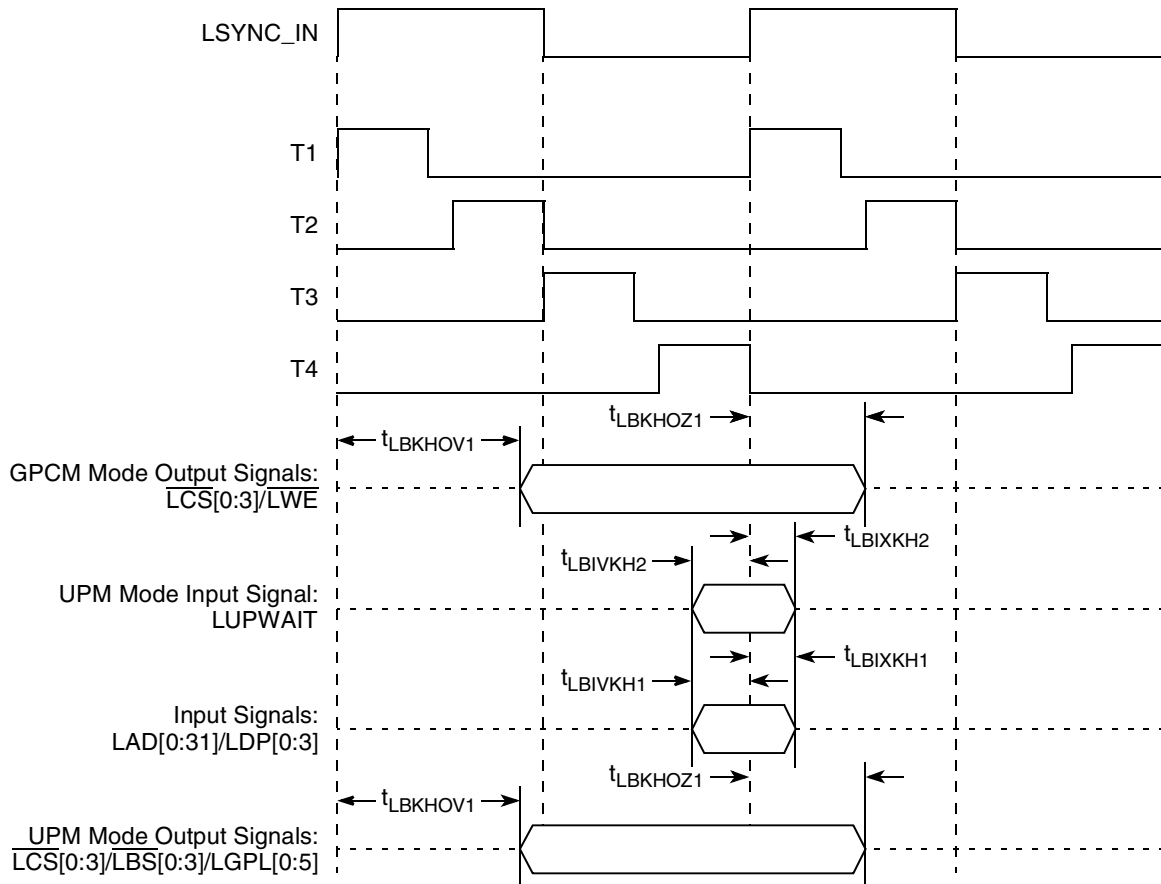


Figure 27. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (DLL Enabled)

10 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8358E.

10.1 JTAG DC Electrical Characteristics

Table 41 provides the DC electrical characteristics for the IEEE 1149.1 (JTAG) interface of the device.

Table 41. JTAG interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	$I_{OH} = -6.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 6.0 \text{ mA}$	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V
Input high voltage	V_{IH}	—	2.5	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 10	μA

10.2 JTAG AC Electrical Characteristics

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the device.

Table 42 provides the JTAG AC timing specifications as defined in Figure 29 through Figure 32.

Table 42. JTAG AC Timing Specifications (Independent of CLKIN)¹

At recommended operating conditions (see Table 2).

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock duty cycle	t_{JTKHKL}/t_{JTG}	45	55	%	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	—
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times:				ns	
Boundary-scan data TMS, TDI	t_{JTDVKH} t_{JTIVKH}	4 4	— —		4
Input hold times:				ns	
Boundary-scan data TMS, TDI	t_{JTDXKH} t_{JTIXKH}	10 10	— —		4
Valid times:				ns	
Boundary-scan data TDO	t_{JTKLDV} t_{JTKLOV}	2 2	11 11		5
Output hold times:				ns	
Boundary-scan data TDO	t_{JTKLDX} t_{JTKLOX}	2 2	— —		5
JTAG external clock to output high impedance:				ns	
Boundary-scan data TDO	t_{JTKLDZ} t_{JTKLOZ}	2 2	19 9		5, 6 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{CLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 21). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{TRST}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{CLK} .
5. Non-JTAG signal output timing with respect to t_{CLK} .
6. Guaranteed by design and characterization.

Table 47. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	7.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0.3	—	ns	2, 4

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS} , reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Figure 35 provides the AC test load for PCI.

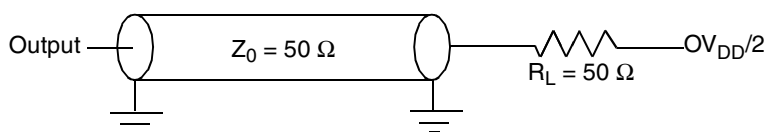

Figure 35. PCI AC Test Load

Figure 36 shows the PCI input AC timing conditions.

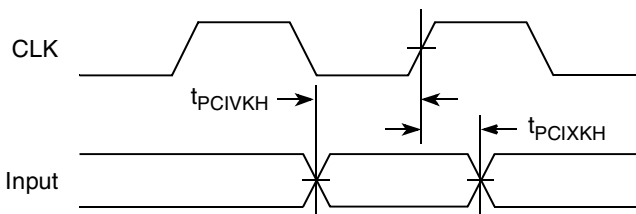

Figure 36. PCI Input AC Timing Measurement Conditions

Figure 39 provides the AC test load for the GPIO.

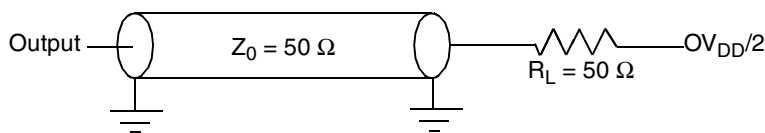


Figure 39. GPIO AC Test Load

15 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8358E.

15.1 IPIC DC Electrical Characteristics

Table 52 provides the DC electrical characteristics for the external interrupt pins of the IPIC.

Table 52. IPIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	—	—	± 10	μA
Output low voltage	V_{OL}	$I_{OL} = 6.0 \text{ mA}$	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V

Notes:

1. This table applies for pins $\overline{IRQ}[0:7]$, $\overline{IRQ_OUT}$, $\overline{MCP_OUT}$, and CE ports Interrupts.
2. $\overline{IRQ_OUT}$ and $\overline{MCP_OUT}$ are open drain pins, thus V_{OH} is not relevant for those pins.

15.2 IPIC AC Timing Specifications

Table 53 provides the IPIC input and output AC timing specifications.

Table 53. IPIC Input AC Timing Specifications¹

Characteristic	Symbol ²	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

16 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8358E.

Table 56. TDM/SI DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input low voltage	V_{IL}	—	−0.3	0.8	V
Input current	I_{IN}	$0\text{ V} \leq V_{IN} \leq OV_{DD}$	—	±10	μA

17.2 TDM/SI AC Timing Specifications

Table 57 provides the TDM/SI input and output AC timing specifications.

Table 57. TDM/SI AC Timing Specifications¹

Characteristic	Symbol ²	Min	Max ³	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	10	ns
TDM/SI outputs—External clock high impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:

- Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
- Timings are measured from the positive or negative edge of the clock, according to SIxMR [CE] and SITXCEI[TXCEIx]. See the *MPC8360E Integrated Communications Processor Family Reference Manual* for more details.

Figure 43 provides the AC test load for the TDM/SI.

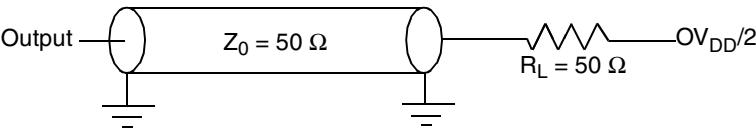


Figure 43. TDM/SI AC Test Load

Figure 44 represents the AC timing from Table 55. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 48 provides the AC test load.

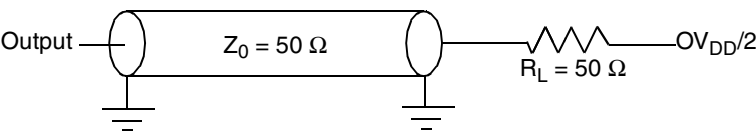
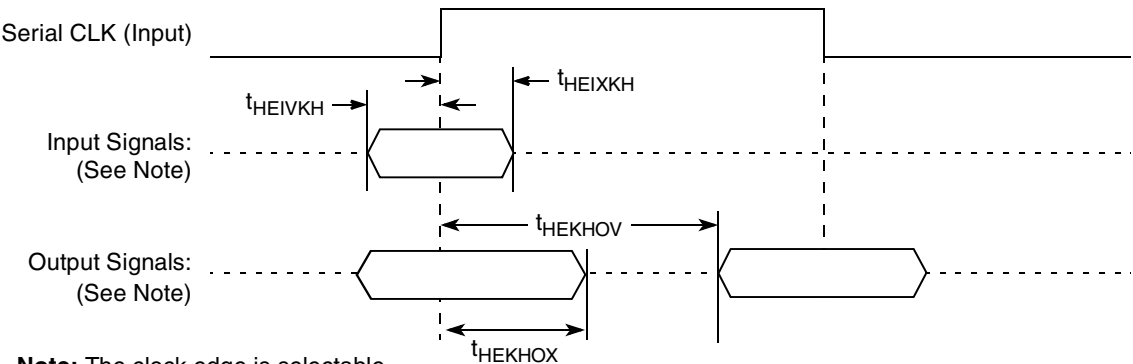


Figure 48. AC Test Load

19.3 AC Test Load

Figure 49 and Figure 50 represent the AC timing from Table 61 and Table 62. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

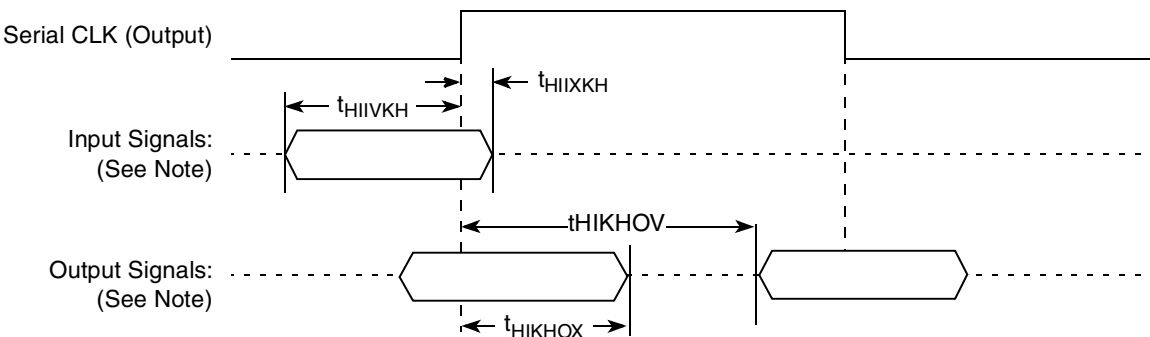
Figure 49 shows the timing with external clock.



Note: The clock edge is selectable.

Figure 49. AC Timing (External Clock) Diagram

Figure 50 shows the timing with internal clock.



Note: The clock edge is selectable.

Figure 50. AC Timing (Internal Clock) Diagram

21 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8358E is available in a plastic ball grid array (PBGA), see [Section 21.1, “Package Parameters for the PBGA Package,”](#) and [Section 21.2, “Mechanical Dimensions of the PBGA Package,”](#) for information on the package.

21.1 Package Parameters for the PBGA Package

The package parameters for rev 2.0 silicon are as provided in the following list. The package type is 29 mm x 29 mm, 668 plastic ball grid array (PBGA).

Package outline	29 mm x 29 mm
Interconnects	668
Pitch	1.00 mm
Module height (typical)	1.46 mm
Solder Balls	62 Sn/36 Pb/2 Ag (ZQ package) 95.5 Sn/0.5 Cu/4Ag (VR package)
Ball diameter (typical)	0.64 mm

input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCIOEN n] parameters enable the PCI_CLK_OUT n , respectively.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock. When the device is configured as a PCI agent device the CLKIN and the CFG_CLKIN_DIV signals should be tied to GND.

When the device is configured as a PCI host device (RCWH[PCIHOST] = 1) and PCI clock output is disabled (RCWH[PCICKDRV] = 0), clock distribution and balancing done externally on the board. Therefore, PCI_SYNC_IN is the primary input clock.

As shown in [Figure 53](#), the primary clock input (frequency) is multiplied by the QUICC Engine block phase-locked loop (PLL), the system PLL, and the clock unit to create the QUICC Engine clock (*ce_clk*), the coherent system bus clock (*csb_clk*), the internal DDRC1 controller clock (*ddr1_clk*), and the internal clock for the local bus interface unit and DDR2 memory controller (*lb_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb_clk = \{PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)\} \times SPMF$$

In PCI host mode, $PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)$ is the CLKIN frequency; in PCI agent mode, CFG_CLKIN_DIV must be pulled down (low), so $PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)$ is the PCI_CLK frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, “Reset, Clocking, and Initialization,” in the *MPC8360E PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for more information on the clock subsystem.

The *ce_clk* frequency is determined by the QUICC Engine PLL multiplication factor (RCWL[CEPMF]) and the QUICC Engine PLL division factor (RCWL[CEPDF]) according to the following equation:

$$ce_clk = (\text{primary clock input} \times CEPMF) \div (1 + CEPDF)$$

The internal *ddr1_clk* frequency is determined by the following equation:

$$ddr1_clk = csb_clk \times (1 + RCWL[DDR1CM])$$

Note that the *lb_clk* clock frequency (for DDRC2) is determined by RCWL[LBCM]. The *internal ddr1_clk* frequency is not the external memory bus frequency; *ddr1_clk* passes through the DDRC1 clock divider ($\div 2$) to create the differential DDRC1 memory bus clock outputs (MEMC1_MCK and MEMC1_MCK). However, the data rate is the same frequency as *ddr1_clk*.

The internal *lb_clk* frequency is determined by the following equation:

$$lb_clk = csb_clk \times (1 + RCWL[LBCM])$$

23.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

23.2.4 Heat Sinks and Junction-to-Ambient Thermal Resistance

In some application environments, a heat sink will be required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, airflow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Table 76 shows heat sinks and junction-to-ambient thermal resistance for PBGA package.

Table 76. Heat Sinks and Junction-to-Ambient Thermal Resistance of PBGA Package

Heat Sink Assuming Thermal Grease	Air Flow	29 × 29 mm PBGA
		Thermal Resistance
AAVID 30 × 30 × 9.4 mm Pin Fin	Natural Convection	12.6
AAVID 30 × 30 × 9.4 mm Pin Fin	1 m/s	8.2
AAVID 30 × 30 × 9.4 mm Pin Fin	2 m/s	7.0
AAVID 31 × 35 × 23 mm Pin Fin	Natural Convection	10.5
AAVID 31 × 35 × 23 mm Pin Fin	1 m/s	6.6
AAVID 31 × 35 × 23 mm Pin Fin	2 m/s	6.1
Wakefield, 53 × 53 × 25 mm Pin Fin	Natural Convection	9.0
Wakefield, 53 × 53 × 25 mm Pin Fin	1 m/s	5.6
Wakefield, 53 × 53 × 25 mm Pin Fin	2 m/s	5.1
MEI, 75 × 85 × 12 no adjacent board, extrusion	Natural Convection	9.0
MEI, 75 × 85 × 12 no adjacent board, extrusion	1 m/s	5.7
MEI, 75 × 85 × 12 no adjacent board, extrusion	2 m/s	5.1

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
473 Sapena Ct. #15
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

Figure 54 shows the PLL power supply filter circuit.

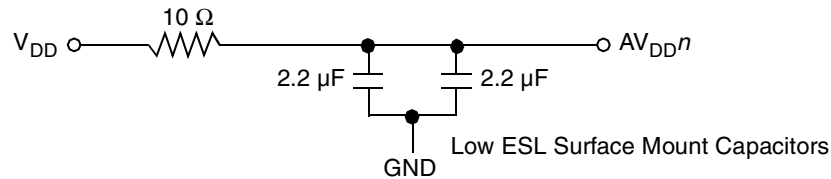


Figure 54. PLL Power Supply Filter Circuit

24.3 Decoupling Recommendations

Due to large address and data buses as well as high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the device system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} pins of the device. These decoupling capacitors should receive their power from separate V_{DD} , OV_{DD} , GV_{DD} , LV_{DD} , and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μF . Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 μF (AVX TPS tantalum or Sanyo OSCON).

24.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD} , GV_{DD} , or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} , GV_{DD} , LV_{DD} , OV_{DD} , and GND pins of the device.

24.5 Output Buffer DC Impedance

The device drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I²C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 55). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

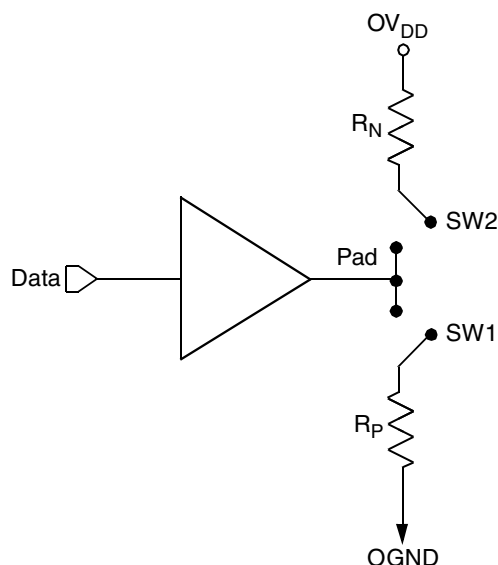


Figure 55. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term} . The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 77 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD} , nominal OV_{DD} , 105°C.

Table 77. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	20 Target	Z_0	W
R_P	42 Target	25 Target	20 Target	Z_0	W

includes an application modifier, which may specify special application conditions. Each part number also contains a revision code that refers to the die mask revision number.

Table 78. Part Numbering Nomenclature¹

<i>MPC</i>	<i>nnnn</i>	<i>e</i>	<i>t</i>	<i>pp</i>	<i>aa</i>	<i>a</i>	<i>a</i>	<i>A</i>
Product Code	Part Identifier	Encryption Acceleration	Temperature Range	Package ²	Processor Frequency ³	Platform Frequency	QUICC Engine Frequency	Die Revision
MPC	8358	Blank = Not included E = included	Blank = 0 °C T _A to 105 °C T _J C = -40°C T _A to 105°C T _J	ZQ = PBGA VR = PBGA (no lead)	e300 core speed AD = 266 MHz AG = 400 MHz	D = 266 MHz	D = 266 MHz G = 400 MHz	A = revision 2.1 silicon

¹ Not all processor, platform, and QUICC Engine block frequency combinations are supported. For available frequency combinations, contact your local Freescale sales office or authorized distributor.

² See [Section 21, "Package and Pin Listings,"](#) for more information on available package types.

³ Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

[Table 79](#) shows the SVR settings by device and package type.

Table 79. SVR Settings

Device	Package	SVR (Rev. 2.1)
MPC8358E	PBGA	0x804E_0021
MPC8358	PBGA	0x804F_0021