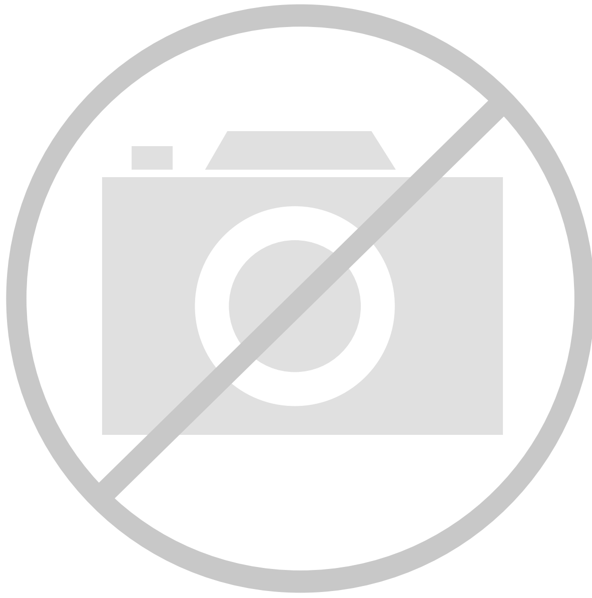

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	668-BBGA Exposed Pad
Supplier Device Package	668-PBGA-PGE (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8358zqagdda

Email: info@E-XFL.COM Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	−0.3 to 1.32	V	—
PLL supply voltage		AV_{DD}	−0.3 to 1.32	V	—
DDR and DDR2 DRAM I/O voltage DDR DDR2		GV_{DD}	 −0.3 to 2.75 −0.3 to 1.89	V	—
Three-speed Ethernet I/O, MII management voltage		LV_{DD}	−0.3 to 3.63	V	—
PCI, local bus, DUART, system control and power management, I^2C, SPI, and JTAG I/O voltage		OV_{DD}	−0.3 to 3.63	V	—
Input voltage	DDR DRAM signals	MV_{IN}	−0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV_{REF}	−0.3 to (GV_{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV_{IN}	−0.3 to (LV_{DD} + 0.3)	V	4, 5
	Local bus, DUART, CLKIN, system control and power management, I^2C, SPI, and JTAG signals	OV_{IN}	−0.3 to (OV_{DD} + 0.3)	V	3, 5
	PCI	OV_{IN}	−0.3 to (OV_{DD} + 0.3)	V	6
Storage temperature range		T_{STG}	−55 to 150	°C	—

Notes:
1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** **MV_{IN}** must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
4. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
5. (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
6. OV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	OV_{DD} = 3.3 V
PCI signals	25	
PCI output clocks (including PCI_SYNC_OUT)	42	
DDR signal	20 36 (half-strength mode)[1]	GV_{DD} = 2.5 V
DDR2 signal	18 36 (half-strength mode)[1]	GV_{DD} = 1.8 V
10/100/1000 Ethernet signals	42	LV_{DD} = 2.5/3.3 V
DUART, system control, I^2C, SPI, JTAG	42	OV_{DD} = 3.3 V
GPIO signals	42	OV_{DD} = 3.3 V LV_{DD} = 2.5/3.3 V

[1] DDR output impedance values for half strength mode are verified by design and not tested.

2.2 Power Sequencing

This section details the power sequencing considerations for the MPC8358E.

2.2.1 Power-Up Sequencing

MPC8358E does not require the core supply voltage (V_{DD} and AV_{DD}) and I/O supply voltages (GV_{DD}, LV_{DD}, and OV_{DD}) to be applied in any particular order. During the power ramp up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there may be a period of time that all input and output pins will actively be driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD}, LV_{DD}, and OV_{DD}) and assert $\overline{PORESET}$ before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V, see Figure 4.

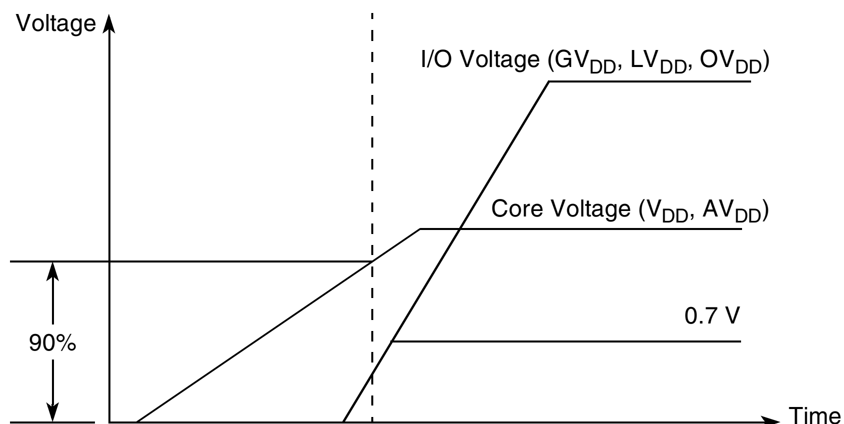


Figure 4. Power Sequencing Example

I/O voltage supplies (GV_{DD}, LV_{DD}, and OV_{DD}) do not have any ordering requirements with respect to one another.

2.2.2 Power-Down Sequencing

The MPC8358E does not require the core supply voltage and I/O supply voltages to be powered down in any particular order.

3 Power Characteristics

The estimated typical power dissipation values are shown in Table 4.

Table 4. MPC8358E PBGA Core Power Dissipation[1]

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
266	266	266	2.2	2.3	W	2, 3, 4
400	266	266	2.4	2.5	W	2, 3, 4
400	266	400	2.5	2.6	W	2, 3, 4

Notes:
1. The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see Table 5.
2. Typical power is based on a voltage of V_{DD} = 1.2 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.
3. Thermal solutions will likely need to design to a value higher than typical power on the end application, T_A target, and I/O power.
4. Maximum power is based on a voltage of V_{DD} = 1.2 V, WC process, a junction T_J = 105°C, and an artificial smoke test.

4.1 DC Electrical Characteristics

Table 6 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the device.

Table 6. CLKIN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V
CLKIN input current	$0\ V \le V_{IN} \le OV_{DD}$	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	$0\ V \le V_{IN} \le 0.5V$ or $OV_{DD} - 0.5V \le V_{IN} \le OV_{DD}$	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	$0.5\ V \le V_{IN} \le OV_{DD} - 0.5\ V$	I_{IN}	—	±100	μA

4.2 AC Electrical Characteristics

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 7 provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the device.

Table 7. CLKIN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
CLKIN/PCI_CLK frequency	f_{CLKIN}	—	—	66.67	MHz	1
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	—	ns	—
CLKIN/PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	±150	ps	4, 5

Notes:

1. **Caution:** The system, core, USB, security, and 10/100/1000 Ethernet must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.

Table 13. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input current (0 V $\le V_{IN} \le OV_{DD}$)	I_{IN}	—	±10	μA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to equal $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} cannot exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to equal MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V $\le V_{OUT} \le GV_{DD}$.

Table 14 provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

Table 14. DDR2 SDRAM Capacitance for GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Table 15 provides the recommended operating conditions for the DDR SDRAM component(s) of the device when GV_{DD}(typ) = 2.5 V.

Table 15. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.18$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.18$	V	—
Output leakage current	I_{OZ}	—	±10	μA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–15.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	15.2	—	mA	—
MV_{REF} input leakage current	I_{VREF}	—	±10	μA	—
Input current (0 V $\le V_{IN} \le OV_{DD}$)	I_{IN}	—	±10	μA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V $\le V_{OUT} \le GV_{DD}$.

Table 16 provides the DDR capacitance when GV_{DD}(typ) = 2.5 V.

Table 16. DDR SDRAM Capacitance for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR2 SDRAM interface when GV_{DD}(typ) = 1.8 V.

Table 17. DDR2 SDRAM Input AC Timing Specifications for GV_{DD}(typ) = 1.8 V

At recommended operating conditions with GV_{DD} of 1.8 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V	—

Table 18 provides the input AC timing specifications for the DDR SDRAM interface when GV_{DD}(typ) = 2.5 V.

Table 18. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V	—

Note:
1. Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 ≤ n ≤ 7) or ECC (MECC[{0...7}] if n = 8).

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) ± 5%.

Parameter[8]	Symbol[1]	Min	Max	Unit	Notes
ADDR/CMD output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHAS}	 2.8 3.5	—	ns	4
ADDR/CMD output hold with respect to MCK 266 MHz—DDR1 266 MHz—DDR2 200 MHz	t_{DDKHAX}	 2.6 2.8 3.5	—	ns	4
$\overline{MCS}$(n) output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHCS}	 2.8 3.5	—	ns	4
$\overline{MCS}$(n) output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHCX}	 2.7 3.5	—	ns	4
MCK to MDQS	t_{DDKHMH}	–0.75	0.6	ns	5
MDQ/MECC/MDM output setup with respect to MDQS 266 MHz 200 MHz	t_{DDKHDS}, t_{DDKLDS}	 1.0 1.2	—	ns	6
MDQ/MECC/MDM output hold with respect to MDQS 266 MHz 200 MHz	t_{DDKHDX}, t_{DDKLDX}	 1.0 1.2	—	ns	6
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	7

10.2 JTAG AC Electrical Characteristics

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the device.

Table 42 provides the JTAG AC timing specifications as defined in Figure 29 through Figure 32.

Table 42. JTAG AC Timing Specifications (Independent of CLKIN)[1]

At recommended operating conditions (see Table 2).

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock duty cycle	t_{JTKHKL}/t_{JTG}	45	55	%	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	—
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	t_{JTDVKH} t_{JTIVKH}	4 4	— —	ns	4
Input hold times: Boundary-scan data TMS, TDI	t_{JTDXKH} t_{JTIXKH}	10 10	— —	ns	4
Valid times: Boundary-scan data TDO	t_{JTKLDV} t_{JTKLOV}	2 2	11 11	ns	5
Output hold times: Boundary-scan data TDO	t_{JTKLDX} t_{JTKLOX}	2 2	— —	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	t_{JTKLDZ} t_{JTKLOZ}	2 2	19 9	ns	5, 6 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 21). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

Figure 28 provides the AC test load for TDO and the boundary-scan outputs of the device.

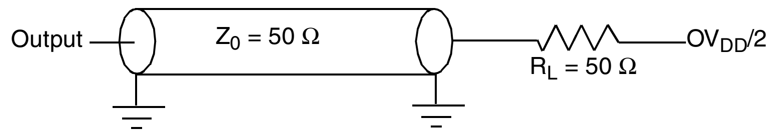


Figure 28. AC Test Load for the JTAG Interface

Figure 29 provides the JTAG clock input timing diagram.

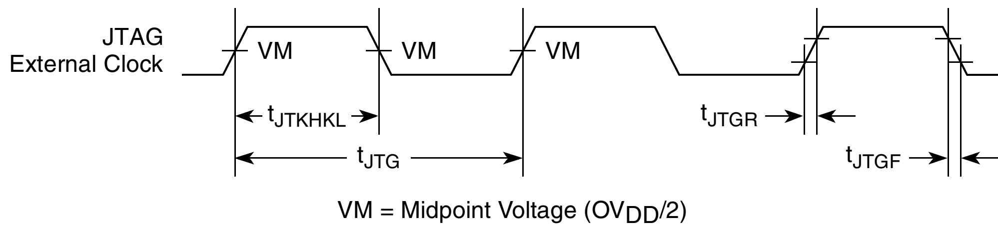


Figure 29. JTAG Clock Input Timing Diagram

Figure 30 provides the $\overline{\text{TRST}}$ timing diagram.

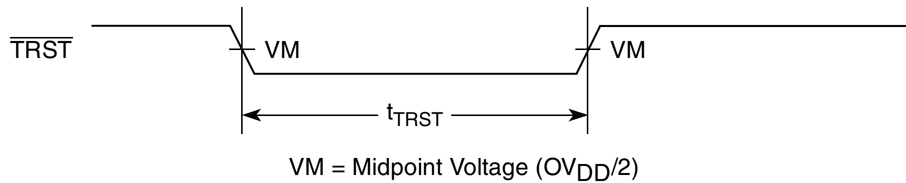


Figure 30. $\overline{\text{TRST}}$ Timing Diagram

Figure 31 provides the boundary-scan timing diagram.

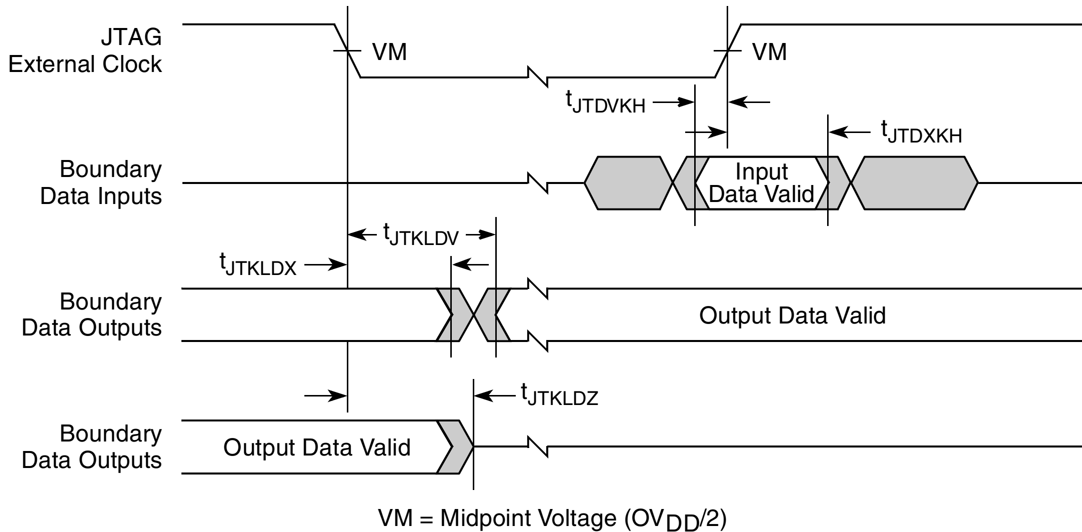
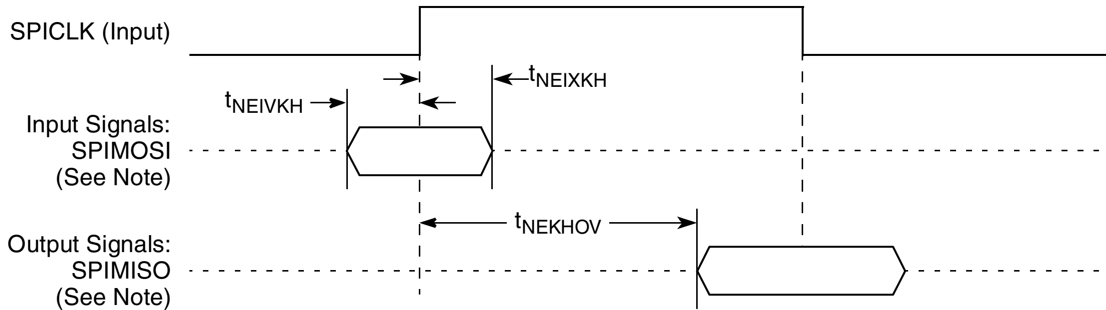


Figure 31. Boundary-Scan Timing Diagram

Figure 41 and Figure 42 represent the AC timing from Table 55. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

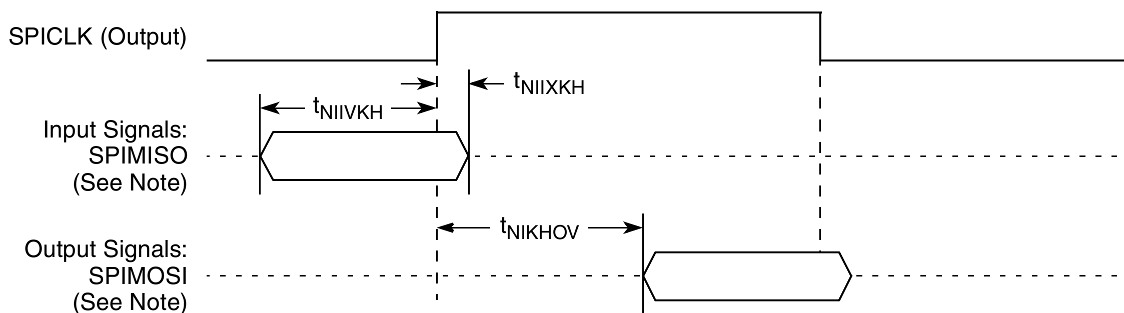
Figure 41 shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 41. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 42 shows the SPI timing in Master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 42. SPI AC Timing in Master Mode (Internal Clock) Diagram

17 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8358E.

17.1 TDM/SI DC Electrical Characteristics

Table 56 provides the DC electrical characteristics for the device TDM/SI.

Table 56. TDM/SI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V

20 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8358E.

20.1 USB DC Electrical Characteristics

Table 63 provides the DC electrical characteristics for the USB interface.

Table 63. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 µA	V_{OH}	OV_{DD} – 0.4	—	V
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current	I_{IN}	—	±10	µA

20.2 USB AC Electrical Specifications

Table 64 describes the general timing parameters of the USB interface of the device.

Table 64. USB General Timing Parameters

Parameter	Symbol[1]	Min	Max	Unit	Notes
USB clock cycle time	t_{USCK}	20.83	—	ns	Full speed 48 MHz
USB clock cycle time	t_{USCK}	166.67	—	ns	Low speed 6 MHz
Skew between TXP and TXN	t_{USTSPN}	—	5	ns	—
Skew among RXP, RXN, and RXD	$t_{USRSPND}$	—	10	ns	Full speed transitions
Skew among RXP, RXN, and RXD	t_{USRPND}	—	100	ns	Low speed transitions

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(state)(signal)}$ for receive signals and $t_{(first\ two\ letters\ of\ functional\ block)(state)(signal)}$ for transmit signals. For example, $t_{USRSPND}$ symbolizes USB timing (US) for the USB receive signals skew (RS) among RXP, RXN, and RXD (PND). Also, t_{USTSPN} symbolizes USB timing (US) for the USB transmit signals skew (TS) between TXP and TXN (PN).

2.Skew measurements are done at OV_{DD}/2 of the rising or falling edge of the signals.

Figure 51 provide the AC test load for the USB.

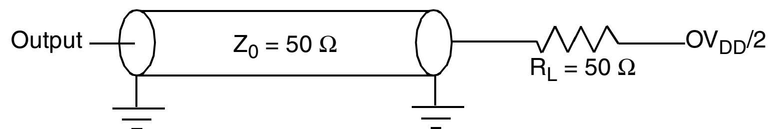


Figure 51. USB AC Test Load

Table 65. MPC8358E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TDI	AE8	I	OV_{DD}	4
TDO	AG7	O	OV_{DD}	3
TMS	AH7	I	OV_{DD}	4
$\overline{\text{TRST}}$	AG8	I	OV_{DD}	4
Test				
TEST	AF9	I	OV_{DD}	7
$\overline{\text{TEST_SEL}}$	AE27	I	GV_{DD}	9
PMC				
$\overline{\text{QUIESCE}}$	AF4	O	OV_{DD}	—
System Control				
$\overline{\text{PORESET}}$	AE9	I	OV_{DD}	—
$\overline{\text{HRESET}}$	AG9	I/O	OV_{DD}	1
$\overline{\text{SRESET}}$	AH10	I/O	OV_{DD}	2
Thermal Management				
THERM0	K25	I	GV_{DD}	—
THERM1	AA26	I	GV_{DD}	—
Power and Ground Signals				
$AV_{DD}1$	AF8	Power for LBIU DLL (1.2 V)	$AV_{DD}1$	—
$AV_{DD}2$	AH8	Power for CE PLL (1.2 V)	$AV_{DD}2$	—
$AV_{DD}5$	AB26	Power for e300 PLL (1.2 V)	$AV_{DD}5$	—
$AV_{DD}6$	AH9	Power for system PLL (1.2 V)	$AV_{DD}6$	—
GND	C16, D11, D21, E24, F7, J10, J12, J15, J16, J17, J28, K11, K13, K14, K17, K18, L4, L9, L11, L12, L13, L14, L15, L16, L17, L18, L19, L24, M10, M11, M14, M15, M18, M19, N11, N18, N25, P9, P11, P18, P19, R9, R11, R14, R15, R18, R19, R26, T10, T11, T14, T15, T18, T25, U10, U11, U18, V9, V11, V14, V15, V18, V24, V27, W18, W19, Y11, Y14, Y18, Y19, Y25, Y27, AB4, AB27, AC27, AE20, AE24, AF5, AF15, AG10	—	—	—

Table 72. QUICC Engine Block PLL Multiplication Factors (continued)

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF])
00101	0	× 5
00110	0	× 6
00111	0	× 7
01000	0	× 8
01001	0	× 9
01010	0	× 10
01011	0	× 11
01100	0	× 12
01101	0	× 13
01110	0	× 14
01111	0	× 15
10000	0	× 16
10001	0	× 17
10010	0	× 18
10011	0	× 19
10100	0	× 20
10101	0	× 21
10110	0	× 22
10111	0	× 23
11000	0	× 24
11001	0	× 25
11010	0	× 26
11011	0	× 27
11100	0	× 28
11101	0	× 29
11110	0	× 30
11111	0	× 31
00011	1	× 1.5
00101	1	× 2.5
00111	1	× 3.5
01001	1	× 4.5

Table 72. QUICC Engine Block PLL Multiplication Factors (continued)

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF])
01011	1	× 5.5
01101	1	× 6.5
01111	1	× 7.5
10001	1	× 8.5
10011	1	× 9.5
10101	1	× 10.5
10111	1	× 11.5
11001	1	× 12.5
11011	1	× 13.5
11101	1	× 14.5

Note:
1. Reserved modes are not listed.

The RCWL[CEVCOD] denotes the QUICC Engine Block PLL VCO internal frequency as shown in Table 73.

Table 73. QUICC Engine Block PLL VCO Divider

RCWL[CEVCOD]	VCO Divider
00	4
01	8
10	2
11	Reserved

NOTE

The VCO divider (RCWL[CEVCOD]) must be set properly so that the QUICC Engine block VCO frequency is in the range of 600–1400 MHz. The QUICC Engine block frequency is not restricted by the CSB and core frequencies. The CSB, core, and QUICC Engine block frequencies should be selected according to the performance requirements.

The QUICC Engine block VCO frequency is derived from the following equations:

$$ce_clk = (\text{primary clock input} \times \text{CEPMF}) \div (1 + \text{CEPDF})$$

$$\text{QE VCO Frequency} = ce_clk \times \text{VCO divider} \times (1 + \text{CEPDF})$$

22.4 Suggested PLL Configurations

To simplify the PLL configurations, the device might be separated into two clock domains. The first domain contains the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb_clk as its input clock. The second clock domain has the QUICC Engine block PLL. The clock domains are independent, and each of their PLLs are configured separately. Both of the domains has one common input clock. Table 74 shows suggested PLL configurations for 33 and 66 MHz input clocks and illustrates each of the clock domains separately. Any combination of clock domains setting with same input clock are valid. Refer to Section 22, “Clocking,” for the appropriate operating frequencies for your device.

Table 74. Suggested PLL Configurations

Conf No.[1]	SPMF	CORE PLL	CEPMF	CEPDF	Input Clock Freq (MHz)	CSB Freq (MHz)	Core Freq (MHz)	QUICC Engine Freq (MHz)	400 (MHz)	533 (MHz)	667 (MHz)
33 MHz CLKIN/PCI_SYNC_IN Options											
s1	0100	0000100	æ	æ	33	133	266	—	∞	∞	∞
s2	0100	0000101	æ	æ	33	133	333	—	∞	∞	∞
s3	0101	0000100	æ	æ	33	166	333	—	∞	∞	∞
s4	0101	0000101	æ	æ	33	166	416	—	—	∞	∞
s5	0110	0000100	æ	æ	33	200	400	—	∞	∞	∞
s6	0110	0000110	æ	æ	33	200	600	—	—	—	∞
s7	0111	0000011	æ	æ	33	233	350	—	∞	∞	∞
s8	0111	0000100	æ	æ	33	233	466	—	—	∞	∞
s9	0111	0000101	æ	æ	33	233	583	—	—	—	∞
s10	1000	0000011	æ	æ	33	266	400	—	∞	∞	∞
s11	1000	0000100	æ	æ	33	266	533	—	—	∞	∞
s12	1000	0000101	æ	æ	33	266	667	—	—	—	∞
s13	1001	0000010	æ	æ	33	300	300	—	∞	∞	∞
s14	1001	0000011	æ	æ	33	300	450	—	—	∞	∞
s15	1001	0000100	æ	æ	33	300	600	—	—	—	∞
s16	1010	0000010	æ	æ	33	333	333	—	∞	∞	∞
s17	1010	0000011	æ	æ	33	333	500	—	—	∞	∞
s18	1010	0000100	æ	æ	33	333	667	—	—	—	∞
c1	æ	æ	01001	0	33	—	—	300	∞	∞	∞
c2	æ	æ	01100	0	33	—	—	400	∞	∞	∞
c3	æ	æ	01110	0	33	—	—	466	—	∞	∞
c4	æ	æ	01111	0	33	—	—	500	—	∞	∞

23.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J – T_A$) are possible.

23.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package will be approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device. At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (°C)

T_B = board temperature at the package perimeter (°C)

$R_{\theta JA}$ = junction to board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

23.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

23.2.4 Heat Sinks and Junction-to-Ambient Thermal Resistance

In some application environments, a heat sink will be required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, airflow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Millennium Electronics (MEI) 408-436-8770
Loroco Sites
671 East Brokaw Road
San Jose, CA 95112
Internet: www.mei-millennium.com

Tyco Electronics 800-522-6752
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Wakefield Engineering 603-635-5102
33 Bridge St.
Pelham, NH 03076
Internet: www.wakefield.com

Interface material vendors include the following:

Chomerics, Inc. 781-935-4850
77 Dragon Ct.
Woburn, MA 01888-4014
Internet: www.chomerics.com

Dow-Corning Corporation 800-248-2481
Dow-Corning Electronic Materials
2200 W. Salzburg Rd.
Midland, MI 48686-0997
Internet: www.dowcorning.com

Shin-Etsu MicroSi, Inc. 888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

The Bergquist Company 800-347-4572
18930 West 78th St.
Chanhassen, MN 55317
Internet: www.bergquistcompany.com

23.3 Heat Sink Attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. Recommended maximum force on the top of the package is 10 lb force (4.5 kg force). If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

26 Document Revision History

Table 80 provides a revision history for this hardware specification.

Table 80. Revision History

Rev. Number	Date	Substantive Change(s)
3	01/2011	• Updated references to the LCRR register throughout • Removed references to DDR DLL mode in Section 6.2.2, "DDR and DDR2 SDRAM Output AC Timing Specifications." • Changed "Junction-to-Case" to "Junction-to-Ambient" in Section 23.2.4, "Heat Sinks and Junction-to-Ambient Thermal Resistance," and Table 76, "Heat Sinks and Junction-to-Ambient Thermal Resistance of PBGA Package," titles.
2	03/2010	• Changed references to RCWH[PCICKEN] to RCWH[PCICKDRV]. • In Table 2, added extended temperature characteristics. • Added Figure 5, "DDR Input Timing Diagram." • In Figure 52, "Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package," removed watermark. • In Table 4, "MPC8358E PBGA Core Power Dissipation[1]," added row for 400/266/400 part offering. • Updated the title of Table 18,"DDR SDRAM Input AC Timing Specifications." • In Table 19, "DDR and DDR2 SDRAM Input AC Timing Specifications Mode," changed table subtitle. • In Table 26–Table 29, and Table 32—Table 33, changed the rise and fall time specifications to reference 20–80% and 80–20% of the voltage supply, respectively. • In Table 37, "IEEE 1588 Timer AC Specifications," changed first parameter to "Timer clock frequency." • In Table 44, "I2C AC Electrical Specifications," changed units to "ns" for t_{I2DVKH}. • In Table 65 "MPC8358E PBGA Pinout Listing, added note 7: "This pin must always be tied to GND" to the TEST pin. • In Table 67, "Operating Frequencies for the PBGA Package," and Table 78, "Part Numbering Nomenclature," updated for 400 MHz QE part offering • In Section 4, "Clock Input Timing," added note regarding rise/fall time on QUICC Engine block input pins. • Added Section 4.3, "Gigabit Reference Clock Input Timing." • Updated Section 8.1.1, "10/100/1000 Ethernet DC Electrical Characteristics." • In Section 21.3, "Pinout Listings," added sentence stating "Refer to AN3097, 'MPC8360/MPC8358E PowerQUICC Design Checklist,' for proper pin termination and usage." • In Section 22, "Clocking," removed statement: "The OCCR[PCICDn] parameters select whether CLKIN or CLKIN/2 is driven out on the PCI_CLK_OUTn signals." • In Section 22.1, "System PLL Configuration," updated the system VCO frequency conditions. • In Table 78, added extended temperature characteristics.
1	12/2007	Initial release.

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