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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	668-BBGA Exposed Pad
Supplier Device Package	668-PBGA-PGE (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8358zqagdga

  - Multiple master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
  - System initialization data is optionally loaded from I^2C-1 EPROM by boot sequencer embedded hardware
- DMA controller
  - Four independent virtual channels
  - Concurrent execution across multiple channels with programmable bandwidth control
  - All channels accessible by local core and remote PCI masters
  - Misaligned transfer capability
  - Data chaining and direct mode
  - Interrupt on completed segment and chain
  - DMA external handshake signals: $\overline{\text{DMA\_DREQ}}$[0:3]/$\overline{\text{DMA\_DACK}}$[0:3]/$\overline{\text{DMA\_DONE}}$[0:3]. There is one set for each DMA channel. The pins are multiplexed to the parallel IO pins with other QE functions.
- DUART
  - Two 4-wire interfaces (RxD, TxD, RTS, CTS)
  - Programming model compatible with the original 16450 UART and the PC16550D
- System timers
  - Periodic interrupt timer
  - Real-time clock
  - Software watchdog timer
  - Eight general-purpose timers
- IEEE Std. 1149.1™-compliant, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8358E. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the device. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	1.2 V ± 60 mV	V	1
PLL supply voltage	AV_{DD}	1.2 V ± 60 mV	V	1
DDR and DDR2 DRAM I/O supply voltage DDR DDR2	GV_{DD}	 2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Three-speed Ethernet I/O supply voltage	$LV_{DD}0$	3.3 V ± 330 mV 2.5 V ± 125 mV	V	—
Three-speed Ethernet I/O supply voltage	$LV_{DD}1$	3.3 V ± 330 mV 2.5 V ± 125 mV	V	—
Three-speed Ethernet I/O supply voltage	$LV_{DD}2$	3.3 V ± 330 mV 2.5 V ± 125 mV	V	—
PCI, local bus, DUART, system control and power management, I^2C, SPI, and JTAG I/O voltage	OV_{DD}	3.3 V ± 330 mV	V	—
Junction temperature	T_J	0 to 105 –40 to 105	°C	—

Notes:
1. GV_{DD}, LV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.

Table 9. RESET Pins DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:
1. This table applies for pins $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, and $\overline{\text{QUIESCE}}$.
2. $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

5.2 RESET AC Electrical Characteristics

This section describes the AC electrical specifications for the reset initialization timing requirements of the device. Table 10 provides the reset initialization AC timing specifications for the DDR SDRAM component(s).

Table 10. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$ (input) to activate reset flow	32	—	$t_{PCI\_SYNC\_IN}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to CLKIN when the device is in PCI host mode	32	—	t_{CLKIN}	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_SYNC_IN when the device is in PCI agent mode	32	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$/$\overline{\text{SRESET}}$ assertion (output)	512	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$ negation to $\overline{\text{SRESET}}$ negation (output)	16	—	$t_{PCI\_SYNC\_IN}$	1
Input setup time for POR config signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR config signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode	4	—	$t_{PCI\_SYNC\_IN}$	1
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	
Time for the device to turn off POR config signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the device to turn on POR config signals with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Notes:
1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8360E PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for more details.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the device is in PCI host mode. See the *MPC8360E PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for more details.
3. POR config signals consists of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications Mode

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
MDQS—MDQ/MECC input skew per byte 266 MHz 200 MHz	t_{DISKEW}	 –1125 –1250	 1125 1250	ps	1, 2

Notes:
1. AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.
2. Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 ≤ n ≤ 7) or ECC (MECC[{0...7}] if n = 8).

Figure 5 shows the input timing diagram for the DDR controller.

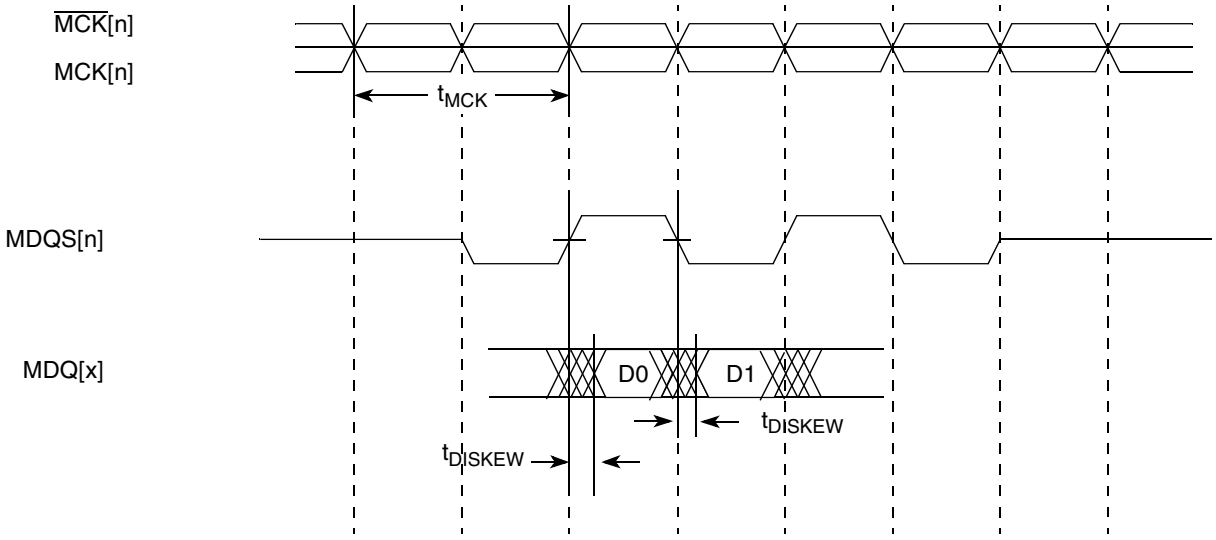

Figure 5. DDR Input Timing Diagram

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20 and Table 21 provide the output AC timing specifications and measurement conditions for the DDR and DDR2 SDRAM interface.

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) ± 5%.

Parameter[8]	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time, (MCK[n]/$\overline{\text{MCK}}$[n] crossing)	t_{MCK}	6	10	ns	2
Skew between any MCK to ADDR/CMD 266 MHz 200 MHz	t_{AOSKEW}	 –1.1 –1.2	 0.3 0.4	ns	3

Figure 7 provides the AC test load for the DDR bus.

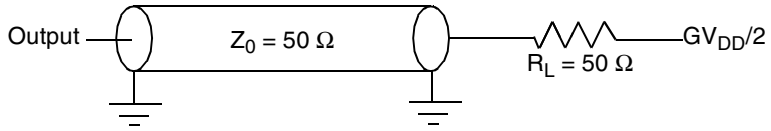

Figure 7. DDR AC Test Load

Table 21. DDR and DDR2 SDRAM Measurement Conditions

Symbol	DDR	DDR2	Unit	Notes
V_{TH}	MV_{REF} ± 0.31 V	MV_{REF} ± 0.25 V	V	1
V_{OUT}	0.5 × GV_{DD}	0.5 × GV_{DD}	V	2

Notes:
1. Data input threshold measurement point.
2. Data output measurement point.

Figure 8 shows the DDR SDRAM output timing diagram for source synchronous mode.

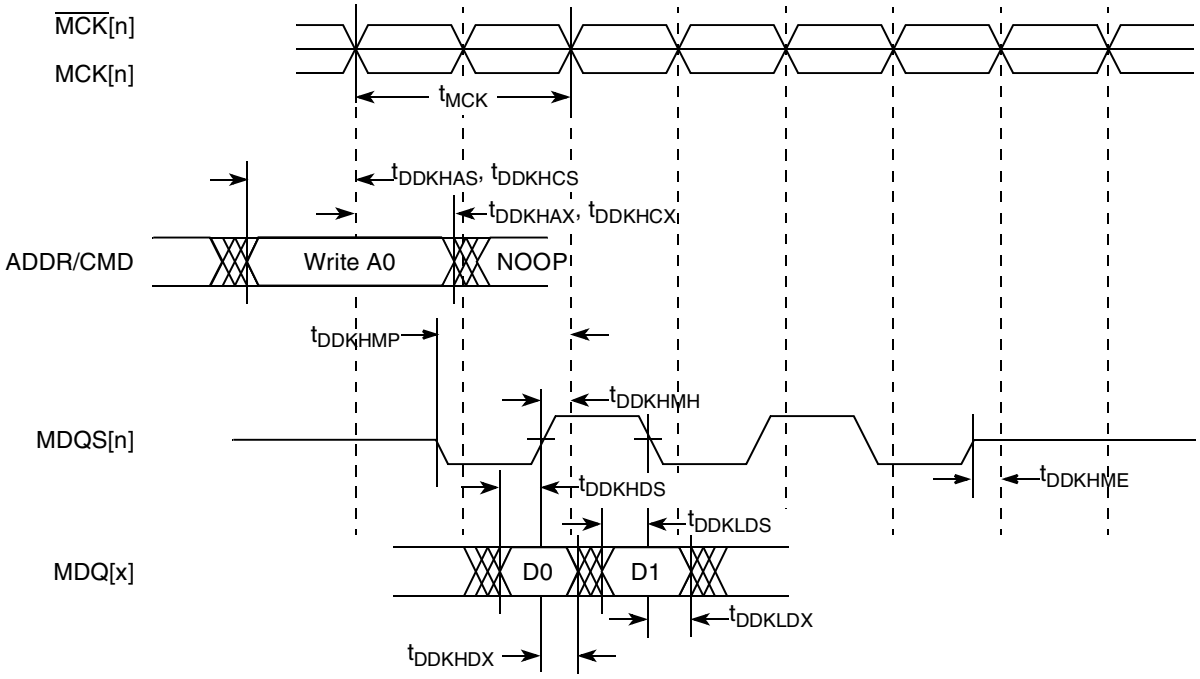

Figure 8. DDR SDRAM Output Timing Diagram for Source Synchronous Mode

8.1 Three-Speed Ethernet Controller (10/100/1000 Mbps)—GMII/MII/RMII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), MII (media independent interface), RMII (reduced media independent interface), TBI (ten-bit interface), RGMII (reduced gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The MII, RMII, GMII, and TBI interfaces are only defined for 3.3 V, while the RGMII and RTBI interfaces are only defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for the MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

8.1.1 10/100/1000 Ethernet DC Electrical Characteristics

The electrical characteristics specified here apply to media independent interface (MII), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), reduced media independent interface (RMII) signals, management data input/output (MDIO) and management data clock (MDC).

The MII and RMII interfaces are defined for 3.3 V, while the RGMII and RTBI interfaces can be operated at 2.5 V. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3*. The RMII interface follows the *RMII Consortium RMII Specification Version 1.2*.

Table 24. RGMII/RTBI, GMII, TBI, MII, and RMII DC Electrical Characteristics (when operating at 3.3 V)

Parameter	Symbol	Conditions		Min	Max	Unit	Notes
Supply voltage 3.3 V	LV_{DD}	—		2.97	3.63	V	1
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	LV_{DD} = Min	2.40	LV_{DD} + 0.3	V	—
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	LV_{DD} = Min	GND	0.50	V	—
Input high voltage	V_{IH}	—	—	2.0	LV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	—	—	–0.3	0.90	V	—
Input current	I_{IN}	$0 V \le V_{IN} \le LV_{DD}$		—	±10	μA	—

Note:
1. GMII/MII pins that are not needed for RGMII, RMII, or RTBI operation are powered by the OV_{DD} supply.

Figure 9 shows the GMII transmit AC timing diagram.

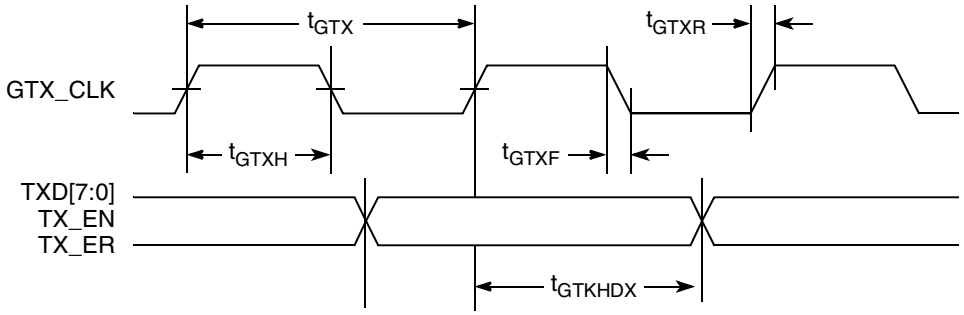

Figure 9. GMII Transmit AC Timing Diagram

8.2.1.2 GMII Receive AC Timing Specifications

Table 27 provides the GMII receive AC timing specifications.

Table 27. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
RX_CLK clock period	t_{GRX}	—	8.0	—	ns	—
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	%	—
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns	—
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.3	—	—	ns	—
RX_CLK clock rise time, (20% to 80%)	t_{GRXR}	—	—	1.0	ns	—
RX_CLK clock fall time, (80% to 20%)	t_{GRXF}	—	—	1.0	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 13 shows the MII receive AC timing diagram.

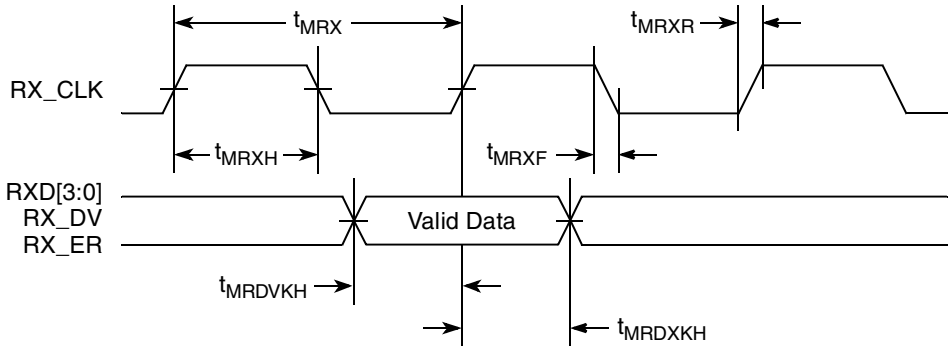

Figure 13. MII Receive AC Timing Diagram

8.2.3 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.3.1 RMII Transmit AC Timing Specifications

Table 30 provides the RMII transmit AC timing specifications.

Table 30. RMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$ $t_{RMTKHDV}$	2 —	—	— 10	ns
REF_CLK data clock rise time	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall time	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

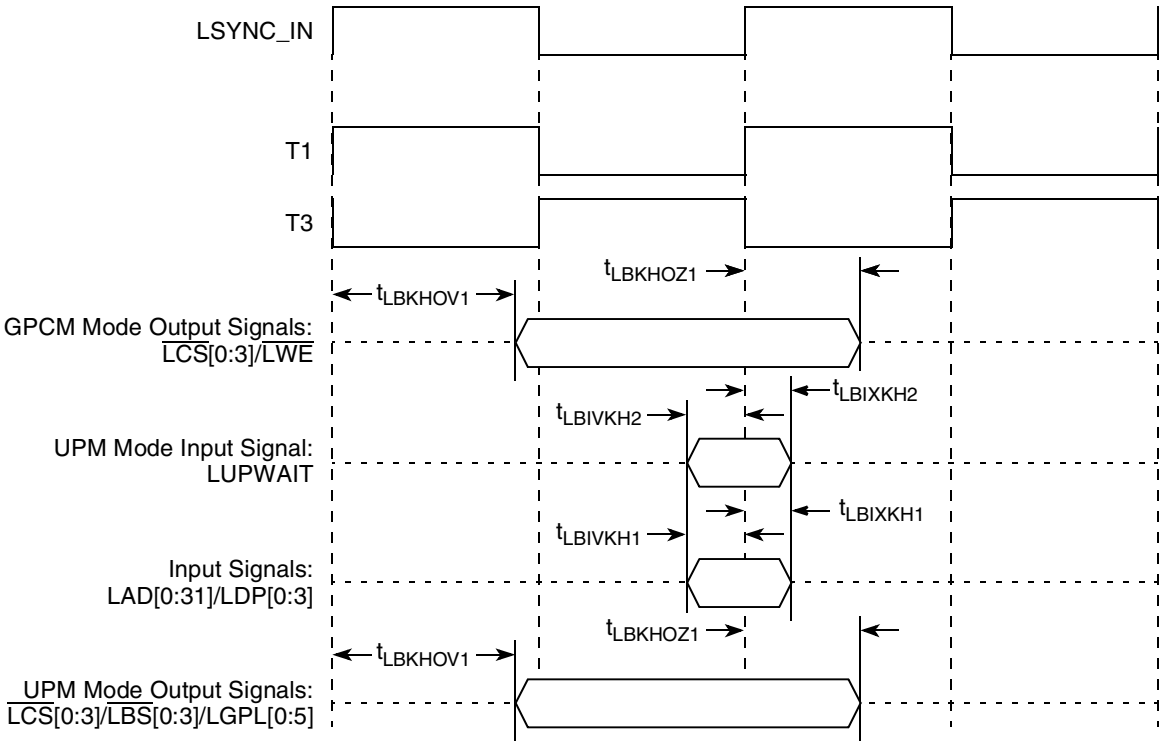

Figure 24. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (DLL Enabled)

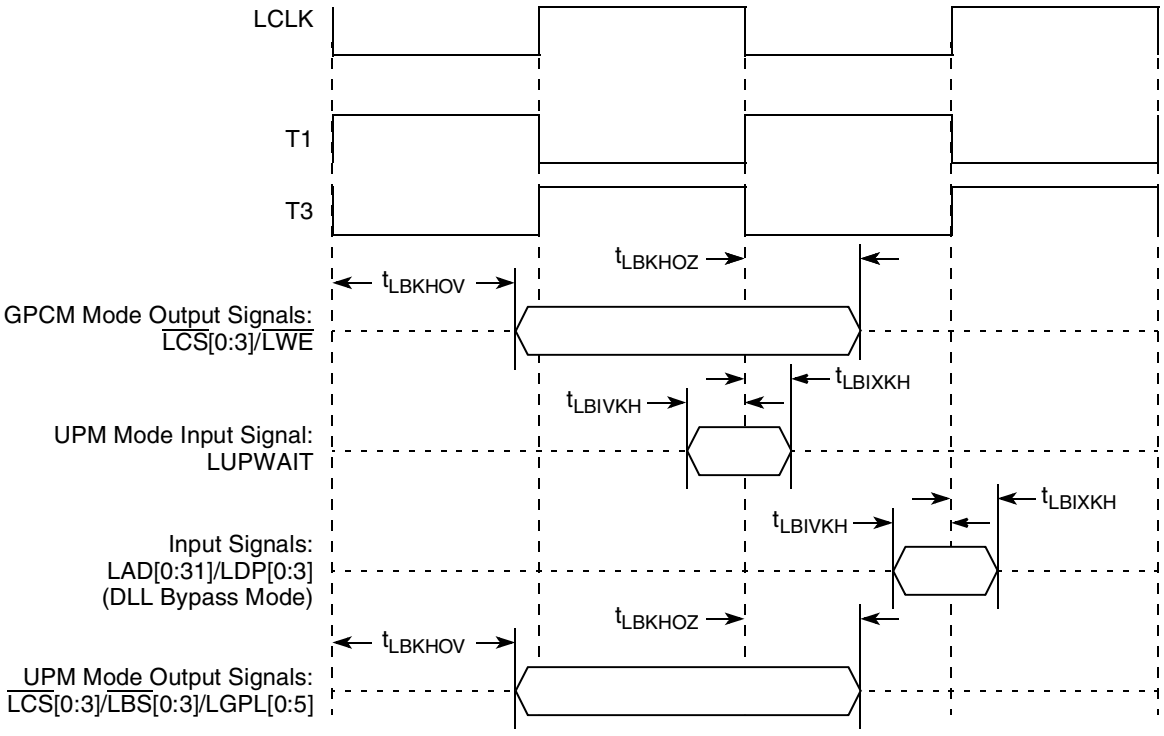

Figure 25. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (DLL Bypass Mode)

10.2 JTAG AC Electrical Characteristics

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the device.

Table 42 provides the JTAG AC timing specifications as defined in Figure 29 through Figure 32.

Table 42. JTAG AC Timing Specifications (Independent of CLKIN)[1]

At recommended operating conditions (see Table 2).

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock duty cycle	t_{JTKHKL}/t_{JTG}	45	55	%	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	—
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	 4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	 4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 11 11	ns	 5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 2 2	 — —	ns	 5
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	 5, 6 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 21). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

Table 47. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	7.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0.3	—	ns	2, 4

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Figure 35 provides the AC test load for PCI.

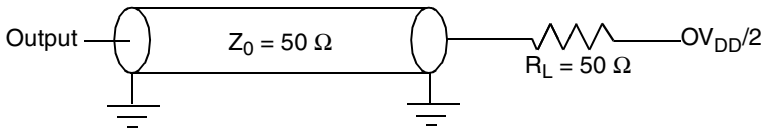

Figure 35. PCI AC Test Load

Figure 36 shows the PCI input AC timing conditions.

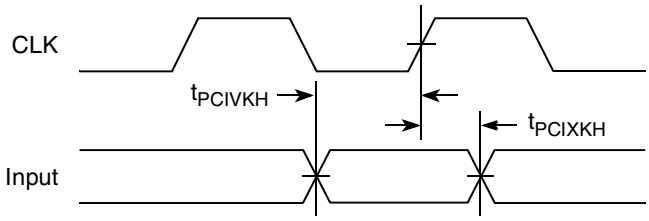

Figure 36. PCI Input AC Timing Measurement Conditions

Table 56. TDM/SI DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±10	μA

17.2 TDM/SI AC Timing Specifications

Table 57 provides the TDM/SI input and output AC timing specifications.

Table 57. TDM/SI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max[3]	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	10	ns
TDM/SI outputs—External clock high impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
3. Timings are measured from the positive or negative edge of the clock, according to SIxMR [CE] and SITXCEI[TXCEIx]. See the *MPC8360E Integrated Communications Processor Family Reference Manual* for more details.

Figure 43 provides the AC test load for the TDM/SI.

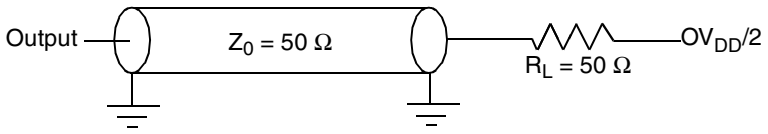

Figure 43. TDM/SI AC Test Load

Figure 44 represents the AC timing from Table 55. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

21.2 Mechanical Dimensions of the PBGA Package

Figure 52 depicts the mechanical dimensions and bottom surface nomenclature of the 668-PBGA package.

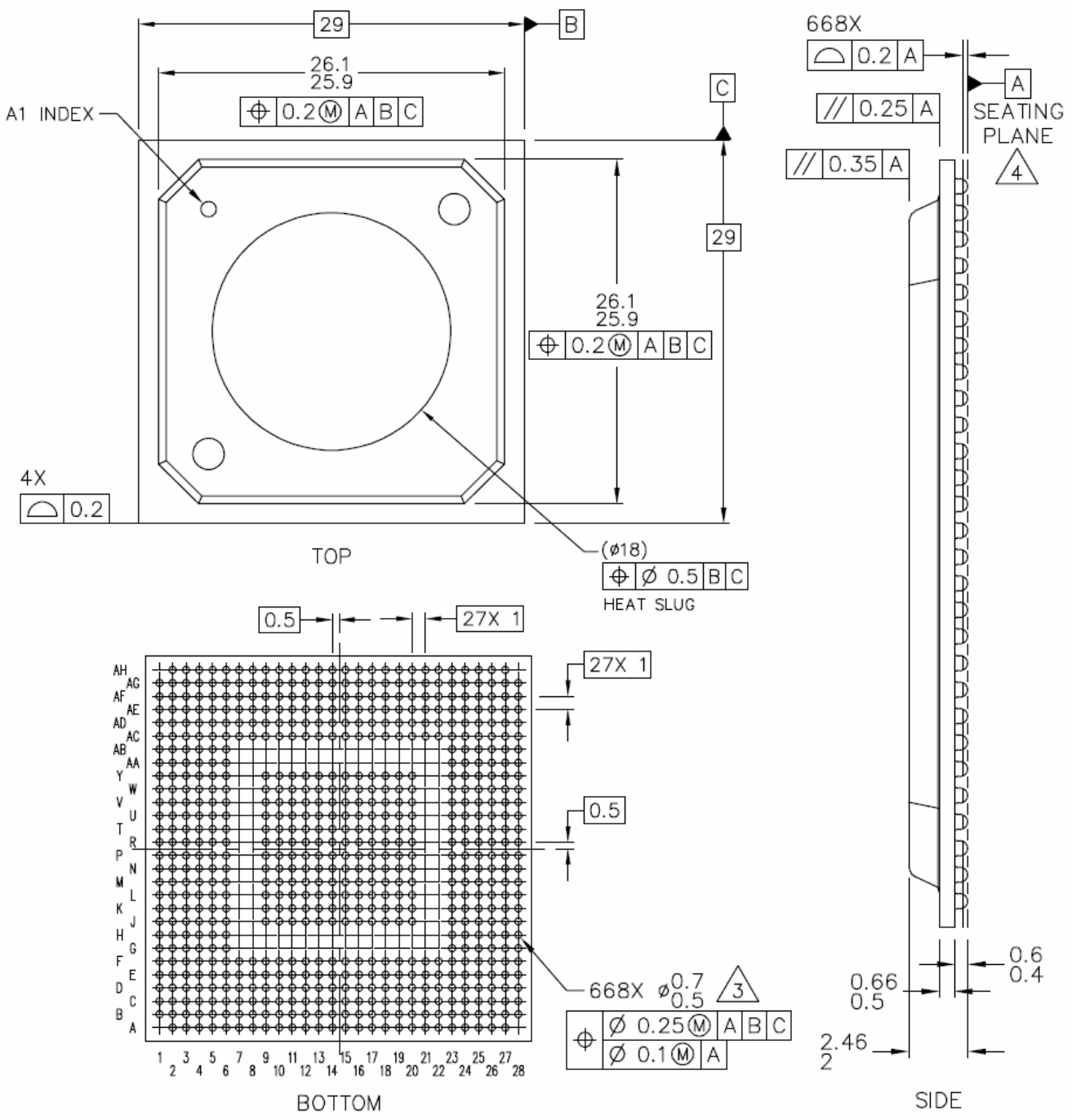

Figure 52. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package

Notes:
1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.

Table 65. MPC8358E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LGPL2/ LSDRAS/ LOE	AH19	O	OV_{DD}	—
LGPL3/ LSDCAS/ cfg_reset_source2	AE18	I/O	OV_{DD}	—
LGPL4/ LGTA/ LUPWAIT/ LPBSE	AG19	I/O	OV_{DD}	—
LGPL5/ cfg_clkin_div	AF19	I/O	OV_{DD}	—
LCKE	AD8	O	OV_{DD}	—
LCLK[0]	AC9	O	OV_{DD}	—
LCLK[1]/ LCS[6]	AG6	O	OV_{DD}	—
LCLK[2]/ LCS[7]	AE7	O	OV_{DD}	—
LSYNC_OUT	AG4	O	OV_{DD}	—
LSYNC_IN	AC8	I	OV_{DD}	—
Programmable Interrupt Controller				
MCP_OUT	AG3	O	OV_{DD}	2
IRQ0/ MCP_IN	AH4	I	OV_{DD}	—
IRQ[1:2]	AG5, AH5	I/O	OV_{DD}	—
IRQ[3]/ CORE_SRESET	AD7	I/O	OV_{DD}	—
IRQ[4:5]	AC7, AD6	I/O	OV_{DD}	—
IRQ[6:7]	AC6, AC10	I/O	OV_{DD}	—
DUART				
UART1_SOUT	AE3	O	OV_{DD}	—
UART1_SIN	AE4	I/O	OV_{DD}	—
UART1_CTS	AG2	I/O	OV_{DD}	—
UART1_RTS	AA6	O	OV_{DD}	—
I^2C Interface				
IIC1_SDA	AB6	I/O	OV_{DD}	2
IIC1_SCL	AD5	I/O	OV_{DD}	2
IIC2_SDA	AF3	I/O	OV_{DD}	2
IIC2_SCL	AH2	I/O	OV_{DD}	2
QUICC Engine				
CE_PA[0]	F6	I/O	$LV_{DD}0$	—

Table 65. MPC8358E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
CE_PA[1:2]	A22, C20	I/O	OV_{DD}	—
CE_PA[3:7]	C3, D3, C2, D2, B1	I/O	$LV_{DD}0$	—
CE_PA[8]	F18	I/O	OV_{DD}	—
CE_PA[9:12]	E3, C1, B2, D1	I/O	$LV_{DD}0$	—
CE_PA[13:14]	B21, D19	I/O	OV_{DD}	—
CE_PA[15]	E4	I/O	$LV_{DD}0$	—
CE_PA[16]	E18	I/O	OV_{DD}	—
CE_PA[17:21]	M2, N5, N3, N4, N2	I/O	$LV_{DD}1$	—
CE_PA[22]	F17	I/O	OV_{DD}	—
CE_PA[23:26]	N1, P1, P2, P4	I/O	$LV_{DD}1$	—
CE_PA[27:28]	A21, E17	I/O	OV_{DD}	—
CE_PA[29]	P5	I/O	$LV_{DD}1$	—
CE_PA[30]	B20	I/O	OV_{DD}	—
CE_PA[31]	M4	I/O	$LV_{DD}1$	—
CE_PB[0:27]	D18, C18, A20, B19, F16, E16, B18, A19, C17, D16, E15, A18, F15, B17, A17, D15, B16, A16, C15, B15, A15, E14, F14, D14, C14, B14, A14, E13	I/O	OV_{DD}	—
CE_PC[0:1]	F13, D13	I/O	OV_{DD}	—
CE_PC[2:3]	N6, M1	I/O	$LV_{DD}1$	—
CE_PC[4:6]	C13, B13, A13	I/O	OV_{DD}	—
CE_PC[7]	R1	I/O	$LV_{DD}2$	—
CE_PC[8:9]	F4, E2	I/O	$LV_{DD}0$	—
CE_PC[10:30]	D12, E12, F12, B12, A12, A11, B11, K5, K6, J1, J2, J3, H1, J4, H6, J5, M5, L1, M3, F5, B22	I/O	OV_{DD}	—
CE_PD[0:27]	H2, H3, G6, G1, H4, H5, G2, G3, F1, J6, F2, G4, E1, G5, B3, A3, D4, C4, A2, E5, B4, F8, A4, D5, C5, B5, E6, E8	I/O	OV_{DD}	—
CE_PE[0:31]	D8, A7, A5, E7, D6, F9, B6, A6, D7, C7, B7, E9, C8, E11, C11, F11, A10, B10, C10, E10, D10, A9, B9, C9, D9, F10, A8, B8, M6, K1, L3, L2	I/O	OV_{DD}	—
CE_PF[0:3]	L6, K2, L5, K4	I/O	OV_{DD}	—
Clocks				
PCI_CLK[0]/ PF[26]	R6	I/O	$LV_{DD}2$	—
PCI_CLK[1:2]/ PF[27:28]	U3, T6	I/O	OV_{DD}	—
CLKIN	AH6	I	OV_{DD}	—
PCI_SYNC_IN	AF7	I	OV_{DD}	—
PCI_SYNC_OUT/ PF[29]	AF6	I/O	OV_{DD}	3
JTAG				
TCK	AD9	I	OV_{DD}	—

input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCIOEN*n*] parameters enable the PCI_CLK_OUT*n*, respectively.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock. When the device is configured as a PCI agent device the CLKIN and the CFG_CLKIN_DIV signals should be tied to GND.

When the device is configured as a PCI host device (RCWH[PCIHOST] = 1) and PCI clock output is disabled (RCWH[PCICKDRV] = 0), clock distribution and balancing done externally on the board. Therefore, PCI_SYNC_IN is the primary input clock.

As shown in Figure 53, the primary clock input (frequency) is multiplied by the QUICC Engine block phase-locked loop (PLL), the system PLL, and the clock unit to create the QUICC Engine clock (*ce_clk*), the coherent system bus clock (*csb_clk*), the internal DDRC1 controller clock (*ddr1_clk*), and the internal clock for the local bus interface unit and DDR2 memory controller (*lb_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = \{PCI\_SYNC\_IN \times (1 + CFG\_CLKIN\_DIV)\} \times SPMF$$

In PCI host mode, PCI_SYNC_IN × (1 + CFG_CLKIN_DIV) is the CLKIN frequency; in PCI agent mode, CFG_CLKIN_DIV must be pulled down (low), so PCI_SYNC_IN × (1 + CFG_CLKIN_DIV) is the PCI_CLK frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, “Reset, Clocking, and Initialization,” in the *MPC8360E PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for more information on the clock subsystem.

The *ce_clk* frequency is determined by the QUICC Engine PLL multiplication factor (RCWL[CEPMF) and the QUICC Engine PLL division factor (RCWL[CEPDF]) according to the following equation:

$$ce\_clk = (\text{primary clock input} \times CEPMF) \div (1 + CEPDF)$$

The internal *ddr1_clk* frequency is determined by the following equation:

$$ddr1\_clk = csb\_clk \times (1 + RCWL[DDR1CM])$$

Note that the lb_clk clock frequency (for DDRC2) is determined by RCWL[LBCM]. The *internal ddr1_clk* frequency is not the external memory bus frequency; *ddr1_clk* passes through the DDRC1 clock divider (÷2) to create the differential DDRC1 memory bus clock outputs (MEMC1_MCK and $\overline{\text{MEMC1\_MCK}}$). However, the data rate is the same frequency as *ddr1_clk*.

The internal *lb_clk* frequency is determined by the following equation:

$$lb\_clk = csb\_clk \times (1 + RCWL[LBCM])$$

Table 74. Suggested PLL Configurations (continued)

Conf No.[1]	SPMF	CORE PLL	CEPMF	CEPDF	Input Clock Freq (MHz)	CSB Freq (MHz)	Core Freq (MHz)	QUICC Engine Freq (MHz)	400 (MHz)	533 (MHz)	667 (MHz)
c5	æ	æ	**10000**	**0**	33	—	—	533	—	∞	∞
c6	æ	æ	**10001**	**0**	33	—	—	566	—	—	∞
66 MHz CLKIN/PCI_SYNC_IN Options											
s1h	**0011**	**0000110**	æ	æ	66	200	400	—	∞	∞	∞
s2h	**0011**	**0000101**	æ	æ	66	200	500	—	—	∞	∞
s3h	**0011**	**0000110**	æ	æ	66	200	600	—	—	—	∞
s4h	**0100**	**0000011**	æ	æ	66	266	400	—	∞	∞	∞
s5h	**0100**	**0000100**	æ	æ	66	266	533	—	—	∞	∞
s6h	**0100**	**0000101**	æ	æ	66	266	667	—	—	—	∞
s7h	**0101**	**0000010**	æ	æ	66	333	333	—	∞	∞	∞
s8h	**0101**	**0000011**	æ	æ	66	333	500	—	—	∞	∞
s9h	**0101**	**0000100**	æ	æ	66	333	667	—	—	—	∞
c1h	æ	æ	**00101**	**0**	66	—	—	333	∞	∞	∞
c2h	æ	æ	**00110**	**0**	66	—	—	400	∞	∞	∞
c3h	æ	æ	**00111**	**0**	66	—	—	466	—	∞	∞
c4h	æ	æ	**01000**	**0**	66	—	—	533	—	∞	∞
c5h	æ	æ	**01001**	**0**	66	—	—	600	—	—	∞

[1] The Conf No. consist of prefix, an index and a postfix. The prefix “s” and “c” stands for “syset” and “ce” respectively. The postfix “h” stands for “high input clock.”The index is a serial number.

The following steps describe how to use Table 74. See Example 1.

1. Choose the up or down sections in the table according to input clock rate 33 MHz or 66 MHz.
2. Select a suitable CSB and core clock rates from Table 74. Copy the SPMF and CORE PLL configuration bits.
3. Select a suitable QUICC Engine block clock rate from Table 74. Copy the CEPMF and CEPDF configuration bits.
4. Insert the chosen SPMF, COREPLL, CEPMF and CEPDF to the RCWL fields, respectively.

Example 1. Sample Table Use

SPMF	CORE PLL	CEPMF	CEPDF	Input Clock (MHz)	CSB Freq (MHz)	Core Freq (MHz)	QUICC Engine Freq (MHz)	400 (MHz)
1000	**0000011**	**01001**	**0**	33	266	400	300	∞

- To configure the device with CSB clock rate of 266 MHz, core rate of 400 MHz, and QUICC Engine clock rate 300 MHz while the input clock rate is 33 MHz. Conf No. ‘s10’ and ‘c1’ are selected from Table 74. SPMF is 1000, CORPLL is 0000011, CEPMF is 01001, and CEPDF is 0.

23 Thermal

This section describes the thermal specifications of the MPC8358E.

23.1 Thermal Characteristics

Table 75 provides the package thermal characteristics for the 668 29 mm x 29 mm PBGA package.

Table 75. Package Thermal Characteristics for the PBGA Package

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection on single layer board (1s)	$R_{\theta JA}$	20	°C/W	1, 2
Junction-to-ambient Natural Convection on four layer board (2s2p)	$R_{\theta JA}$	14	°C/W	1, 2, 3
Junction-to-ambient (@1 m/s) on single layer board (1s)	$R_{\theta JMA}$	15	°C/W	1, 3
Junction-to-ambient (@ 1 m/s) on four layer board (2s2p)	$R_{\theta JMA}$	11	•C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	6	•C/W	4
Junction-to-case thermal	$R_{\theta JC}$	4	•C/W	5
Junction-to-Package Natural Convection on Top	Ψ_{JT}	4	•C/W	6

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 and JEDEC JESD51-9 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal. 1 m/sec is approximately equal to 200 linear feet per minute (LFM).
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

23.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers. See Table 5 for typical power dissipations values.

24.5 Output Buffer DC Impedance

The device drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 55). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

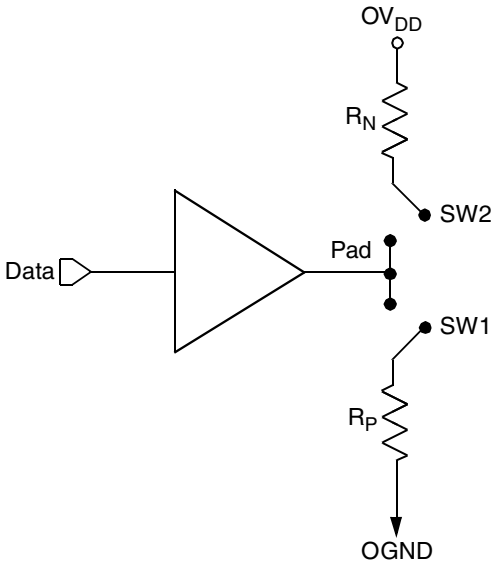

Figure 55. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 77 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 77. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	20 Target	Z_0	W
R_P	42 Target	25 Target	20 Target	Z_0	W

Table 77. Impedance Characteristics (continued)

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
Differential	NA	NA	NA	Z_{DIFF}	W

Note: Nominal supply voltages. See Table 1, T_J = 105°C.

24.6 Configuration Pin Muxing

The device provides the user with power-on configuration options that can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

24.7 Pull-Up Resistor Requirements

The device requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins including I^2C pins, Ethernet Management MDIO pin, and EPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, see *MPC8360E/MPC8358E PowerQUICC Design Checklist* (AN3097).

25 Ordering Information

25.1 Part Numbers Fully Addressed by this Document

Table 78 provides the Freescale part numbering nomenclature for the MPC8358E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also