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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2600
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, SCI, SmartCard
Peripherals	LCD, Motor control PWM, POR, PWM, WDT
Number of I/O	92
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BFQFP
Supplier Device Package	144-QFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2646rfc20jv

Item	Page	Revision (See Manual for Details)
15.2.5 Transmit Wait Register (TXPR) Bits 15 to 9 and 7 to 0	547	Table amended **Bit y, TXPRx** / **Description** 0: Transmit message idle state in corresponding mailbox (Initial value) [Clearing condition] Message transmission completion and cancellation completion 1: Transmit message transmit wait in corresponding mailbox (CAN bus arbitration) (x = 15 to 1, y = 15 to 9 and 7 to 0)
15.2.6 Transmit Wait Cancel Register (TXCR) Bits 15 to 9 and 7 to 0	548	Table amended **Bit y, TXCRx** / **Description** 0: Transmit message cancellation idle state in corresponding mailbox (Initial value) [Clearing condition] Completion of TXPR clearing (when transmit message is canceled normally) 1: TXPR cleared for corresponding mailbox (transmit message cancellation) (x = 15 to 1, y = 15 to 9 and 7 to 0)
15.2.7 Transmit Acknowledge Register (TXACK) Bits 15 to 9 and 7 to 0	549	Table amended **Bit y, TXACKx** / **Description** 0: [Clearing condition] (Initial value) Writing 1 1: Completion of message transmission for corresponding mailbox (x = 15 to 1, y = 15 to 9 and 7 to 0)
15.2.8 Abort Acknowledge Register (ABACK) Bits 15 to 9 and 7 to 0	550	Table amended **Bit y, ABACKx** / **Description** 0: [Clearing condition] (Initial value) Writing 1 1: Completion of transmit message cancellation for corresponding mailbox (x = 15 to 1, y = 15 to 9 and 7 to 0)
15.2.17 Local Acceptance Filter Masks (LAFML, LAFMH) LAFMH Bits 7 to 0 and 15 to 13	564	Table amended **Bit y, LAFMHx** / **Description** 0: Stored in RX0 (receive-only mailbox) depending on bit match between RX0 message identifier and receive message identifier (Initial value) 1: Stored in RX0 (receive-only mailbox) regardless of bit match between RX0 message identifier and receive message identifier (x = 15 to 5, y = 15 to 13 and 7 to 0)

4.2 Reset

4.2.1 Overview

A reset has the highest exception priority.

When the $\overline{\text{RES}}$ pin goes low, all current operations are stopped, and this LSI enters reset state. A reset initializes the internal state of the CPU and the registers of on-chip supporting modules. Immediately after a reset, interrupt control mode 0 is set.

When the $\overline{\text{RES}}$ pin goes from low to high, reset exception handling starts.

The H8S/2646 Group can also be reset by overflow of the watchdog timer. For details see section 12, Watchdog Timer.

4.2.2 Reset Sequence

This LSI enters reset state when the $\overline{\text{RES}}$ pin goes low.

To ensure that this LSI is reset, hold the $\overline{\text{RES}}$ pin low for at least 20 ms at power-up. To reset during operation, hold the $\overline{\text{RES}}$ pin low for at least 20 states.

When the $\overline{\text{RES}}$ pin goes high after being held low for the necessary time, this LSI starts reset exception handling as follows.

1. The internal state of the CPU and the registers of the on-chip supporting modules are initialized, the T bit is cleared to 0 in EXR, and the I bit is set to 1 in EXR and CCR.
2. The reset exception handling vector address is read and transferred to the PC, and program execution starts from the address indicated by the PC.

Figures 4.2 and 4.3 show examples of the reset sequence.

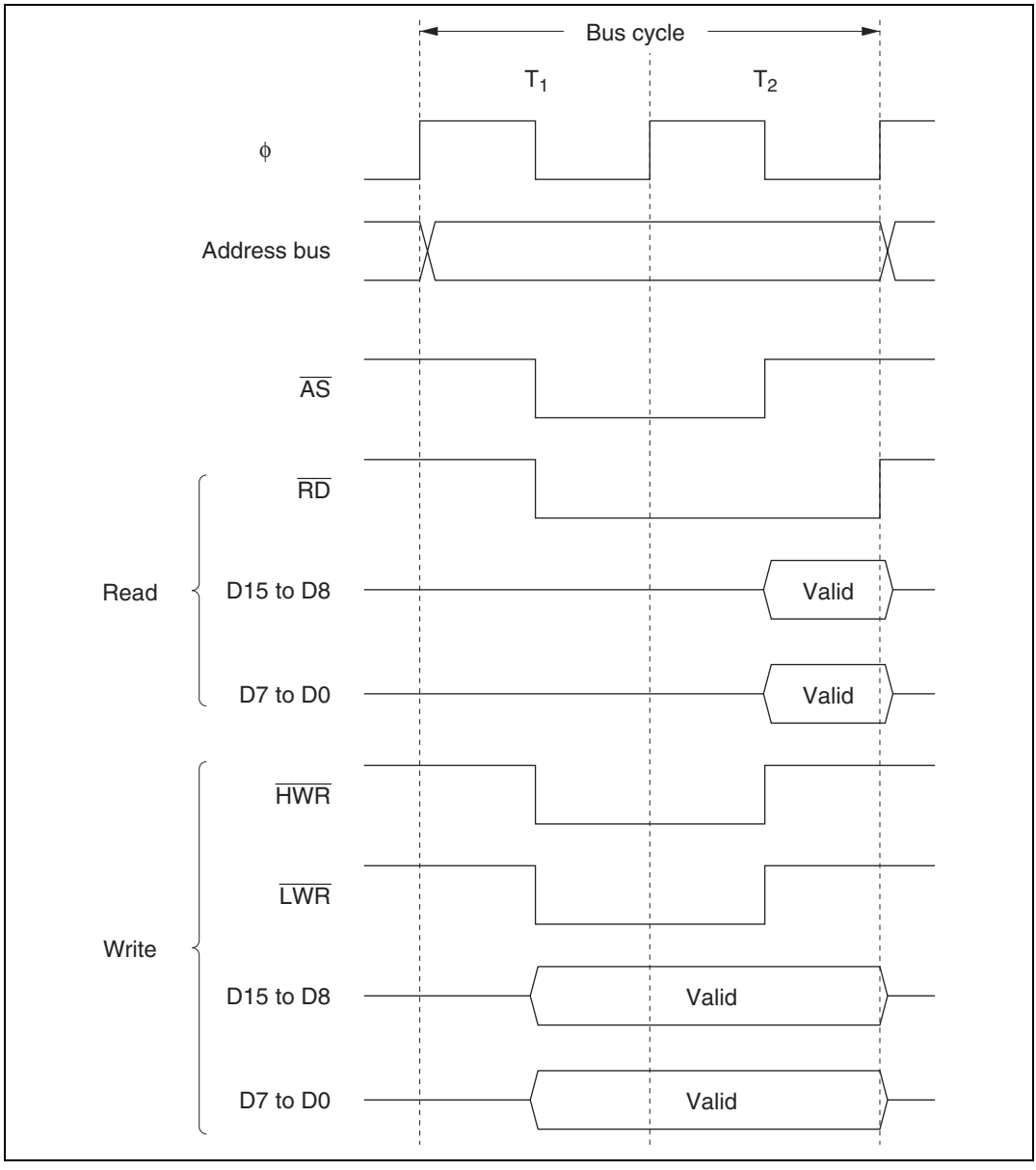

Figure 7.9 Bus Timing for 16-Bit 2-State Access Space (3) (Word Access)

Port	Description	Pins	Mode 4	Mode 5	Mode 6	Mode 7
Port 3	• 8-bit I/O port • Open-drain output capability	P37 P36 P35/SCK1/$\overline{\text{IRQ5}}$ P34/RxD1 P33/TxD1 P32/SCK0/$\overline{\text{IRQ4}}$ P31/RxD0 P30/TxD0	SCI (channels 0, 1) I/O pins (TxD0, RxD0, SCK0, TxD1, RxD1, SCK1), interrupt input pins ($\overline{\text{IRQ4}}$, $\overline{\text{IRQ5}}$), and 8-bit I/O port			
Port 4	• 8-bit input port	P47/AN7 P46/AN6 P45/AN5 P44/AN4 P43/AN3 P42/AN2 P41/AN1 P40/AN0	A/D converter analog input (AN7 to AN0) and 8-bit input port			
Port 5	• 3-bit I/O port	P52/SCK2 P51/RxD2 P50/TxD2	SCI (channel 2) I/O pins (SCK2, RxD2, TxD2) and 3-bit I/O port			
Port 9	• 8-bit input port	P97 P96 P95 P94 P93/AN11 P92/AN10 P91/AN9 P90/AN8	A/D converter analog input (AN11 to AN8) and 8-bit input port			
Port A	• 8-bit I/O port • Built-in MOS input pull-up • Open-drain output capability	PA7/A23/SEG40 PA6/A22/SEG39 PA5/A21/SEG38 PA4/A20/SEG37 PA3/A19/COM4 PA2/A18/COM3 PA1/A17/COM2 PA0/A16/COM1	LCD segment and common output (SEG37 to SEG40, COM1 to COM4), address output (A23 to A16), and 8-bit I/O port			LCD segment and common output (SEG37 to SEG40, COM1 to COM4) and 8-bit I/O port

After a reset and in hardware standby mode, PORTH contents are determined by the pin states, as PHDDR and PHDR are initialized. PORTH retains its prior state in software standby mode.

9.14.3 Pin Functions

As shown in table 9.31, the port H pin functions can be switched, bit by bit, by changing the values of OE1A to OE1H of motor control PWM timer PWOCR1 and PHDDR.

Table 9.31 Port H Pin Functions

OE1A to OE1H	1	0	
PHDDR	—	0	1
Pin function	Motor control PWM timer output	PH7 to PH0 input	PH7 to PH0 output

9.15 Port J

9.15.1 Overview

Port J is an 8-bit I/O port. Port J pins also function as motor control PWM timer output pins (PWM2A to PWM2H).

Figure 9.14 shows the port J pin configuration.

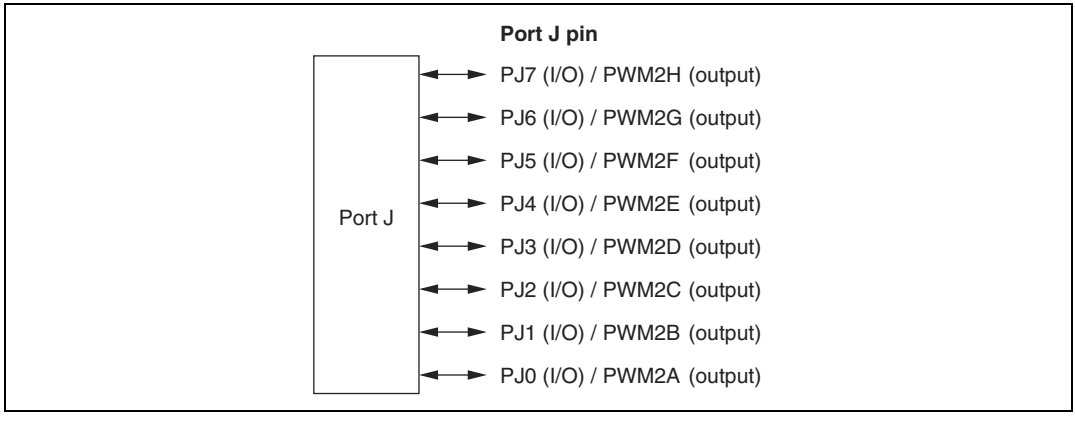

Figure 9.14 Port J Pin Functions

Channel	Bit 3 IOC3	Bit 2 IOC2	Bit 1 IOC1	Bit 0 IOC0	Description		
0	0	0	0	0	TGR0C is output compare register*1	Output disabled	(Initial value)
				1		Initial output is 0 output	0 output at compare match
			1	0			1 output at compare match
				1			Toggle output at compare match
		1	0	0		Output disabled	
				1		Initial output is 1 output	0 output at compare match
			1	0			1 output at compare match
				1			Toggle output at compare match
	1	0	0	0	TGR0C is input capture register*1	Capture input source is TIOCC0 pin	Input capture at rising edge
				1			Input capture at falling edge
			1	*			Input capture at both edges
		1	*	*		Capture input source is channel 1/count clock	Input capture at TCNT1 count-up/count-down

*: Don't care

Note: 1. When the BFA bit in TMDR0 is set to 1 and TGR0C is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Channel	Bit 3 IOC3	Bit 2 IOC2	Bit 1 IOC1	Bit 0 IOC0	Description		
3	0	0	0	0	TGR3C is output compare register*1	Output disabled	(Initial value)
				1		Initial output is 0 output	0 output at compare match
			1	0			1 output at compare match
				1			Toggle output at compare match
		1	0	0		Output disabled	
				1		Initial output is 1 output	0 output at compare match
			1	0			1 output at compare match
				1			Toggle output at compare match
	1	0	0	0	TGR3C is input capture register*1	Capture input source is TIOCC3 pin	Input capture at rising edge
				1			Input capture at falling edge
			1	*			Input capture at both edges
		1	*	*		Capture input source is channel 4/count clock	Input capture at TCNT4 count-up/count-down

*: Don't care

Note: 1. When the BFA bit in TMDR3 is set to 1 and TGR3C is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

13.3.4 Operation in Clocked Synchronous Mode

In clocked synchronous mode, data is transmitted or received in synchronization with clock pulses, making it suitable for high-speed serial communication.

Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communication by use of a common clock. Both the transmitter and the receiver also have a double-buffered structure, so that data can be read or written during transmission or reception, enabling continuous data transfer.

Figure 13.14 shows the general format for clocked synchronous serial communication.

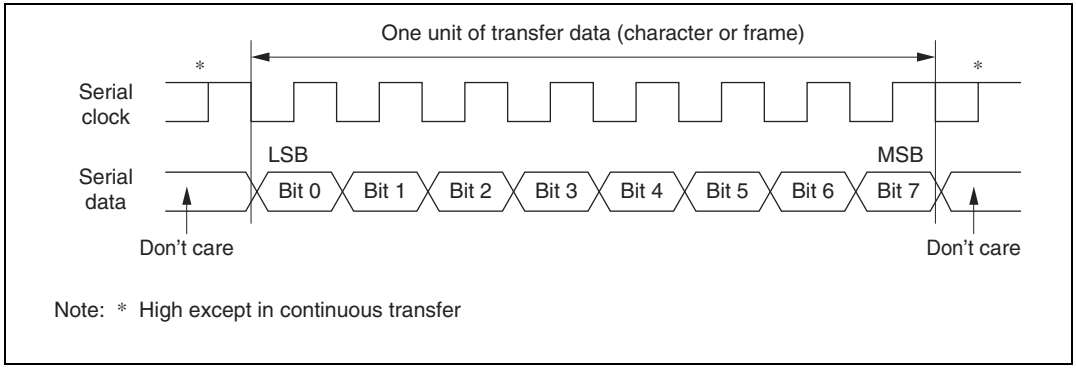

Figure 13.14 Data Format in Synchronous Communication

In clocked synchronous serial communication, data on the transmission line is output from one falling edge of the serial clock to the next. Data confirmation is guaranteed at the rising edge of the serial clock.

In clocked serial communication, one character consists of data output starting with the LSB and ending with the MSB. After the MSB is output, the transmission line holds the MSB state.

In clocked synchronous mode, the SCI receives data in synchronization with the rising edge of the serial clock.

Data Transfer Format

A fixed 8-bit data format is used.

No parity or multiprocessor bits are added.

Table 16.4 A/D Conversion Time (Single Mode)

		CKS1 = 0						CKS1 = 0					
		CKS0 = 0			CKS0 = 1			CKS0 = 0			CKS0 = 1		
Item	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
A/D conversion start delay	t_D	18	—	33	10	—	17	6	—	9	4	—	5
Input sampling time	t_{SPL}	—	127	—	—	63	—	—	31	—	—	15	—
A/D conversion time	t_{CONV}	515	—	530	259	—	266	131	—	134	67	—	68

Note: Values in the table are the number of states.

Table 16.5 A/D Conversion Time (Scan Mode)

CKS1	CKS0	Conversion Time (State)
0	0	512 (Fixed)
	1	256 (Fixed)
1	0	128 (Fixed)
	1	64 (Fixed)

16.4.4 External Trigger Input Timing

A/D conversion can be externally triggered. When the TRGS1 and TRGS0 bits are set to 11 in ADCR, external trigger input is enabled at the $\overline{\text{ADTRG}}$ pin. A falling edge at the $\overline{\text{ADTRG}}$ pin sets the ADST bit to 1 in ADCSR, starting A/D conversion. Other operations, in both single and scan modes, are the same as if the ADST bit has been set to 1 by software. Figure 16.6 shows the timing.

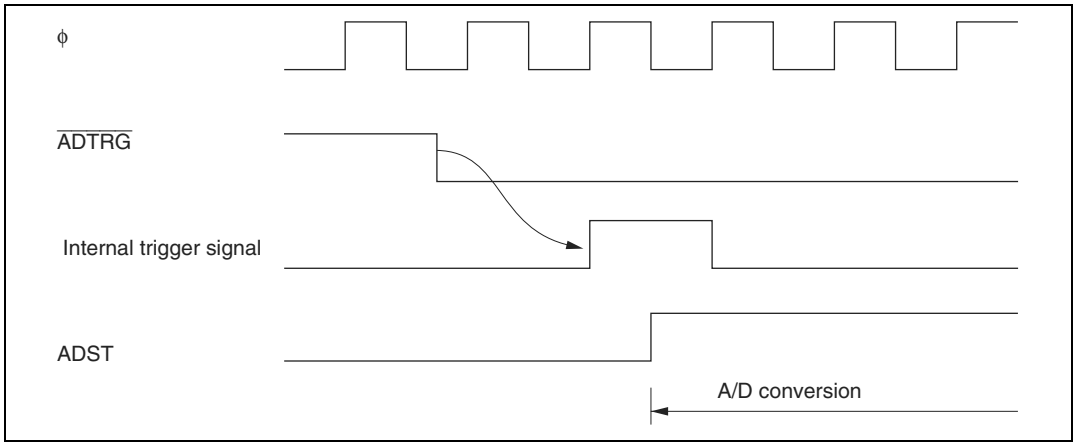

Figure 16.6 External Trigger Input Timing

16.5 Interrupts

The A/D converter generates an A/D conversion end interrupt (ADI) at the end of A/D conversion. ADI interrupt requests can be enabled or disabled by means of the ADIE bit in ADCSR.

The DTC can be activated by an ADI interrupt. Having the converted data read by the DTC in response to an ADI interrupt enables continuous conversion to be achieved without imposing a load on software.

The A/D converter interrupt source is shown in table 16.6.

Table 16.6 A/D Converter Interrupt Source

Interrupt Source	Description	DTC Activation
ADI	Interrupt due to end of conversion	Possible

A/D Conversion Precision Definitions: H8S/2646 Group A/D conversion precision definitions are given below.

- Resolution

  The number of A/D converter digital output codes

- Offset error

  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from the minimum voltage value B'0000000000 (H'00) to B'0000000001 (H'01) (see figure 16.10).

- Full-scale error

  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from B'1111111110 (H'3E) to B'1111111111 (H'3F) (see figure 16.10).

- Quantization error

  The deviation inherent in the A/D converter, given by 1/2 LSB (see figure 16.9).

- Nonlinearity error

  The error with respect to the ideal A/D conversion characteristic between the zero voltage and the full-scale voltage. Does not include the offset error, full-scale error, or quantization error.

- Absolute precision

  The deviation between the digital value and the analog input value. Includes the offset error, full-scale error, quantization error, and nonlinearity error.

17.4 Operation

17.4.1 PWM Channel 1 Operation

PWM waveforms are output from pins PWM1A to PWM1H as shown in figure 17.10.

Initial Settings: Set the PWM output polarity in PWPR1; enable the pins for PWM output with PWOCR1; select the clock to be input to PWCNT1 with bits CKS2 to CKS0 in PWCR1; set the PWM conversion cycle in PWCYR1; and set the first frame of data in PWBFR1A, PWBFR1C, PWBFR1E, and PWBFR1G.

Activation: When the CST bit in PWCR1 is set to 1, a compare match between PWCNT1 and PWCYR1 is generated. Data is transferred from PWBFR1A to PWDTR1A, from PWBFR1C to PWDTR1C, from PWBFR1E to PWDTR1E, and from PWBFR1G to PWDTR1G. PWCNT1 starts counting up. At the same time the CMF bit in PWCR1 is set, so that, if the IE bit in PWCR1 has been set, an interrupt can be requested or the DTC can be activated.

Waveform Output: The PWM outputs selected by the OTS bits in PWDTR1A, C, E, and G go high when a compare match occurs between PWCNT1 and PWCYR1. The PWM outputs not selected by the OTS bits are low. When a compare match occurs between PWCNT1 and PWDTR1A, C, E, and G, the corresponding PWM output goes low. If the corresponding bit in PWPR1 is set to 1, the output is inverted.

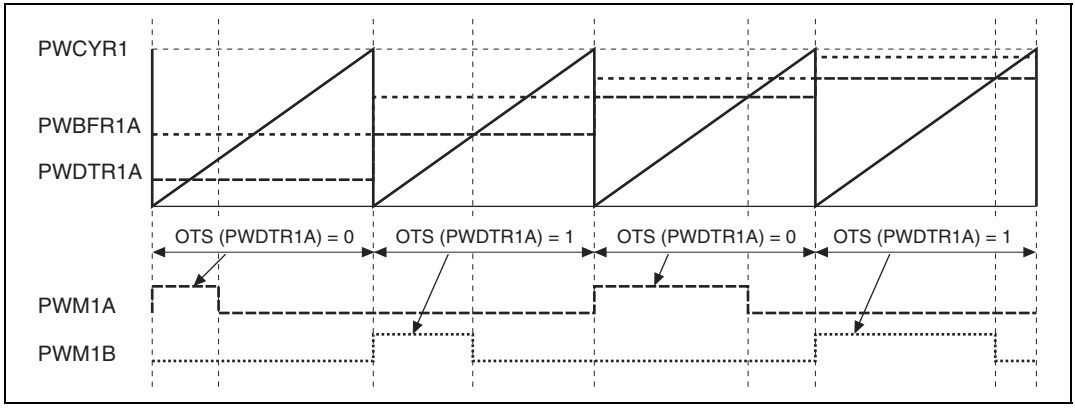

Figure 17.10 PWM Channel 1 Operation

20.8.2 Software Protection

Software protection can be implemented by setting the SWE bit in FLMCR1, erase block register 1 (EBR1), erase block register 2 (EBR2), and the RAMS bit in the RAM emulation register (RAMER). When software protection is in effect, setting the P or E bit in flash memory control register 1 (FLMCR1), does not cause a transition to program mode or erase mode. (See table 20.9.)

Table 20.9 Software Protection

Item	Description	Functions	
		Program	Erase
SWE bit protection	• Setting bit SWE in FLMCR1 to 0 will place area H'000000 to H'01FFFF in the program/erase-protected state. (Execute the program in the on-chip RAM, external memory)	Yes	Yes
Block specification protection	• Erase protection can be set for individual blocks by settings in erase block register 1 (EBR1) and erase block register 2 (EBR2). • Setting EBR1 and EBR2 to H'00 places all blocks in the erase-protected state.	—	Yes
Emulation protection	• Setting the RAMS bit to 1 in the RAM emulation register (RAMER) places all blocks in the program/erase-protected state.	Yes	Yes

22.2.2 System Clock Control Register (SCKCR)

Bit	:	7	6	5	4	3	2	1	0
		PSTOP	—	—	—	STCS	SCK2	SCK1	SCK0
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	—	—	—	R/W	R/W	R/W	R/W

SCKCR is an 8-bit readable/writable register that performs φ clock output control and medium-speed mode control.

SCKCR is initialized to H'00 by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bit 7—φ Clock Output Disable (PSTOP): In combination with the DDR of the applicable port, this bit controls φ output. See section 22.12, φ Clock Output Disable Function, for details.

	Description			
Bit 7 PSTOP	**High Speed Mode, Medium Speed Mode, Subactive Mode**	**Sleep Mode, Subsleep Mode**	**Software Standby Mode, Watch Mode, and Direct Transition**	**Hardware Standby Mode**
0	φ output (initial value)	φ output	Fixed high	High impedance
1	Fixed high	Fixed high	Fixed high	High impedance

Bits 6 to 4—Reserved: These bits are always read as 0 and cannot be modified.

Bit 3—Frequency Multiplication Factor Switching Mode Select (STCS): Selects the operation when the PLL circuit frequency multiplication factor is changed.

Bit 3 STCS	**Description**
0	Specified multiplication factor is valid after transition to software standby mode, watch mode, or subactive mode (Initial value)
1	Specified multiplication factor is valid immediately after STC bits are rewritten

Instruction	1	2	3	4	5	6	7	8	9
BTST #xx:3,@aa:8	R:W 2nd	R:B EA	R:W:M NEXT						
BTST #xx:3,@aa:16	R:W 2nd	R:W 3rd	R:B EA	R:W:M NEXT					
BTST #xx:3,@aa:32	R:W 2nd	R:W 3rd	R:W 4th	R:B EA	R:W:M NEXT				
BTST Rn,Rd	R:W NEXT								
BTST Rn,@ERd	R:W 2nd	R:B EA	R:W:M NEXT						
BTST Rn,@aa:8	R:W 2nd	R:B EA	R:W:M NEXT						
BTST Rn,@aa:16	R:W 2nd	R:W 3rd	R:B EA	R:W:M NEXT					
BTST Rn,@aa:32	R:W 2nd	R:W 3rd	R:W 4th	R:B EA	R:W:M NEXT				
BXOR #xx:3,Rd	R:W NEXT								
BXOR #xx:3,@ERd	R:W 2nd	R:B EA	R:W:M NEXT						
BXOR #xx:3,@aa:8	R:W 2nd	R:B EA	R:W:M NEXT						
BXOR #xx:3,@aa:16	R:W 2nd	R:W 3rd	R:B EA	R:W:M NEXT					
BXOR #xx:3,@aa:32	R:W 2nd	R:W 3rd	R:W 4th	R:B EA	R:W:M NEXT				
CLRMAC	R:W NEXT	Internal operation, 1 state							
CMP.B #xx:8,Rd	R:W NEXT								
CMP.B Rs,Rd	R:W NEXT								
CMP.W #xx:16,Rd	R:W 2nd	R:W NEXT							
CMP.W Rs,Rd	R:W NEXT								
CMP.L #xx:32,ERd	R:W 2nd	R:W 3rd	R:W NEXT						
CMP.L ERs,ERd	R:W NEXT								
DAA Rd	R:W NEXT								
DAS Rd	R:W NEXT								
DEC.B Rd	R:W NEXT								
DEC.W #1/2,Rd	R:W NEXT								
DEC.L #1/2,ERd	R:W NEXT								
DIVXS.B Rs,Rd	R:W 2nd	R:W NEXT	Internal operation, 11 states						
DIVXS.W Rs,ERd	R:W 2nd	R:W NEXT	Internal operation, 19 states						
DIVXU.B Rs,Rd	R:W NEXT	Internal operation, 11 states							
DIVXU.W Rs,ERd	R:W NEXT	Internal operation, 19 states							
EEPMOV.B	R:W 2nd	R:B EAs*1	R:B EAd*1	R:B EAs*2	W:B EAd*2	R:W NEXT			
EEPMOV.W	R:W 2nd	R:B EAs*1	R:B EAd*1	R:B EAs*2	W:B EAd*2	R:W NEXT			
EXTS.W Rd	R:W NEXT			← Repeated n times*2 →					
EXTS.L ERd	R:W NEXT								
EXTU.W Rd	R:W NEXT								
EXTU.L ERd	R:W NEXT								
INC.B Rd	R:W NEXT								

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'F8E8	MD7[1]	MSG_DATA_1 (8 bits)								HCAN	8/16
H'F8E9	MD7[2]	MSG_DATA_2 (8 bits)									
H'F8EA	MD7[3]	MSG_DATA_3 (8 bits)									
H'F8EB	MD7[4]	MSG_DATA_4 (8 bits)									
H'F8EC	MD7[5]	MSG_DATA_5 (8 bits)									
H'F8ED	MD7[6]	MSG_DATA_6 (8 bits)									
H'F8EE	MD7[7]	MSG_DATA_7 (8 bits)									
H'F8EF	MD7[8]	MSG_DATA_8 (8 bits)									
H'F8F0	MD8[1]	MSG_DATA_1 (8 bits)									
H'F8F1	MD8[2]	MSG_DATA_2 (8 bits)									
H'F8F2	MD8[3]	MSG_DATA_3 (8 bits)									
H'F8F3	MD8[4]	MSG_DATA_4 (8 bits)									
H'F8F4	MD8[5]	MSG_DATA_5 (8 bits)									
H'F8F5	MD8[6]	MSG_DATA_6 (8 bits)									
H'F8F6	MD8[7]	MSG_DATA_7 (8 bits)									
H'F8F7	MD8[8]	MSG_DATA_8 (8 bits)									
H'F8F8	MD9[1]	MSG_DATA_1 (8 bits)									
H'F8F9	MD9[2]	MSG_DATA_2 (8 bits)									
H'F8FA	MD9[3]	MSG_DATA_3 (8 bits)									
H'F8FB	MD9[4]	MSG_DATA_4 (8 bits)									
H'F8FC	MD9[5]	MSG_DATA_5 (8 bits)									
H'F8FD	MD9[6]	MSG_DATA_6 (8 bits)									
H'F8FE	MD9[7]	MSG_DATA_7 (8 bits)									
H'F8FF	MD9[8]	MSG_DATA_8 (8 bits)									
H'F900	MD10[1]	MSG_DATA_1 (8 bits)									
H'F901	MD10[2]	MSG_DATA_2 (8 bits)									
H'F902	MD10[3]	MSG_DATA_3 (8 bits)									
H'F903	MD10[4]	MSG_DATA_4 (8 bits)									
H'F904	MD10[5]	MSG_DATA_5 (8 bits)									
H'F905	MD10[6]	MSG_DATA_6 (8 bits)									
H'F906	MD10[7]	MSG_DATA_7 (8 bits)									
H'F907	MD10[8]	MSG_DATA_8 (8 bits)									
H'F908	MD11[1]	MSG_DATA_1 (8 bits)									
H'F909	MD11[2]	MSG_DATA_2 (8 bits)									
H'F90A	MD11[3]	MSG_DATA_3 (8 bits)									
H'F90B	MD11[4]	MSG_DATA_4 (8 bits)									
H'F90C	MD11[5]	MSG_DATA_5 (8 bits)									
H'F90D	MD11[6]	MSG_DATA_6 (8 bits)									
H'F90E	MD11[7]	MSG_DATA_7 (8 bits)									
H'F90F	MD11[8]	MSG_DATA_8 (8 bits)									

MBCR—Mailbox Configuration Register H'F804 HCAN

Bit	15	14	13	12	11	10	9	8
	MBCR7	MBCR6	MBCR5	MBCR4	MBCR3	MBCR2	MBCR1	—
Initial value	0	0	0	0	0	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—

Bit	7	6	5	4	3	2	1	0
	MBCR15	MBCR14	MBCR13	MBCR12	MBCR11	MBCR10	MBCR9	MBCR8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Mailbox Setting Register

0	Corresponding mailbox is set for transmission
1	Corresponding mailbox is set for reception

TXPR—Transmit Wait Register H'F806 HCAN

Bit	15	14	13	12	11	10	9	8
	TXPR7	TXPR6	TXPR5	TXPR4	TXPR3	TXPR2	TXPR1	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—

Bit	7	6	5	4	3	2	1	0
	TXPR15	TXPR14	TXPR13	TXPR12	TXPR11	TXPR10	TXPR9	TXPR8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Transmit Wait Register

0	Transmit message idle state in corresponding mailbox [Clearing condition] Message transmission completion and cancellation completion
1	Transmit message transmit wait in corresponding mailbox (CAN bus arbitration)

MC121—Message Control 121	**H'F880**	**HCAN**
MC122—Message Control 122	**H'F881**	**HCAN**
MC123—Message Control 123	**H'F882**	**HCAN**
MC124—Message Control 124	**H'F883**	**HCAN**
MC125—Message Control 125	**H'F884**	**HCAN**
MC126—Message Control 126	**H'F885**	**HCAN**
MC127—Message Control 127	**H'F886**	**HCAN**
MC128—Message Control 128	**H'F887**	**HCAN**

MC121

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	DLC3	DLC2	DLC1	DLC0
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	—	—	—	—	—	—	—	—

Data Length Code

0	0	0	0	Data length = 0 byte
			1	Data length = 1 byte
		1	0	Data length = 2 bytes
			1	Data length = 3 bytes
	1	0	0	Data length = 4 bytes
			1	Data length = 5 bytes
		1	0	Data length = 6 bytes
			1	Data length = 7 bytes
1	0	0	0	Data length = 8 bytes
Other than the above				Setting prohibited

MC122

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MC123

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

NDRL—Next Data Register L H'FE2D, H'FE2F PPG

Same Trigger for Pulse Output Groups

Address H'FE2D

Bit	7	6	5	4	3	2	1	0
	NDR7	NDR6	NDR5	NDR4	NDR3	NDR2	NDR1	NDR0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address H'FE2F

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	1	1	1	1	1	1	1	1
Read/Write	—	—	—	—	—	—	—	—

Different Triggers for Pulse Output Groups

Address H'FE2D

Bit	7	6	5	4	3	2	1	0
	NDR7	NDR6	NDR5	NDR4	—	—	—	—
Initial value	0	0	0	0	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	—	—	—	—

Address H'FE2F

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	NDR3	NDR2	NDR1	NDR0
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Note: For details, see section 11.2.4, Notes on NDR Access.

Port Name Pin Name	MCU Operating Mode		Reset	Hardware Standby Mode	Software Standby Mode	Program Execution State Sleep Mode
Port C	4, 5		L	T	[OPE = 0] T [OPE = 1] kept	A7 to A0
	6		T	T	[Segment output] port [DDR = 1, OPE = 0] T [DDR = 1, OPE = 1] kept [DDR = 0] kept	[Segment output] SEG8 to SEG1 [DDR = 1] A7 to A0 [DDR = 0] Input port
	7		T	T	[Segment output] port [Otherwise] kept	[Segment output] SEG8 to SEG1 [Otherwise] I/O port
Port D	4 to 6		T	T	T	Data bus
	7		T	T	kept	I/O port
Port E	4 to 6	8 bit bus	T	T	kept	I/O port
		16 bit bus	T	T	T	Data bus
	7		T	T	kept	I/O port
PF7/ϕ	4 to 6		Clock output	T	[DDR = 0] T [DDR = 1] H	[DDR = 0] T [DDR = 1] Clock output
	7		T	T	[DDR = 0] T [DDR = 1] H	[DDR = 0] T [DDR = 1] Clock output
PF6/$\overline{AS}$	4 to 6		H	T	[OPE = 0] T [OPE = 1] H	$\overline{AS}$
	7		T	T	[Segment output] port [Otherwise] kept	[Segment output] SEG20 [Otherwise] I/O port