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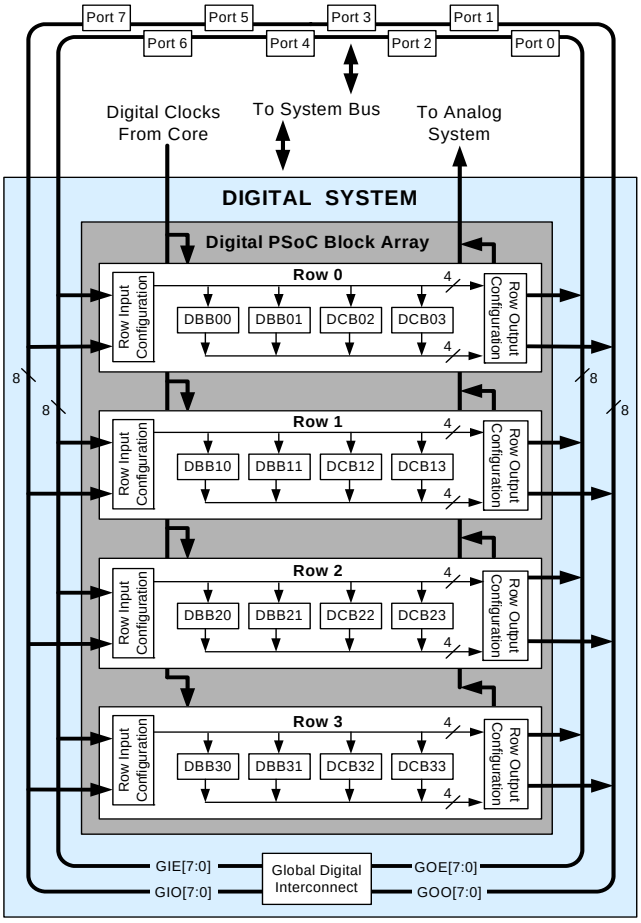
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	HB LED Controller
Core Processor	M8C
Program Memory Type	FLASH (32KB)
Controller Series	CY8CLED
RAM Size	2K x 8
Interface	I²C, SPI, UART/USART
Number of I/O	44
Voltage - Supply	3V ~ 5.25V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	48-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8cled16-48pvxi

Figure 1. Digital System Block Diagram



The Analog System

The Analog System is composed of 12 configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common EZ-Color analog functions (most available as user modules) are listed below.

- Analog-to-digital converters (up to 4, with 6- to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (2, 4, 6, or 8 pole band-pass, low-pass, and notch)
- Amplifiers (up to 4, with selectable gain to 48x)
- Instrumentation amplifiers (up to 2, with selectable gain to 93x)
- Comparators (up to 4, with 16 selectable thresholds)
- DACs (up to 4, with 6- to 9-bit resolution)
- Multiplying DACs (up to 4, with 6- to 9-bit resolution)
- High current output drivers (four with 40 mA drive as a core resource)
- 1.3 V reference (as a System resource)
- DTMF Dialer
- Modulators
- Correlators
- Peak Detectors
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks, as shown in the figure below.

Figure 2. Analog System Block Diagram

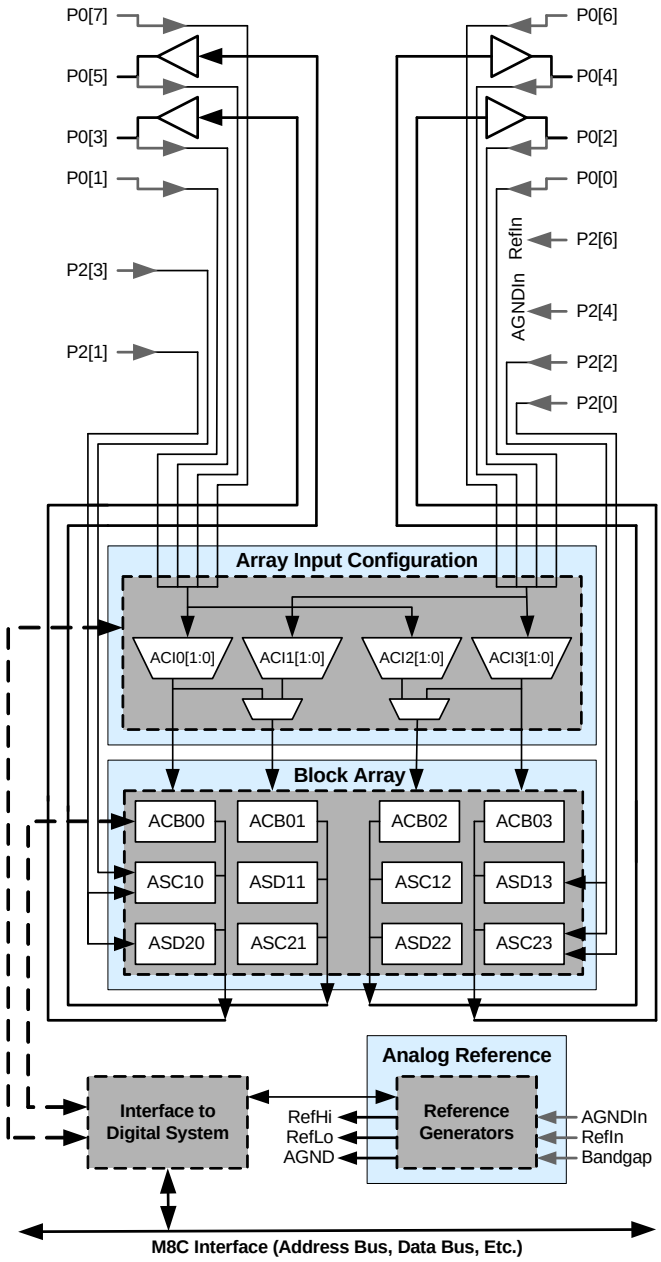


Table 3. 48-Pin Part Pinout (QFN)[2]

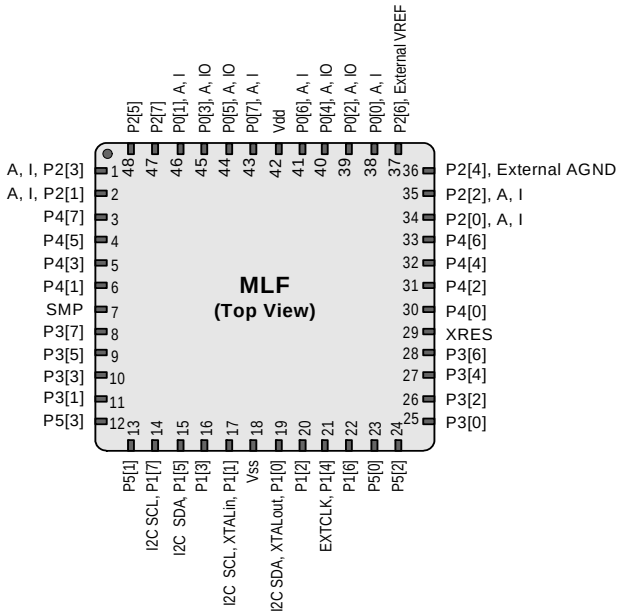
Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P2[3]	Direct switched capacitor block input.
2	I/O	I	P2[1]	Direct switched capacitor block input.
3	I/O		P4[7]	
4	I/O		P4[5]	
5	I/O		P4[3]	
6	I/O		P4[1]	
7	Power		SMP	Switch mode pump (SMP) connection to external components required.
8	I/O		P3[7]	
9	I/O		P3[5]	
10	I/O		P3[3]	
11	I/O		P3[1]	
12	I/O		P5[3]	
13	I/O		P5[1]	
14	I/O		P1[7]	I^2C serial clock (SCL).
15	I/O		P1[5]	I^2C serial data (SDA).
16	I/O		P1[3]	
17	I/O		P1[1]	Crystal (XTALin), I^2C serial clock (SCL), ISSP-SCLK[1].
18	Power		Vss	Ground connection.
19	I/O		P1[0]	Crystal (XTALout), I^2C serial data (SDA), ISSP-SDATA[1].
20	I/O		P1[2]	
21	I/O		P1[4]	optional external clock input (EXTCLK).
22	I/O		P1[6]	
23	I/O		P5[0]	
24	I/O		P5[2]	
25	I/O		P3[0]	
26	I/O		P3[2]	
27	I/O		P3[4]	
28	I/O		P3[6]	
29	Input		XRES	Active high external reset with internal pull-down.
30	I/O		P4[0]	
31	I/O		P4[2]	
32	I/O		P4[4]	
33	I/O		P4[6]	
34	I/O	I	P2[0]	Direct switched capacitor block input.
35	I/O	I	P2[2]	Direct switched capacitor block input.
36	I/O		P2[4]	external analog ground (AGND).
37	I/O		P2[6]	external voltage reference (VREF).
38	I/O	I	P0[0]	Analog column mux input.
39	I/O	I/O	P0[2]	Analog column mux input and column output.
40	I/O	I/O	P0[4]	Analog column mux input and column output.
41	I/O	I	P0[6]	Analog column mux input.
42	Power		V_{DD}	Supply voltage.
43	I/O	I	P0[7]	Analog column mux input.
44	I/O	I/O	P0[5]	Analog column mux input and column output.
45	I/O	I/O	P0[3]	Analog column mux input and column output.
46	I/O	I	P0[1]	Analog column mux input.
47	I/O		P2[7]	
48	I/O		P2[5]	

LEGEND: A = Analog, I = Input, and O = Output.

Note

2. The center pad on the QFN package should be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

Figure 4. 48-Pin Device



Register Reference

Register Conventions

Abbreviations Used

The register conventions specific to this section are listed in the following table.

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

This chapter lists the registers of the CY8CLED16 EZ-Color device.

The device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, Bank 0 and bank 1. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are reserved and should not be accessed.

Table 4. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Acces	Name	Addr (0,Hex)	Acces
PRT0DR	00	RW	DBB20DR0	40	#	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0IE	01	RW	DBB20DR1	41	W	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0GS	02	RW	DBB20DR2	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0DM2	03	RW	DBB20CR0	43	#	ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DR	04	RW	DBB21DR0	44	#	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1IE	05	RW	DBB21DR1	45	W	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1GS	06	RW	DBB21DR2	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1DM2	07	RW	DBB21CR0	47	#	ASD11CR3	87	RW		C7	
PRT2DR	08	RW	DCB22DR0	48	#	ASC12CR0	88	RW	RDI3RI	C8	RW
PRT2IE	09	RW	DCB22DR1	49	W	ASC12CR1	89	RW	RDI3SYN	C9	RW
PRT2GS	0A	RW	DCB22DR2	4A	RW	ASC12CR2	8A	RW	RDI3IS	CA	RW
PRT2DM2	0B	RW	DCB22CR0	4B	#	ASC12CR3	8B	RW	RDI3LT0	CB	RW
PRT3DR	0C	RW	DCB23DR0	4C	#	ASD13CR0	8C	RW	RDI3LT1	CC	RW
PRT3IE	0D	RW	DCB23DR1	4D	W	ASD13CR1	8D	RW	RDI3RO0	CD	RW
PRT3GS	0E	RW	DCB23DR2	4E	RW	ASD13CR2	8E	RW	RDI3RO1	CE	RW
PRT3DM2	0F	RW	DCB23CR0	4F	#	ASD13CR3	8F	RW		CF	
PRT4DR	10	RW	DBB30DR0	50	#	ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW	DBB30DR1	51	W	ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW	DBB30DR2	52	RW	ASD20CR2	92	RW		D2	
PRT4DM2	13	RW	DBB30CR0	53	#	ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW	DBB31DR0	54	#	ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW	DBB31DR1	55	W	ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW	DBB31DR2	56	RW	ASC21CR2	96	RW	I2C_CFG	D6	RW
PRT5DM2	17	RW	DBB31CR0	57	#	ASC21CR3	97	RW	I2C_SCR	D7	#
PRT6DR	18	RW	DCB32DR0	58	#	ASD22CR0	98	RW	I2C_DR	D8	RW
PRT6IE	19	RW	DCB32DR1	59	W	ASD22CR1	99	RW	I2C_MSCR	D9	#
PRT6GS	1A	RW	DCB32DR2	5A	RW	ASD22CR2	9A	RW	INT_CLR0	DA	RW
PRT6DM2	1B	RW	DCB32CR0	5B	#	ASD22CR3	9B	RW	INT_CLR1	DB	RW
PRT7DR	1C	RW	DCB33DR0	5C	#	ASC23CR0	9C	RW	INT_CLR2	DC	RW
PRT7IE	1D	RW	DCB33DR1	5D	W	ASC23CR1	9D	RW	INT_CLR3	DD	RW
PRT7GS	1E	RW	DCB33DR2	5E	RW	ASC23CR2	9E	RW	INT_MSK3	DE	RW
PRT7DM2	1F	RW	DCB33CR0	5F	#	ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCB02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCB02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCB02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBB10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBB10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBB11CR0	37	#	ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12DR0	38	#	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12DR1	39	W	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12DR2	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
DCB12CR0	3B	#	ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13DR0	3C	#	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13DR1	3D	W	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13DR2	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCB13CR0	3F	#	ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are reserved and should not be accessed. # Access is bit specific.

Table 5. Register Map Bank 1 Table: Configuration Space

Name	Addr(1,Hex)	Access	Name	Addr(1,Hex)	Access	Name	Addr(1,Hex)	Access	Name	Addr(1,Hex)	Access
PRT0DM0	00	RW	DBB20FN	40	RW	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0DM1	01	RW	DBB20IN	41	RW	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBB20OU	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW		43		ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DM0	04	RW	DBB21FN	44	RW	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1DM1	05	RW	DBB21IN	45	RW	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1IC0	06	RW	DBB21OU	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW	DCB22FN	48	RW	ASC12CR0	88	RW	RDI3RI	C8	RW
PRT2DM1	09	RW	DCB22IN	49	RW	ASC12CR1	89	RW	RDI3SYN	C9	RW
PRT2IC0	0A	RW	DCB22OU	4A	RW	ASC12CR2	8A	RW	RDI3IS	CA	RW
PRT2IC1	0B	RW		4B		ASC12CR3	8B	RW	RDI3LT0	CB	RW
PRT3DM0	0C	RW	DCB23FN	4C	RW	ASD13CR0	8C	RW	RDI3LT1	CC	RW
PRT3DM1	0D	RW	DCB23IN	4D	RW	ASD13CR1	8D	RW	RDI3RO0	CD	RW
PRT3IC0	0E	RW	DCB23OU	4E	RW	ASD13CR2	8E	RW	RDI3RO1	CE	RW
PRT3IC1	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DM0	10	RW	DBB30FN	50	RW	ASD20CR0	90	RW	GDI_O_IN	D0	RW
PRT4DM1	11	RW	DBB30IN	51	RW	ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW	DBB30OU	52	RW	ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW	DBB31FN	54	RW	ASC21CR0	94	RW		D4	
PRT5DM1	15	RW	DBB31IN	55	RW	ASC21CR1	95	RW		D5	
PRT5IC0	16	RW	DBB31OU	56	RW	ASC21CR2	96	RW		D6	
PRT5IC1	17	RW		57		ASC21CR3	97	RW		D7	
PRT6DM0	18	RW	DCB32FN	58	RW	ASD22CR0	98	RW		D8	
PRT6DM1	19	RW	DCB32IN	59	RW	ASD22CR1	99	RW		D9	
PRT6IC0	1A	RW	DCB32OU	5A	RW	ASD22CR2	9A	RW		DA	
PRT6IC1	1B	RW		5B		ASD22CR3	9B	RW		DB	
PRT7DM0	1C	RW	DCB33FN	5C	RW	ASC23CR0	9C	RW		DC	
PRT7DM1	1D	RW	DCB33IN	5D	RW	ASC23CR1	9D	RW	OSC_GO_EN	DD	RW
PRT7IC0	1E	RW	DCB33OU	5E	RW	ASC23CR2	9E	RW	OSC_CR4	DE	RW
PRT7IC1	1F	RW		5F		ASC23CR3	9F	RW	OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7		DEC_CR2	E7	RW
DCB02FN	28	RW	ALT_CR1	68	RW		A8		IMO_TR	E8	W
DCB02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
DBB10FN	30	RW	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10IN	31	RW	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10OU	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11FN	34	RW	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11IN	35	RW	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11OU	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12FN	38	RW	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12IN	39	RW	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12OU	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
	3B		ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13FN	3C	RW	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13IN	3D	RW	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13OU	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
	3F		ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

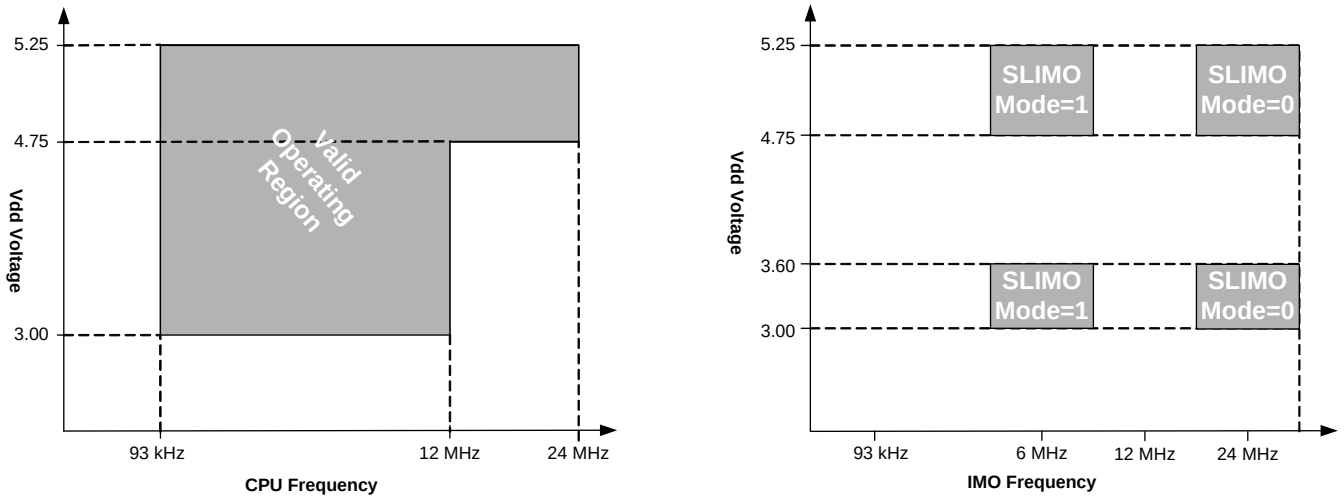
Blank fields are reserved and should not be accessed. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CLED16 EZ-Color device. For the most up-to-date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Refer to Table 20 for the electrical specifications for the internal main oscillator (IMO) using SLIMO mode.

Figure 5. Voltage versus CPU Frequency, and IMO Frequency Trim Options



Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	25	+100	°C	Higher storage temperatures reduces data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 65 °C degrade reliability.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	
$T_{BAKETIME}$	Bake time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied	–40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC input voltage	Vss - 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC Voltage applied to Tri-state	Vss - 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
I_{MAIO}	Maximum current into any port pin configured as analog driver	–50	–	+50	mA	
ESD	Electro static discharge voltage	2000	–	–	V	Human body model ESD.
LU	Latch up current	–	–	200	mA	

Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	–0	–	+85	°C	
T_J	Junction temperature	–0	–	+100	°C	The temperature rise from ambient to junction is package specific. See Thermal Impedances per Package on page 42. The user must limit the power consumption to comply with this requirement.

DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and -40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The operational amplifier is a component of both the Analog Continuous Time PSoC blocks and the analog switched capacitor PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 8. 5-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = Low, Opamp bias = Low Power = Low, Opamp bias = High Power = Medium, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = Low Power = High, Opamp bias = High	 – – – – – –	 1.6 1.6 1.6 1.6 1.6 1.6	 10 10 10 10 10 10	 mV mV mV mV mV mV	–
TCV_{OSOA}	Average input offset voltage drift	–	4	23	µV/°C	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	200	–	pA	Gross tested to 1 µA
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range (All cases, except Power = High, Opamp bias = High) Common mode voltage range (Power = High, Opamp bias = High)	0 0.5	– –	V_{DD} V_{DD} – 0.5	V V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
CMRROA	Common mode rejection ratio	60	–	–	dB	–
GOLOA	Open loop gain	80	–	–	dB	–
$V_{OHIGHOA}$	High output voltage swing (internal signals)	V_{DD} – 0.01	–	–	V	–
V_{OLOWOA}	Low output voltage swing (internal signals)	–	–	0.1	V	–
I_{SOA}	Supply current (including associated AGND buffer) Power = Low, Opamp bias = Low Power = Low, Opamp bias = High Power = Medium, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = Low Power = High, Opamp bias = High	 – – – – – –	 150 300 600 1200 2400 4600	 200 400 800 1600 3200 6400	 µA µA µA µA µA µA	–
$PSRR_{OA}$	Supply voltage rejection ratio	67	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$.

Table 12. 3.3-V DC Analog Output Buffer Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Notes
I_{SOB}	Supply current including bias cell (no load) Power = Low Power = High	 – –	 0.8 2.0	 1 5	 mA mA	–
$PSRR_{OB}$	Supply voltage rejection ratio	60	64	–	dB	
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit driven by the analog output buffer.

DC Switch Mode Pump Specifications

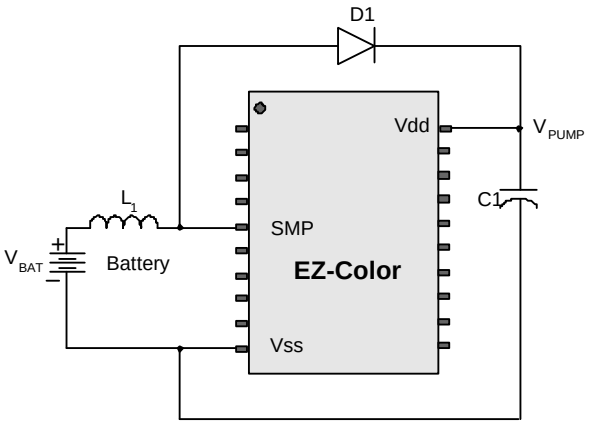
The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 13. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PUMP} 5V	5 V output voltage at V_{DD} from Pump	4.75	5.0	5.25	V	Configured as in Note 3. Average, neglecting ripple. SMP trip voltage is set to 5.0 V.
V_{PUMP} 3V	3 V output voltage at V_{DD} from Pump	3.00	3.25	3.60	V	Configured as in Note 3. Average, neglecting ripple. SMP trip voltage is set to 3.25 V.
I_{PUMP}	Available output current V_{BAT} = 1.5 V, V_{PUMP} = 3.25 V V_{BAT} = 1.8 V, V_{PUMP} = 5.0 V	 8 5	 – –	 – –	 mA mA	Configured as in Note 3. SMP trip voltage is set to 3.25 V. SMP trip voltage is set to 5.0 V.
V_{BAT}5V	Input voltage range from battery	1.8	–	5.0	V	Configured as in Note 3. SMP trip voltage is set to 5.0 V.
V_{BAT}3V	Input voltage range from battery	1.0	3–	3.3	V	Configured as in Note 3. SMP trip voltage is set to 3.25 V.
$V_{BATSTART}$	Minimum input voltage from battery to start Pump	1.2	–	–	V	Configured as in Note 3. 0 °C ≤ T_A ≤ 100. 1.25 V at T_A = -40 °C.
ΔV_{PUMP_Line}	Line regulation (over V_{BAT} range)	–	5	–	$\%V_O$	Configured as in Note 3. V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in Table 17, "DC POR, SMP, and LVD Specifications," on page 28.
ΔV_{PUMP_Load}	Load regulation	–	5	–	$\%V_O$	Configured as in Note 3. V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in Table 17, "DC POR, SMP, and LVD Specifications," on page 28.
ΔV_{PUMP_Ripple}	Output Voltage Ripple (depends on capacitor/load)	–	100	–	mVpp	Configured as in Note 3. Load is 5 mA.
E_3	Efficiency	35	50	–	%	Configured as in Note 3. Load is 5 mA. SMP trip voltage is set to 3.25 V.
F_{PUMP}	Switching Frequency	–	1.4	–	MHz	–
DC_{PUMP}	Switching Duty Cycle	–	50	–	%	–

Note
3. L_1 = 2 mH inductor, C_1 = 10 mF capacitor, D_1 = Schottky diode. See Figure 6.

Figure 6. Basic Switch Mode Pump Circuit



DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The guaranteed specifications are measured through the analog continuous time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the analog reference control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Table 14. 5-V DC Analog Reference Specifications

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b000	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.228	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.352	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.078	$V_{DD}/2$ – 0.007	$V_{DD}/2$ + 0.063	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.336	$V_{DD}/2$ – 1.295	$V_{DD}/2$ – 1.250	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.224	$V_{DD}/2$ + 1.293	$V_{DD}/2$ + 1.356	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.056	$V_{DD}/2$ – 0.005	$V_{DD}/2$ + 0.043	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.338	$V_{DD}/2$ – 1.298	$V_{DD}/2$ – 1.255	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.293	$V_{DD}/2$ + 1.356	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.057	$V_{DD}/2$ – 0.006	$V_{DD}/2$ + 0.044	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.337	$V_{DD}/2$ – 1.298	$V_{DD}/2$ – 1.256	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.294	$V_{DD}/2$ + 1.359	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.047	$V_{DD}/2$ – 0.004	$V_{DD}/2$ + 0.035	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.338	$V_{DD}/2$ – 1.299	$V_{DD}/2$ – 1.258	V

Table 15. 3.3-V DC Analog Reference Specifications

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b000	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	$V_{DD}/2$ + BandGap	$V_{DD}/2$ + 1.225	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.361	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.067	$V_{DD}/2$ – 0.002	$V_{DD}/2$ + 0.063	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – BandGap	$V_{DD}/2$ – 1.35	$V_{DD}/2$ – 1.293	$V_{DD}/2$ – 1.210	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	$V_{DD}/2$ + BandGap	$V_{DD}/2$ + 1.218	$V_{DD}/2$ + 1.294	$V_{DD}/2$ + 1.370	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.038	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.035	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – BandGap	$V_{DD}/2$ – 1.329	$V_{DD}/2$ – 1.296	$V_{DD}/2$ – 1.259	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	$V_{DD}/2$ + BandGap	$V_{DD}/2$ + 1.221	$V_{DD}/2$ + 1.294	$V_{DD}/2$ + 1.366	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.050	$V_{DD}/2$ – 0.002	$V_{DD}/2$ + 0.046	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – BandGap	$V_{DD}/2$ – 1.331	$V_{DD}/2$ – 1.296	$V_{DD}/2$ – 1.260	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	$V_{DD}/2$ + BandGap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.295	$V_{DD}/2$ + 1.365	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.028	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.025	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – BandGap	$V_{DD}/2$ – 1.329	$V_{DD}/2$ – 1.297	$V_{DD}/2$ – 1.262	V
0b001	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.098	P2[4] + P2[6] – 0.018	P2[4] + P2[6] + 0.055	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.055	P2[4] – P2[6] + 0.013	P2[4] – P2[6] + 0.086	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.082	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.050	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.037	P2[4] – P2[6] + 0.006	P2[4] – P2[6] + 0.054	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	P2[4] + P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.079	P2[4] + P2[6] – 0.012	P2[4] + P2[6] + 0.047	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.038	P2[4] – P2[6] + 0.006	P2[4] – P2[6] + 0.057	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.080	P2[4] + P2[6] – 0.008	P2[4] + P2[6] + 0.055	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.032	P2[4] – P2[6] + 0.003	P2[4] – P2[6] + 0.042	V

Table 15. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b010	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.06	V_{DD} – 0.010	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.05	$V_{DD}/2$ – 0.002	$V_{DD}/2$ + 0.040	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.009	Vss + 0.056	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.060	V_{DD} – 0.006	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.028	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.025	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.005	Vss + 0.034	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.058	V_{DD} – 0.008	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.037	$V_{DD}/2$ – 0.002	$V_{DD}/2$ + 0.033	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.007	Vss + 0.046	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.057	V_{DD} – 0.006	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.025	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.022	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.004	Vss + 0.030	V
0b011	All power settings. Not allowed for 3.3 V	–	–	–	–	–	–	–
0b100	All power settings. Not allowed for 3.3 V	–	–	–	–	–	–	–
0b101	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	P2[4] + BandGap ($P2[4] = V_{DD}/2$)	P2[4] + 1.213	P2[4] + 1.291	P2[4] + 1.367	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V_{REFLO}	Ref Low	P2[4] – BandGap ($P2[4] = V_{DD}/2$)	P2[4] – 1.333	P2[4] – 1.294	P2[4] – 1.208	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + BandGap ($P2[4] = V_{DD}/2$)	P2[4] + 1.217	P2[4] + 1.294	P2[4] + 1.368	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V_{REFLO}	Ref Low	P2[4] – BandGap ($P2[4] = V_{DD}/2$)	P2[4] – 1.320	P2[4] – 1.296	P2[4] – 1.261	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	P2[4] + BandGap ($P2[4] = V_{DD}/2$)	P2[4] + 1.217	P2[4] + 1.294	P2[4] + 1.369	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V_{REFLO}	Ref Low	P2[4] – BandGap ($P2[4] = V_{DD}/2$)	P2[4] – 1.322	P2[4] – 1.297	P2[4] – 1.262	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + BandGap ($P2[4] = V_{DD}/2$)	P2[4] + 1.219	P2[4] + 1.295	P2[4] + 1.37	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V_{REFLO}	Ref Low	P2[4] – BandGap ($P2[4] = V_{DD}/2$)	P2[4] – 1.324	P2[4] – 1.297	P2[4] – 1.262	V

Table 15. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b110	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	2 × BandGap	2.507	2.598	2.698	V
		V_{AGND}	AGND	BandGap	1.203	1.307	1.424	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.012	Vss + 0.067	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	2 × BandGap	2.516	2.598	2.683	V
		V_{AGND}	AGND	BandGap	1.241	1.303	1.376	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.007	Vss + 0.040	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	2 × BandGap	2.510	2.599	2.693	V
		V_{AGND}	AGND	BandGap	1.240	1.305	1.374	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.008	Vss + 0.048	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	2 × BandGap	2.515	2.598	2.683	V
		V_{AGND}	AGND	BandGap	1.258	1.302	1.355	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.005	Vss + 0.03	V
0b111	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–

DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 16. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.2	–	kΩ	
C_{SC}	Capacitor Unit Value (Switched Capacitor)	–	80	–	fF	

DC POR, SMP, and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 17. DC POR, SMP, and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} Value for PPOR Trip (positive ramp)					
V_{PPOR0R}	PORLEV[1:0] = 00b		2.91		V	
V_{PPOR1R}	PORLEV[1:0] = 01b	–	4.39	–	V	
V_{PPOR2R}	PORLEV[1:0] = 10b		4.55		V	
	V_{DD} Value for PPOR Trip (negative ramp)					
V_{PPOR0}	PORLEV[1:0] = 00b		2.82		V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	4.39	–	V	
V_{PPOR2}	PORLEV[1:0] = 10b		4.55		V	
	PPOR Hysteresis					
V_{PH0}	PORLEV[1:0] = 00b	–	92	–	mV	
V_{PH1}	PORLEV[1:0] = 01b	–	0	–	mV	
V_{PH2}	PORLEV[1:0] = 10b	–	0	–	mV	

Notes
4. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
5. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

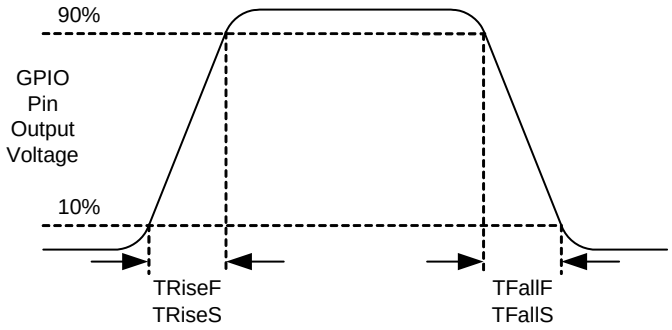
AC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 21. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12.3	MHz	Normal Strong Mode
TRiseF	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	V_{DD} = 4.75 to 5.25 V, 10% - 90%
TFallF	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	V_{DD} = 4.75 to 5.25 V, 10% - 90%
TRiseS	Rise time, slow strong mode, Cload = 50 pF	10	27	–	ns	V_{DD} = 3 to 5.25 V, 10% - 90%
TFallS	Fall time, slow strong mode, Cload = 50 pF	10	22	–	ns	V_{DD} = 3 to 5.25 V, 10% - 90%

Figure 10. GPIO Timing Diagram



AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = High and Opamp Bias = High is not supported at 3.3V.

Table 22. 5-V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time to 0.1% for a 1 V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 3.9 0.72 0.62	 µs µs µs	–
T_{SOA}	Falling Settling Time to 0.1% for a 1 V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 5.9 0.92 0.72	 µs µs µs	–
SR_{ROA}	Rising Slew Rate (20% to 80%) of a 1 V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.15 1.7 6.5	 – – –	 – – –	 V/µs V/µs V/µs	–
SR_{FOA}	Falling Slew Rate (20% to 80%) of a 1 V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.01 0.5 4.0	 – – –	 – – –	 V/µs V/µs V/µs	–
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz	–
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz	–

Table 23. 3.3-V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising settling time to 0.1% of a 1 V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 – –	 – –	 3.92 0.72	 µs µs	–
T_{SOA}	Falling settling time to 0.1% of a 1 V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 – –	 – –	 5.41 0.72	 µs µs	–
SR_{ROA}	Rising Slew Rate (20% to 80%) of a 1 V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 0.31 2.7	 – –	 – –	 V/µs V/µs	–
SR_{FOA}	Falling slew rate (20% to 80%) of a 1 V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 0.24 1.8	 – –	 – –	 V/µs V/µs	–
BW_{OA}	Gain bandwidth product Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 0.67 2.8	 – –	 – –	 MHz MHz	–
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz	–

Table 25. AC Digital Block Specifications (continued)

Function	Description	Min	Typ	Max	Unit	Notes
Transmitter	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8
	$V_{DD} \geq 4.75$ V, 2 stop bits	–	–	49.2	MHz	
	$V_{DD} \geq 4.75$ V, 1 stop bit	–	–	24.6	MHz	
	$V_{DD} < 4.75$ V	–	–	24.6	MHz	
Receiver	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8
	$V_{DD} \geq 4.75$ V, 2 stop bits	–	–	49.2	MHz	
	$V_{DD} \geq 4.75$ V, 1 stop bit	–	–	24.6	MHz	
	$V_{DD} < 4.75$ V	–	–	24.6	MHz	

AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and -40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and -40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 26. 5V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROB}	Rising Settling Time to 0.1%, 1 V Step, 100pF Load Power = Low Power = High	 – –	 – –	 4 4	 µs µs	
T_{SOB}	Falling Settling Time to 0.1%, 1 V Step, 100pF Load Power = Low Power = High	 – –	 – –	 3.4 3.4	 µs µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1 V Step, 100pF Load Power = Low Power = High	 0.5 0.5	 – –	 – –	 V/µs V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1 V Step, 100pF Load Power = Low Power = High	 0.55 0.55	 – –	 – –	 V/µs V/µs	
BW_{OB}	Small Signal Bandwidth, 20mV_{pp}, 3dB BW, 100pF Load Power = Low Power = High	 0.8 0.8	 – –	 – –	 MHz MHz	
BW_{OB}	Large Signal Bandwidth, 1V_{pp}, 3dB BW, 100pF Load Power = Low Power = High	 300 300	 – –	 – –	 kHz kHz	

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and -40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and -40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 30. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	–
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	–
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	–
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	–
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	–
T_{ERASEB}	flash Erase Time (Block)	–	10	–	ms	–
T_{WRITE}	flash Block Write Time	–	40	–	ms	–
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	$V_{DD} > 3.6$
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	50	ns	$3.0 \le V_{DD} \le 3.6$
$T_{ERASEALL}$	flash Erase Time (Bulk)	–	80	–	ms	Erase all blocks and protection fields at once.
$T_{PROGRAM\_HOT}$	flash Block Erase + flash Block Write Time	–	–	100[15]	ms	0°C ≤ T_J ≤ 100 °C
$T_{PROGRAM\_COLD}$	flash Block Erase + flash Block Write Time	–	–	200[15]	ms	-40°C ≤ T_J ≤ 0 °C

Note

15. For the full industrial range, the user must employ a Temperature Sensor User Module (flashTemp) and feed the result to the temperature argument before writing. Refer to the flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

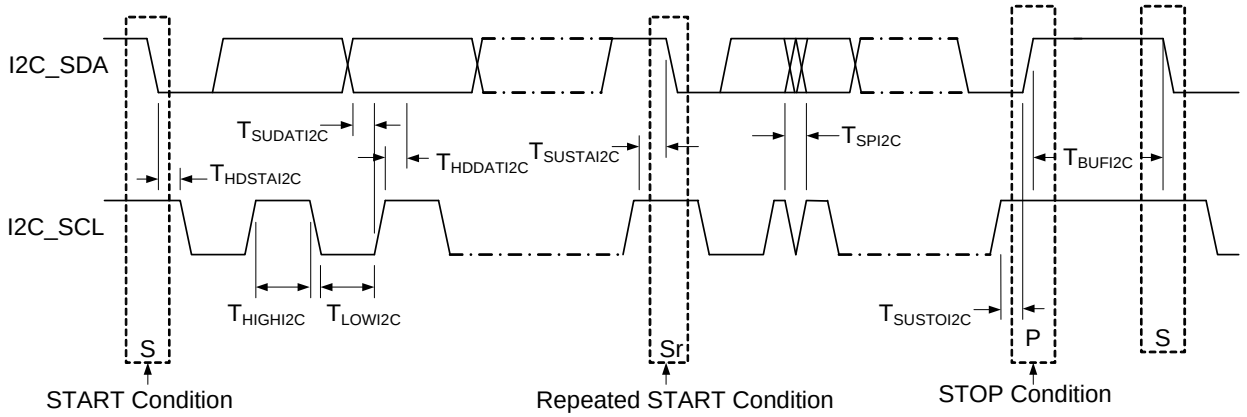
AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and -40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and -40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 31. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard-Mode		Fast-Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz	–
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	–
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs	–
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs	–
$T_{SUSTAI2C}$	Set-up Time for a Repeated START Condition	4.7	–	0.6	–	µs	–
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs	–
$T_{SUDATI2C}$	Data Set-up Time	250	–	100[16]	–	ns	–
$T_{SUSTOI2C}$	Set-up Time for STOP Condition	4.0	–	0.6	–	µs	–
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs	–
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns	–

Figure 13. Definition for Timing for Fast-/Standard-Mode on the I²C Bus



Note

16. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

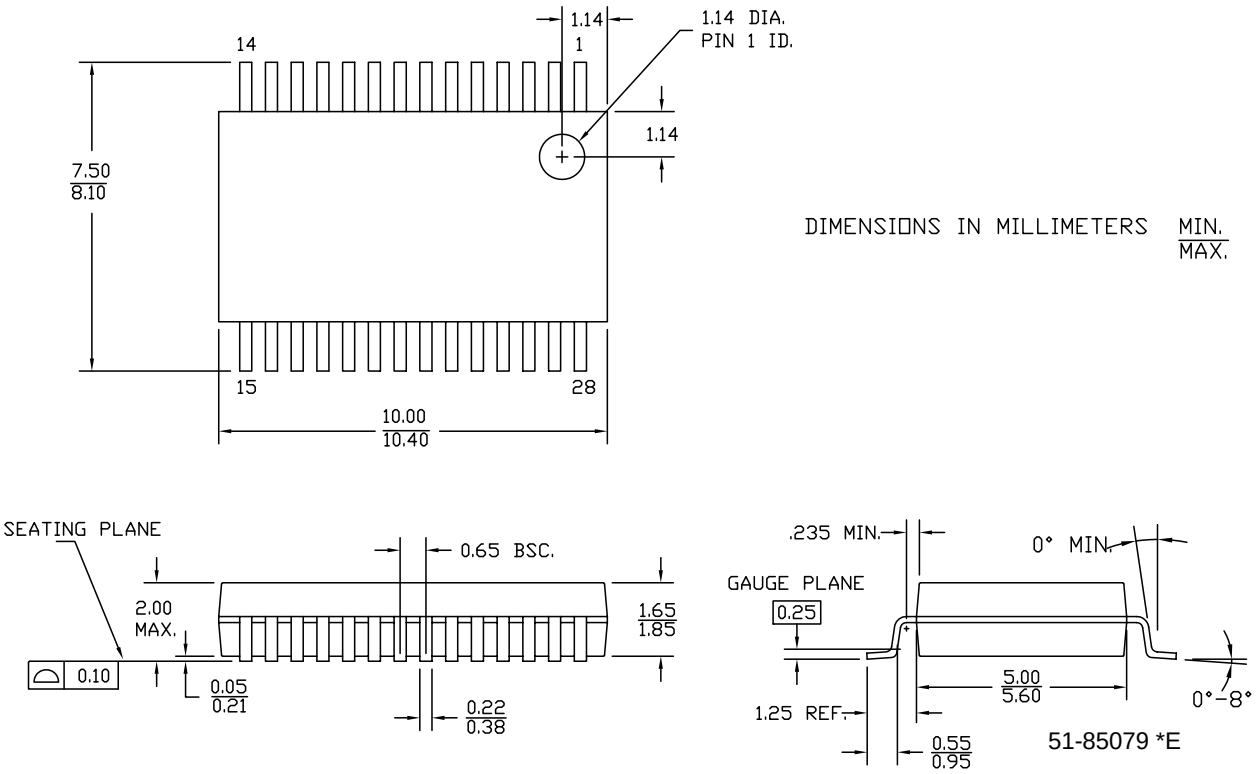
Packaging Information

This section illustrates the packaging specifications for the CY8CLED16 EZ-Color device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

Packaging Dimensions

Figure 14. 28-Pin (210-Mil) SSOP



Development Tool Selection

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at http://www.cypress.com and includes a free C compiler.

PSoC Programmer

PSoC Programmer is flexible and used on the bench in development. It is also suitable for factory programming. PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE Cube In-Circuit Emulator and PSoC MiniProg. It is available free of charge at http://www.cypress.com.

Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval Socket Programming and Evaluation board
- 28-Pin CY8C29466-24PXI PDIP PSoC device sample
- 28-Pin CY8C27443-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

Device Programmers

All device programmers are sold at the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- Three Programming Module cards
- MiniProg programming unit
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment.
Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 programmer unit
- PSoC ISSP software CD
- 110 ~ 240V power supply, euro-plug adapter
- USB 2.0 cable