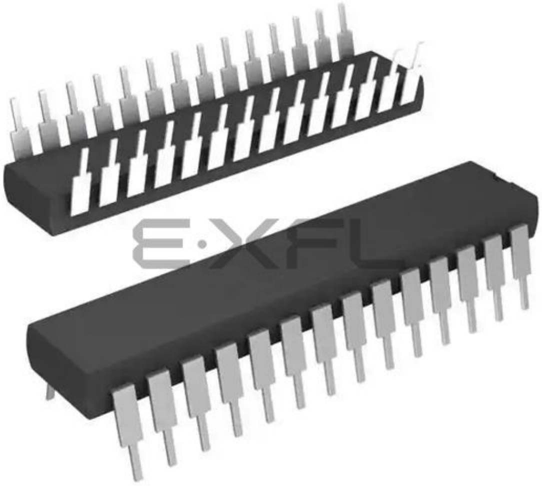


What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	LINbus, SCI
Peripherals	LVD, POR, PWM
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08se8crl

Table of Contents

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to: freescale.com

The following revision history table summarizes changes contained in this document.

Revision	Date	Description of Changes
1	10/8/2008	Initial public released.
2	1/16/2009	In Table 8, added the Max. of S2I_{DD} and S3I_{DD} in 0–105 °C; changed the Max. of S2I_{DD} and S3I_{DD} in 0–85 °C; changed the typical of S2I_{DD} and S3I_{DD}; changed the S23I_{DDRTI} to P.
3	4/7/2009	Added $\|I_{OZTOT}\|$ in the Table 7. Changed V_{DDAD} to V_{DDA}, V_{SSAD} to V_{SSA}. Updated Table 9, Table 10, Table 11, and Table 12. Updated Figure 13 and Figure 14.
4	4/10/2015	Updated Table 9.

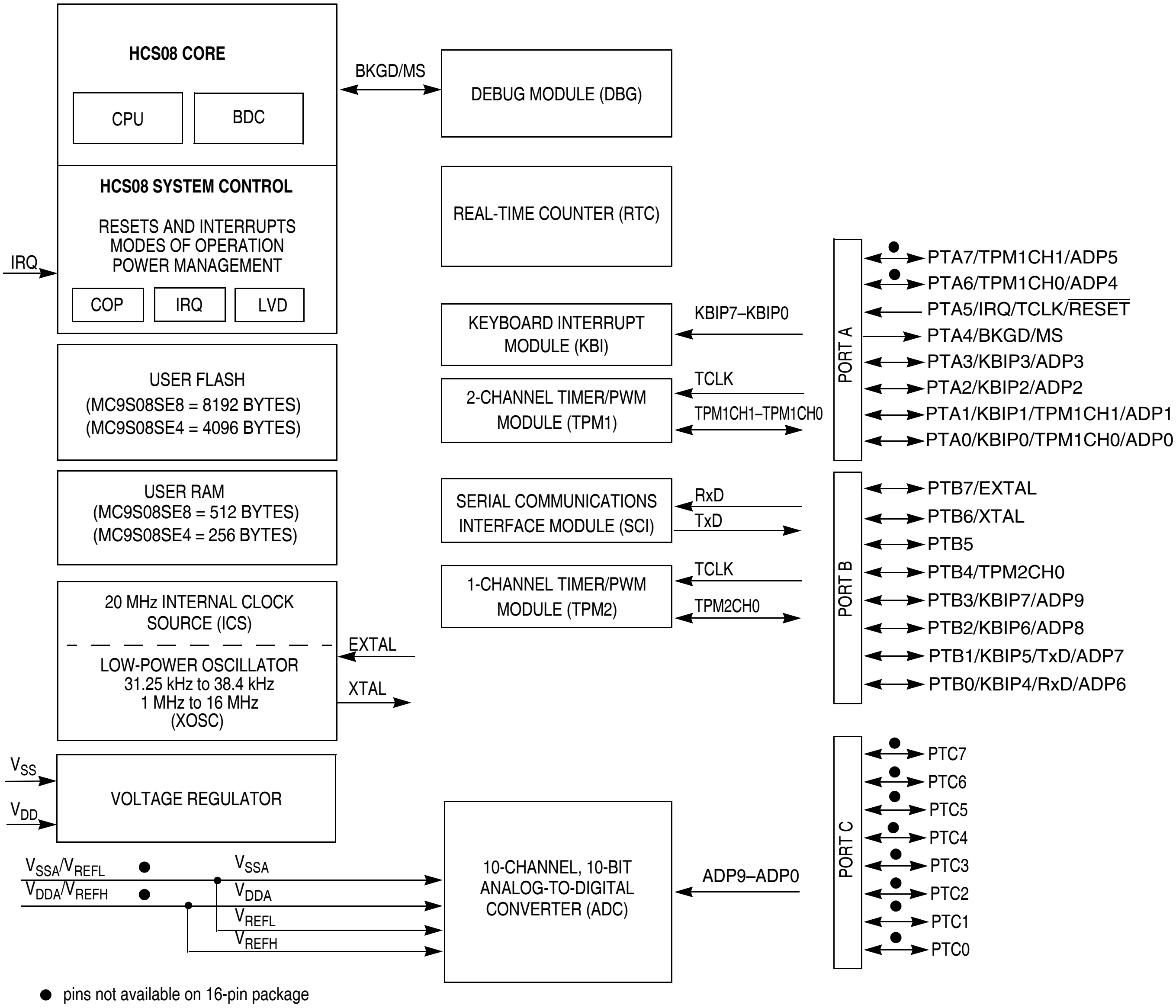
Related Documentation

Find the most current versions of all documents at: http://www.freescale.com

Reference Manual	**(MC9S08SE8RM)** Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 MCU Block Diagram

The block diagram, Figure 1, shows the structure of the MC9S08SE8 series MCUs.



Notes:

When PTA4 is configured as BKGD, pin is bi-directional.

For the 16-pin package: V_{SSA}/V_{REFL} and V_{DDA}/V_{REFH} are double bonded to V_{SS} and V_{DD} respectively.

Figure 1. MC9S08SE8 Series Block Diagram

3 Electrical Characteristics

This chapter contains electrical and timing specifications.

3.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 5.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

[1] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

[2] All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

[3] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

Rating		Symbol	Value	Unit
Operating temperature range (packaged)		T_A	T_L to T_H	°C
	C		–40 to 85	
	V		–40 to 105	
	M		–40 to 125	
Maximum junction temperature		T_{JM}	135	°C
Thermal resistance single-layer board	28-pin SOIC	θ_{JA}	70	°C/W
	28-pin PDIP		68	
	16-pin TSSOP		129	
Thermal resistance four-layer board	28-pin SOIC		48	°C/W
	28-pin PDIP		49	
	16-pin TSSOP		85	

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

Where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user-determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \qquad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \qquad \textit{Eqn. 3}$$

Where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.4 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 5. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	—
Machine	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	—

Table 5. ESD and Latch-up Test Conditions (continued)

Model	Description	Symbol	Value	Unit
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 6. ESD and Latch-up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Machine model (MM)	V_{MM}	±200	—	V
3	Charge device model (CDM)	V_{CDM}	±500	—	V
4	Latch-up current at T_A = 125 °C	I_{LAT}	±100	—	mA

[1] Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.5 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 7. DC Characteristics

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
1	—	Operating voltage	—	2.7	—	5.5	V
2	P	Output high voltage — Low drive (PTxDSn = 0)	V_{OH}				V
		5 V, I_{Load} = –2 mA		V_{DD} – 1.5	—	—	
		3 V, I_{Load} = –0.6 mA		V_{DD} – 1.5	—	—	
		5 V, I_{Load} = –0.4 mA		V_{DD} – 0.8	—	—	
		3 V, I_{Load} = –0.24 mA		V_{DD} – 0.8	—	—	
		Output high voltage — High drive (PTxDSn = 1)					
		5 V, I_{Load} = –10 mA		V_{DD} – 1.5	—	—	
		3 V, I_{Load} = –3 mA		V_{DD} – 1.5	—	—	
		5 V, I_{Load} = –2 mA		V_{DD} – 0.8	—	—	
		3 V, I_{Load} = –0.4 mA		V_{DD} – 0.8	—	—	
3	P	Output low voltage — Low drive (PTxDSn = 0)	V_{OL}				V
		5 V, I_{Load} = 2 mA		1.5	—	—	
		3 V, I_{Load} = 0.6 mA		1.5	—	—	
		5 V, I_{Load} = 0.4 mA		0.8	—	—	
		3 V, I_{Load} = 0.24 mA		0.8	—	—	
		Output low voltage — High drive (PTxDSn = 1)					
		5 V, I_{Load} = 10 mA		1.5	—	—	
		3 V, I_{Load} = 3 mA		1.5	—	—	
		5 V, I_{Load} = 2 mA		0.8	—	—	
		3 V, I_{Load} = 0.4 mA		0.8	—	—	
4	P	Output high current — Max total I_{OH} for all ports	I_{OHT}				mA
		5 V		—	—	100	
		3 V		—	—	60	

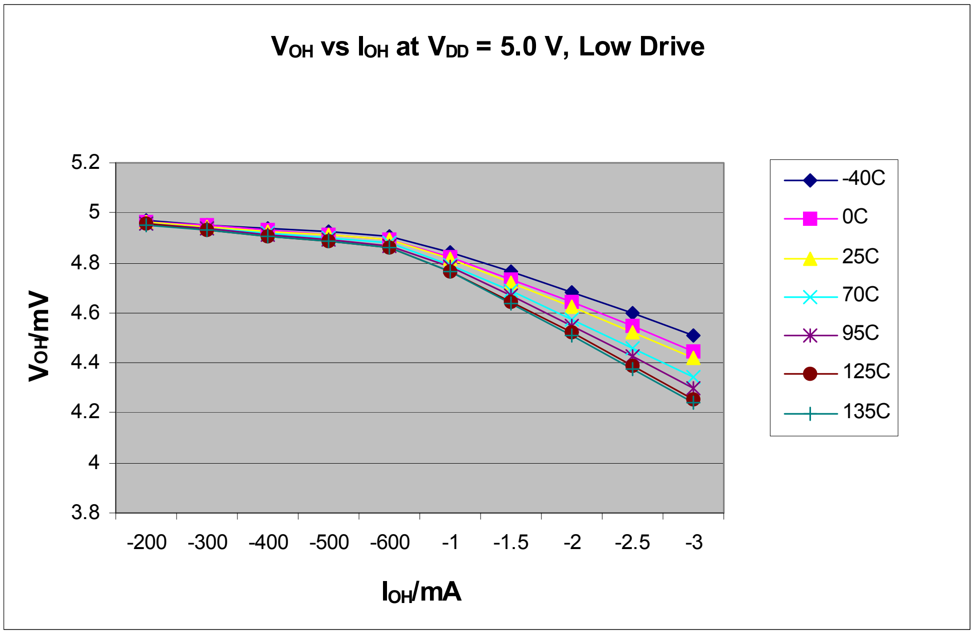


Figure 10. Typical V_{OH} vs. I_{OH} for Low Drive Enabled Pad (V_{DD} = 5 V)

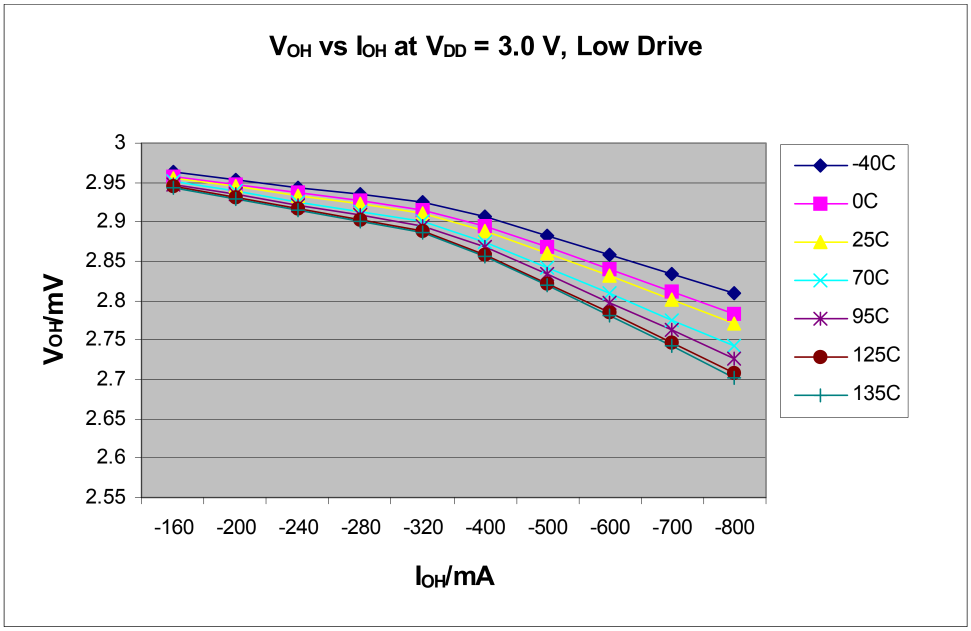


Figure 11. Typical V_{OH} vs. I_{OH} for Low Drive Enabled Pad (V_{DD} = 3 V)

3.6 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 8. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max	Unit	Temp (°C)
1	C	Run supply current[2] measured at (CPU clock = 4 MHz, f_{Bus} = 2 MHz)	RI_{DD}	5	2.4	2.72	mA	–40 to 125
				3	2.18	2.26		
2	P	Run supply current[2] measured at (CPU clock = 20 MHz, f_{Bus} = 10 MHz)	RI_{DD}	5	6.35	7.29	mA	–40 to 125
				3	5.79	6.42		
3	P	Wait supply current[2] measured at f_{Bus} = 2 MHz	WI_{DD}	5	1.4	1.56	mA	–40 to 125
				3	1.36	1.53		
4	P	Stop2 mode supply current	$S2I_{DD}$	5	1.4	19 28 45.8	µA	–40 to 85 –40 to 105 –40 to 125
				3	1.3	15 22 37.2	µA	–40 to 85 –40 to 105 –40 to 125
5	P	Stop3 mode supply current	$S3I_{DD}$	5	1.61	23 43 76.1	µA	–40 to 85 –40 to 105 –40 to 125
				3	1.44	19 38 66.4	µA	–40 to 85 –40 to 105 –40 to 125
6	P	RTC adder to stop2 or stop3[3]	$S23I_{DDRTI}$	5	300	500 500	nA	–40 to 85 –40 to 125
				3	300	500 500	nA	–40 to 85 –40 to 125
7	C	LVD adder to stop3 (LVDE = LVDSE = 1)	$S3I_{DDLVD}$	5	122	180	µA	–40 to 125
				3	110	160	µA	–40 to 125
8	C	Adder to stop3 for oscillator enabled[4] (OSCSTEN =1)	$S3I_{DDOSC}$	5,3	5	8	µA	–40 to 125

---

[1] Typical values are based on characterization data at 25 °C unless otherwise stated. See Figure 12 through Figure 13 for typical curves across voltage/temperature.

[2] All modules except ADC active, ICS configured for FBE, and does not include any dc loads on port pins.

[3] Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode. Wait mode typical is 220 µA at 5 V with f_{Bus} = 1 MHz.

[4] Values given under the following conditions: low range operation (RANGE = 0) with a 32.768 kHz crystal and low power mode (HGO = 0).

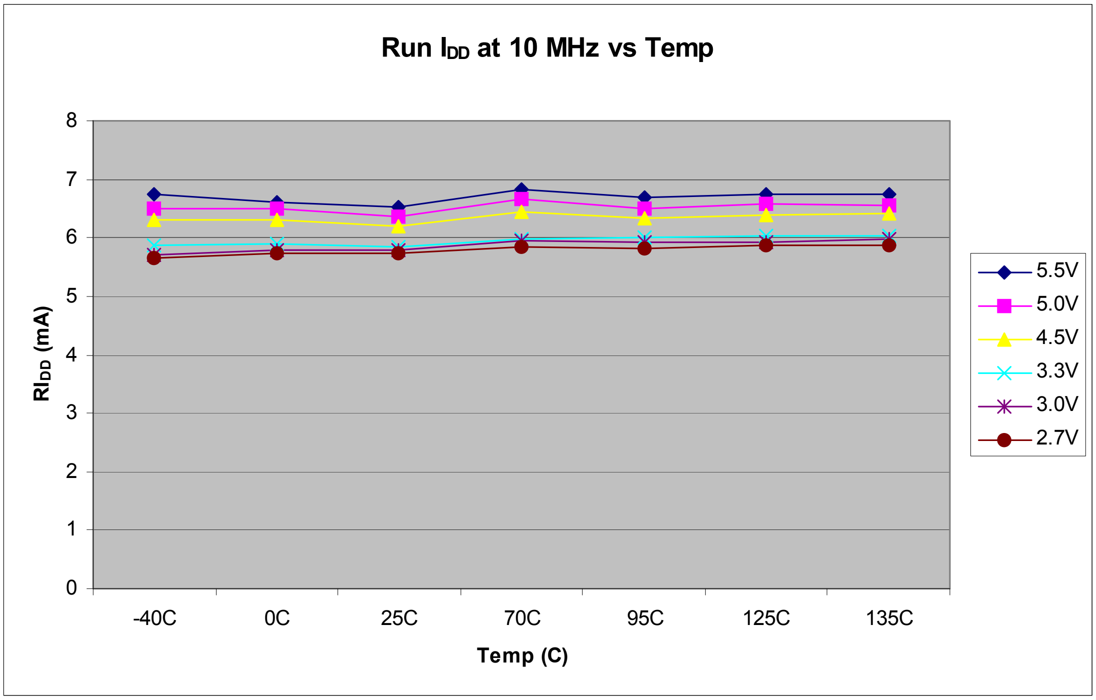


Figure 12. Typical Run I_{DD} Curves

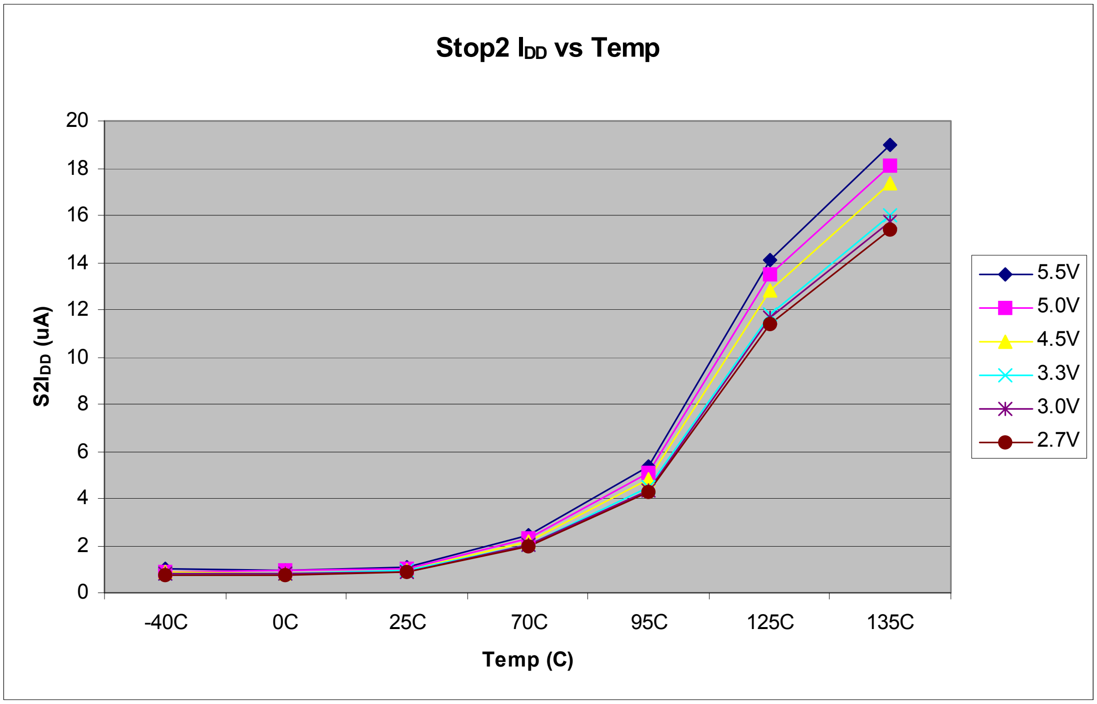


Figure 13. Typical Stop2 I_{DD} Curves

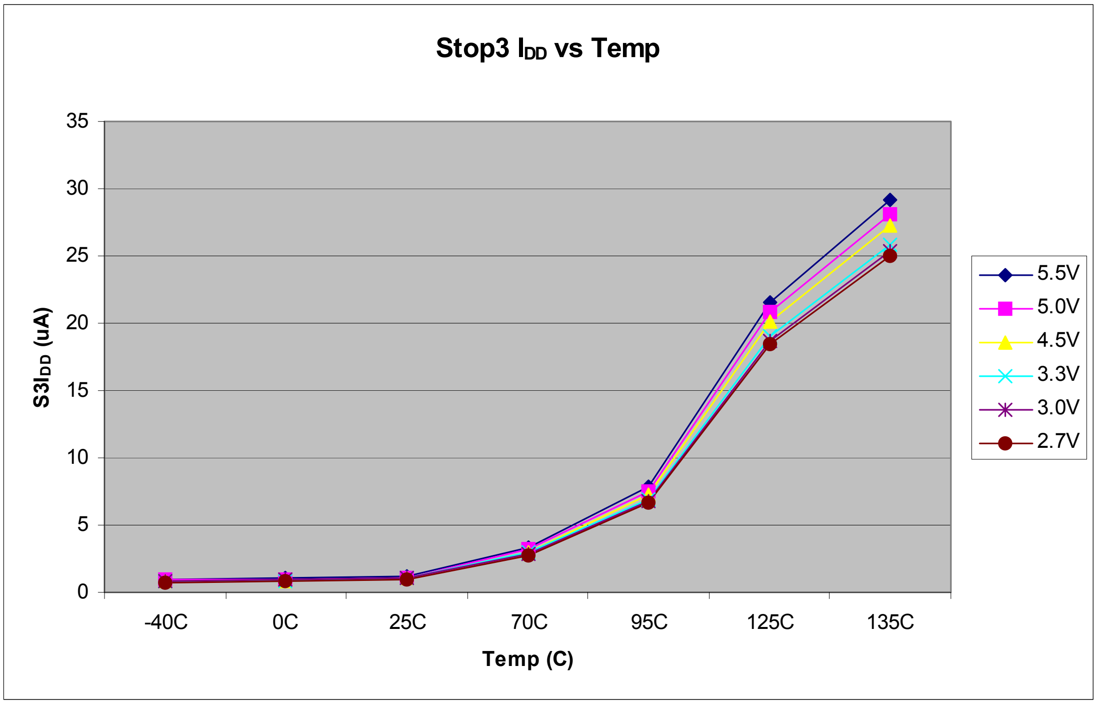


Figure 14. Typical Stop3 I_{DD} Curves

3.7 External Oscillator (XOSC) Characteristics

Table 9. Oscillator electrical specifications (Temperature Range = –40 to 125°C Ambient)

Num	C	Characteristic	Symbol	Min.	Typical[1]	Max.	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1)[2] High range (RANGE = 1), low power (HGO = 0)[2]	f_{lo} $f_{hi\text{-}hgo}$ $f_{hi\text{-}lp}$	32 1 1	— — —	38.4 16 8	kHz MHz MHz
2	—	Load capacitors	C_1,C_2	See crystal or resonator manufacturer's recommendation			
3	—	Feedback resistor Low range (32 kHz to 100 kHz) High range (1 MHz to 16 MHz)	R_F	— —	10 1	— —	MΩ
4	—	Series resistor Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0)	R_S	— — —	0 100 0	— — —	kΩ
		High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz		— — —	0 0 0	0 10 20	

Table 9. Oscillator electrical specifications (Temperature Range = –40 to 125°C Ambient)

Num	C	Characteristic	Symbol	Min.	Typical[1]	Max.	Unit
5	T	Crystal start-up time[3] Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0)[4] High range, high gain (RANGE = 1, HGO = 1)[4]	 $t_{CSTL-LP}$ $t_{CSTH-HGO}$ $t_{CSTH-LP}$ $t_{CSTH-HGO}$	 — — — —	 200 400 5 15	 — — — —	ms
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE or FBE mode [2] FBELP mode	f_{extal}	 0.03125 0	 — —	 20 20	 MHz MHz

[1] Typical column was characterized at 5.0 V, 25 °C or is recommended value.

[2] The input clock source must be divided using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

[3] This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications. This data will vary based upon the crystal manufacturer and board design. The crystal should be characterized by the crystal manufacturer.

[4] 4 MHz crystal.

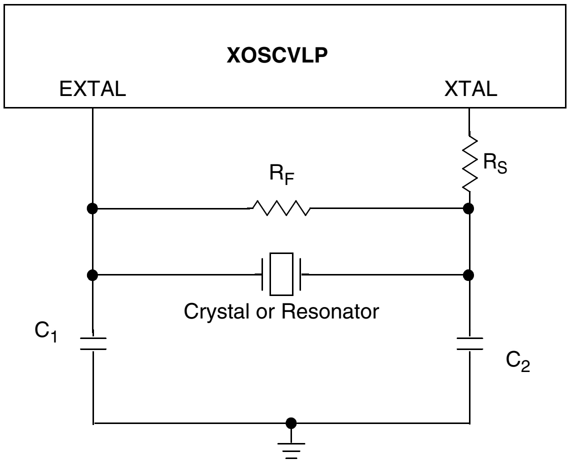


Figure 15. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

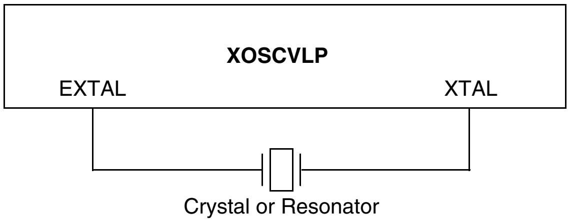


Figure 16. Typical Crystal or Resonator Circuit: Low Range/Low Power

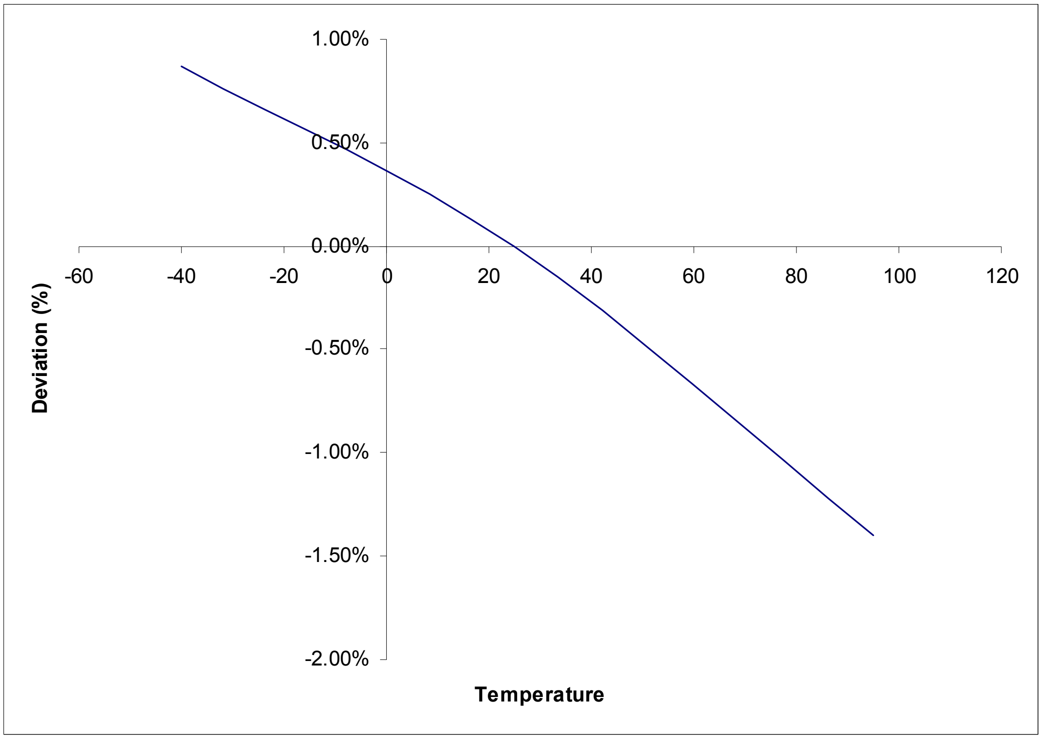


Figure 17. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

3.9 ADC Characteristics

Table 11. 10-Bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	
	Delta to V_{DD} $(V_{DD} - V_{DDA})^2$	ΔV_{DDA}	–100	0	100	mV	
Ground voltage	Delta to V_{SS} $(V_{SS} - V_{SSA})^2$	ΔV_{SSA}	–100	0	100	mV	
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	3	5	kΩ	
Analog source resistance	10-bit mode $f_{ADCK} > 4MHz$ $f_{ADCK} < 4MHz$	R_{AS}	— —	— —	5 10	kΩ	External to MCU
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock frequency	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low power (ADLPC = 1)		0.4	—	4.0		

Table 12. 10-Bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	D	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
	Low Power (ADLPC = 1)			1.25	2	3.3		
Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	D	t_{ADC}	—	20	—	ADCK cycles	See SE8 reference manual for conversion time variances
	Long Sample (ADLSMP = 1)			—	40	—		
Sample Time	Short Sample (ADLSMP = 0)	D	t_{ADS}	—	3.5	—	ADCK cycles	
	Long Sample (ADLSMP = 1)			—	23.5	—		
Temp Sensor Slope	–40°C– 25°C	D	m	—	3.266	—	mV/°C	
	25°C– 125°C			—	3.638	—		
Temp Sensor Voltage	25°C	D	V_{TEMP25}	—	1.396	—	mV	
Characteristics for 28-pin packages only								
Total Unadjusted Error	10-bit mode	P	E_{TUE}	—	±1	±2.5	LSB[3]	Includes quantization
	8-bit mode	P		—	±0.5	±1.0		
Differential Non-Linearity	10-bit mode[2]	P	DNL	—	±0.5	±1.0	LSB[3]	
	8-bit mode[3]	P		—	±0.3	±0.5		
Integral Non-Linearity	10-bit mode	T	INL	—	±0.5	±1.0	LSB[3]	
	8-bit mode	T		—	±0.3	±0.5		
Zero-Scale Error	10-bit mode	P	E_{ZS}	—	±0.5	±1.5	LSB[3]	$V_{ADIN} = V_{SSA}$
	8-bit mode	P		—	±0.5	±0.5		
Full-Scale Error	10-bit mode	T	E_{FS}	—	±0.5	±1	LSB[3]	$V_{ADIN} = V_{DDA}$
	8-bit mode	T		—	±0.5	±0.5		
Quantization Error	10-bit mode	D	E_Q	—	—	±0.5	LSB[3]	
	8-bit mode			—	—	±0.5		
Input Leakage Error	10-bit mode	D	E_{IL}	—	±0.2	±2.5	LSB[3]	Pad leakage[4] * R_{AS}
	8-bit mode			—	±0.1	±1		
Characteristics for 16-pin package only								
Total Unadjusted Error	10-bit mode	P	E_{TUE}	—	±1.5	±3.5	LSB[3]	Includes quantization
	8-bit mode	P		—	±0.7	±1.5		

Table 12. 10-Bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
Differential Non-Linearity	10-bit mode[3]	P	DNL	—	±0.5	±1.0	LSB[3]	
	8-bit mode[3]	P		—	±0.3	±0.5		
Integral Non-Linearity	10-bit mode	T	INL	—	±0.5	±1.0	LSB[3]	
	8-bit mode	T		—	±0.3	±0.5		
Zero-Scale Error	10-bit mode	P	E_{ZS}	—	±1.5	±2.1	LSB[3]	$V_{ADIN} = V_{SSA}$
	8-bit mode	P		—	±0.5	±0.7		
Full-Scale Error	10-bit mode	T	E_{FS}	—	±1	±1.5	LSB[3]	$V_{ADIN} = V_{DDA}$
	8-bit mode	T		—	±0.5	±0.5		
Quantization Error	10-bit mode	D	E_Q	—	—	±0.5	LSB[3]	
	8-bit mode			—	—	±0.5		
Input Leakage Error	10-bit mode	D	E_{IL}	—	±0.2	±2.5	LSB[3]	Pad leakage[4] * R_{AS}
	8-bit mode			—	±0.1	±1		

[1] Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] Monotonicity and No-Missing-Codes guaranteed in 10-bit and 8-bit modes

[3] 1 LSB =$(V_{REFH} - V_{REFL})/2^N$

[4] Based on input pad leakage current. Refer to pad electricals.

3.10 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 13. Control Timing

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	DC	—	10	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	µs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive[3]	t_{rstdrv}	$34 \times t_{cyc}$	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes[4]	t_{MSH}	100	—	—	µs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[5]	t_{ILIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	—	—	ns
8	D	Pin interrupt pulse width Asynchronous path[2] Synchronous path[5]	t_{ILIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	—	—	ns
9	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	—	40 75	—	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF) Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	—	11 35	—	ns

[1] Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

[2] This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

[3] When any reset is initiated, internal circuitry drives the reset pin (if enabled, RSTPE = 1) low for about 34 cycles of t_{cyc}.

[4] To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

[5] This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

[6] Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 125 °C.

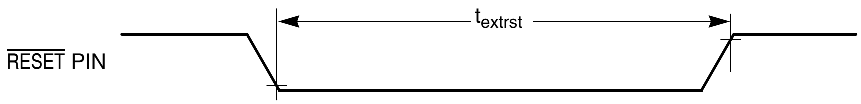


Figure 19. Reset Timing

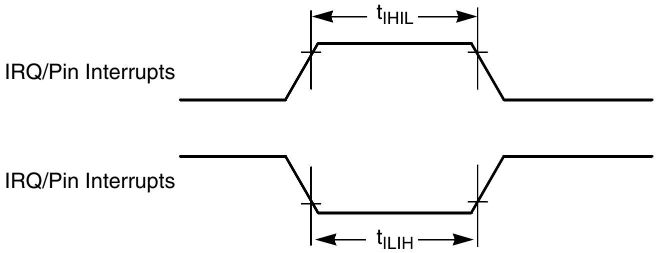


Figure 20. IRQ/Pin Interrupt Timing

3.10.2 TPM/MTIM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 14. TPM Input Timing

Num	C	Rating	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TPMext}	DC	$f_{Bus}/4$	MHz
2	D	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

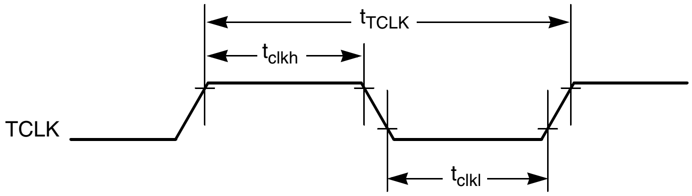


Figure 21. Timer External Clock

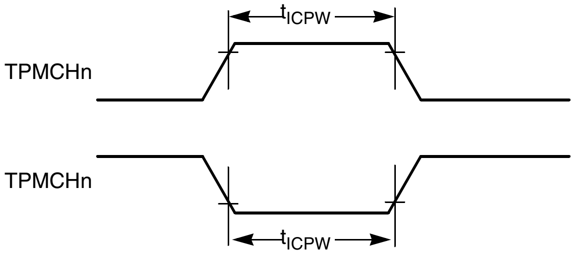


Figure 22. Timer Input Capture Pulse

3.11 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section in the reference manual.

Table 15. Flash Characteristics

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage for program/erase	$V_{prog/erase}$	2.7	—	5.5	V
2	D	Supply voltage for read operation	V_{Read}	2.7	—	5.5	V
3	D	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz
4	D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	μs
5	P	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}
6	P	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}
7	P	Page erase time[2]	t_{Page}	4000			t_{Fcyc}
8	P	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}
9	C	Program/erase endurance[3] T_L to T_H = –40 °C to 125 °C T = 25 °C	n_{FLPE}	10,000	— 100,000	—	cycles
10	C	Data retention[4]	t_{D_ret}	15	100	—	years

[1] The frequency of this clock is controlled by a software setting.

[2] These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

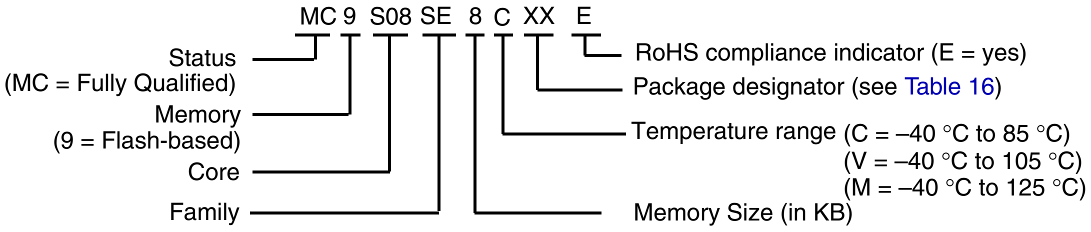
[3] **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory.*

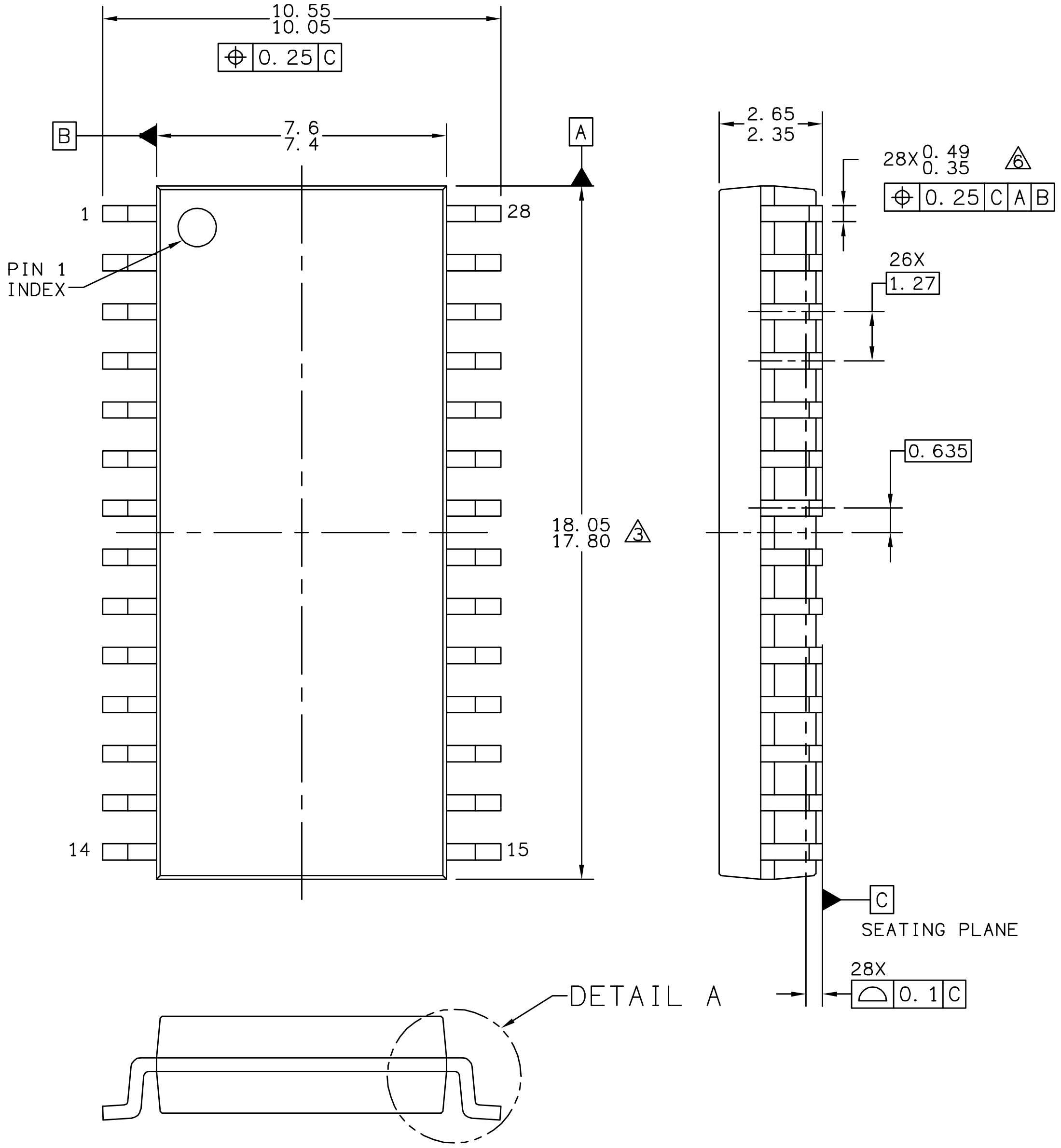
[4] **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25 °C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory.*

4 Ordering Information

This chapter contains ordering information for the device numbering system.

Example of the device numbering system:





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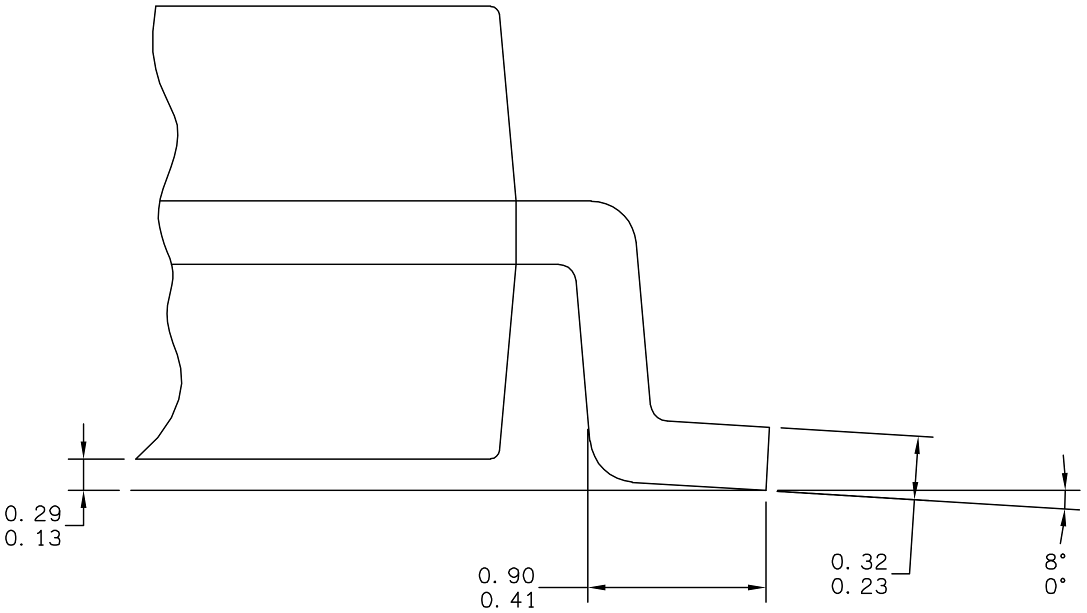
	CASE NUMBER: 751F-05	10 MAR 2005
	STANDARD: MS-013AE	



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TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE	DOCUMENT NO: 98ASB42345B	REV: G
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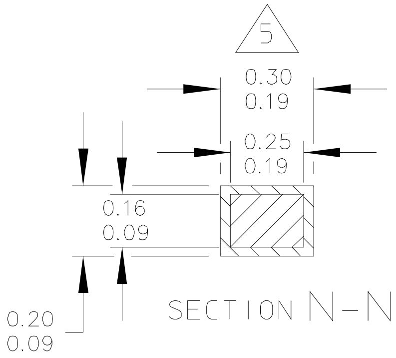

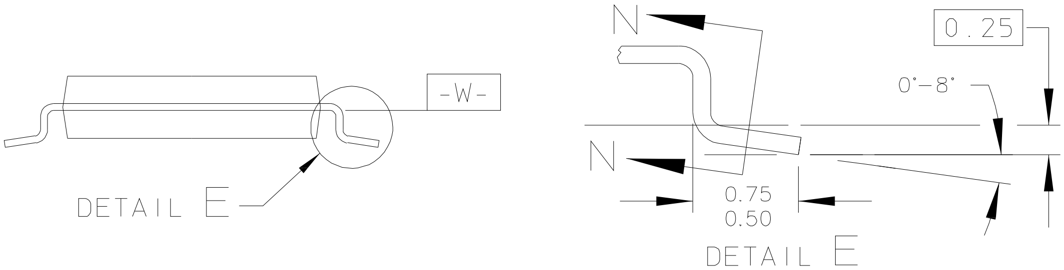

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	CASE NUMBER: 948F-01	19 MAY 2005
	STANDARD: JEDEC	