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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	LINbus, SCI
Peripherals	LVD, POR, PWM
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08se8cwl

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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to: freescale.com

The following revision history table summarizes changes contained in this document.

Revision	Date	Description of Changes
1	10/8/2008	Initial public released.
2	1/16/2009	In Table 8, added the Max. of $S2I_{DD}$ and $S3I_{DD}$ in 0–105 °C; changed the Max. of $S2I_{DD}$ and $S3I_{DD}$ in 0–85 °C; changed the typical of $S2I_{DD}$ and $S3I_{DD}$; changed the $S23I_{DDRTI}$ to P.
3	4/7/2009	Added $\lvert I_{OZTOT}\rvert$ in the Table 7. Changed V_{DDAD} to V_{DDA}, V_{SSAD} to V_{SSA}. Updated Table 9, Table 10, Table 11, and Table 12. Updated Figure 13 and Figure 14.
4	4/10/2015	Updated Table 9.

Related Documentation

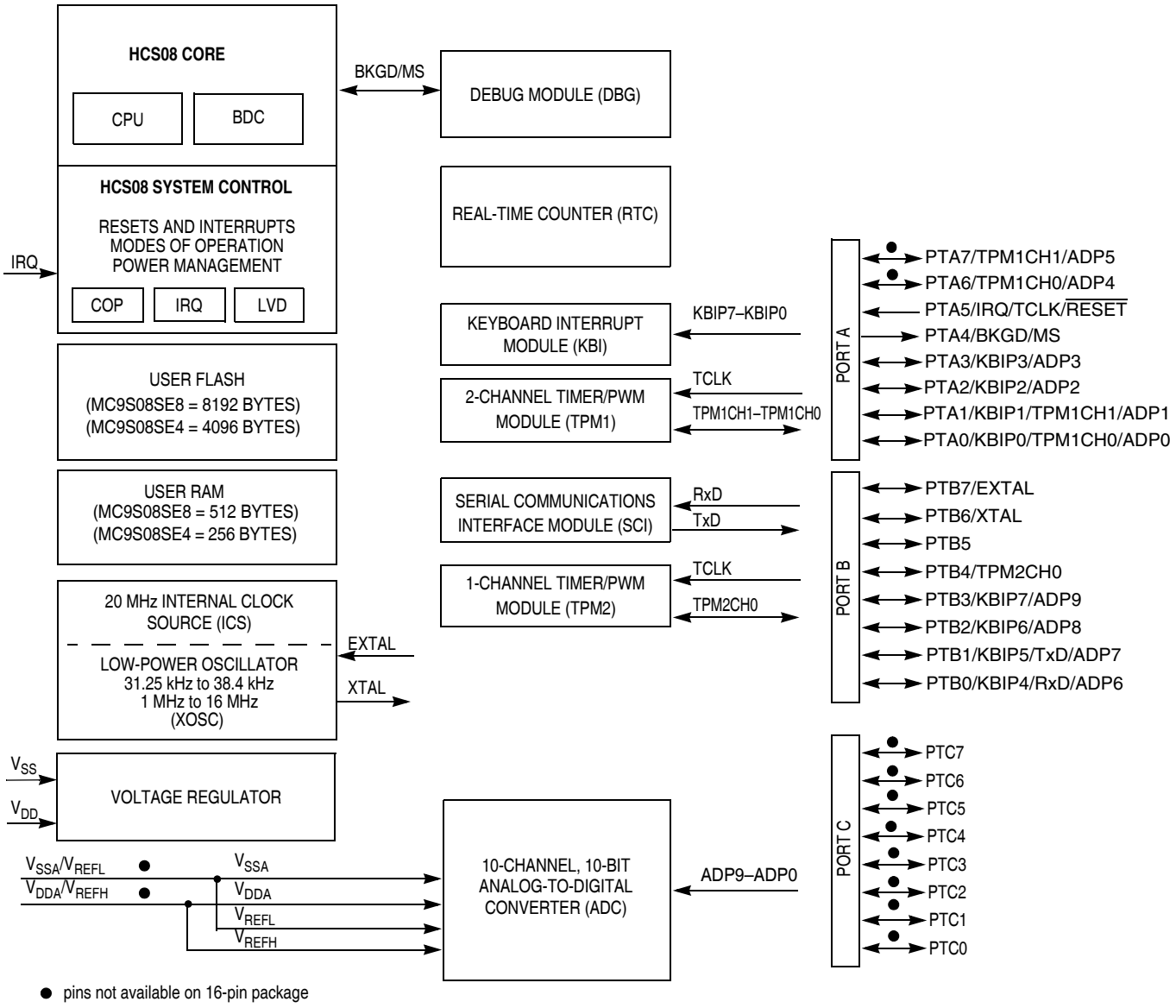
Find the most current versions of all documents at: http://www.freescale.com

Reference Manual (MC9S08SE8RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 MCU Block Diagram

The block diagram, Figure 1, shows the structure of the MC9S08SE8 series MCUs.



● pins not available on 16-pin package

Notes:

When PTA4 is configured as BKGD, pin is bi-directional.

For the 16-pin package: V_{SSA}/V_{REFL} and V_{DDA}/V_{REFH} are double bonded to V_{SS} and V_{DD} respectively.

Figure 1. MC9S08SE8 Series Block Diagram

2 Pin Assignments

This chapter shows the pin assignments in the packages available for the MC9S08SE8 series.

Table 1. Pin Availability by Package Pin-Count

Pin Number (Package)		<-- Lowest **Priority** --> Highest			
28 (SOIC/PDIP)	**16 (TSSOP)**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**
1	—	PTC5			
2	—	PTC4			
3	1	PTA5	IRQ	TCLK	$\overline{\text{RESET}}$
4	2	PTA4		BKGD	MS
5	3				V_{DD}
6	—			V_{DDA}	V_{REFH}
7	—			V_{SSA}	V_{REFL}
8	4				V_{SS}
9	5	PTB7	EXTAL		
10	6	PTB6	XTAL		
11	7	PTB5			
12	8	PTB4		TPM2CH0	
13	—	PTC3			
14	—	PTC2			
15	—	PTC1			
16	—	PTC0			
17	9	PTB3	KBIP7		ADP9
18	10	PTB2	KBIP6		ADP8
19	11	PTB1	KBIP5	TxD	ADP7
20	12	PTB0	KBIP4	RxD	ADP6
21	—	PTA7		TPM1CH1[1]	ADP5
22	—	PTA6		TPM1CH0[1]	ADP4
23	13	PTA3	KBIP3		ADP3
24	14	PTA2	KBIP2		ADP2
25	15	PTA1	KBIP1	TPM1CH1[1]	ADP1
26	16	PTA0	KBIP0	TPM1CH0[1]	ADP0
27	—	PTC7			
28	—	PTC6			

[1] TPM1 pins can be remapped to PTA7, PTA6 and PTA1,PTA0

3 Electrical Characteristics

This chapter contains electrical and timing specifications.

3.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 5.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

Rating		Symbol	Value	Unit
Operating temperature range (packaged) C V M		T_A	T_L to T_H –40 to 85 –40 to 105 –40 to 125	°C
Maximum junction temperature		T_{JM}	135	°C
Thermal resistance single-layer board	28-pin SOIC	θ_{JA}	70	°C/W
	28-pin PDIP		68	
	16-pin TSSOP		129	
Thermal resistance four-layer board	28-pin SOIC		48	°C/W
	28-pin PDIP		49	
	16-pin TSSOP		85	

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

Where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user-determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

Where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.4 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 5. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	—
Machine	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	—

Table 7. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
25	T	Low-voltage inhibit reset/recover hysteresis 5 V 3 V	V_{hys}	 — —	 100 60	 — —	mV
26	P	Bandgap voltage reference[9]	V_{BG}	1.18	1.20	1.21	V

1 Typical values are measured at 25 °C. Characterized, not tested.

2 Measured with $V_{In} = V_{DD}$ or V_{SS}.

3 Measured with $V_{In} = V_{SS}$.

4 Measured with $V_{In} = V_{DD}$.

5 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

6 Input must be current-limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

8 Maximum is highest voltage that POR is guaranteed.

9 Factory trimmed at V_{DD} = 5.0 V, Temp = 25 °C.

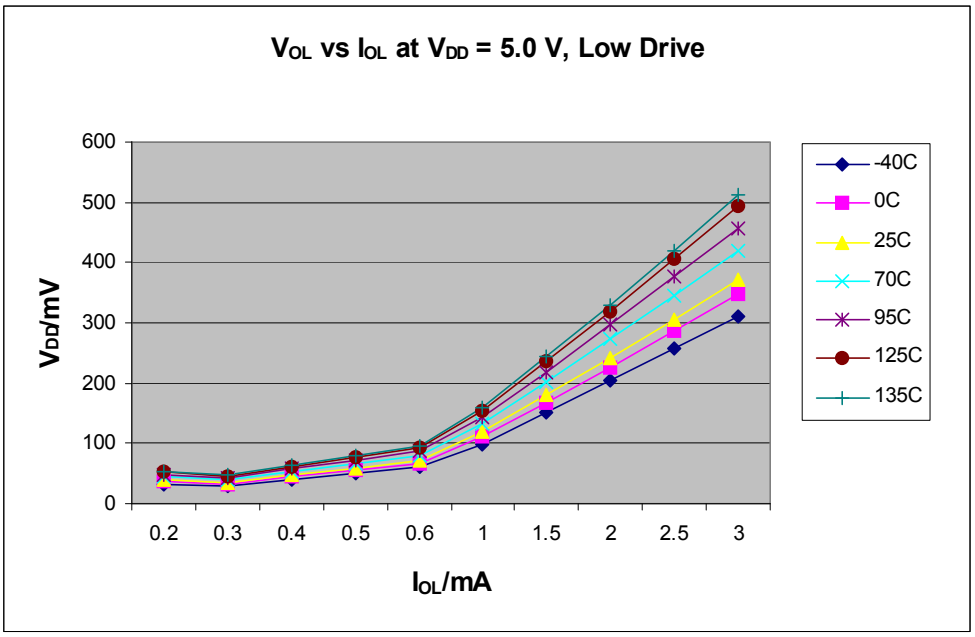


Figure 6. Typical V_{OL} vs. I_{OL} for Low Drive Enabled Pad (V_{DD} = 5 V)

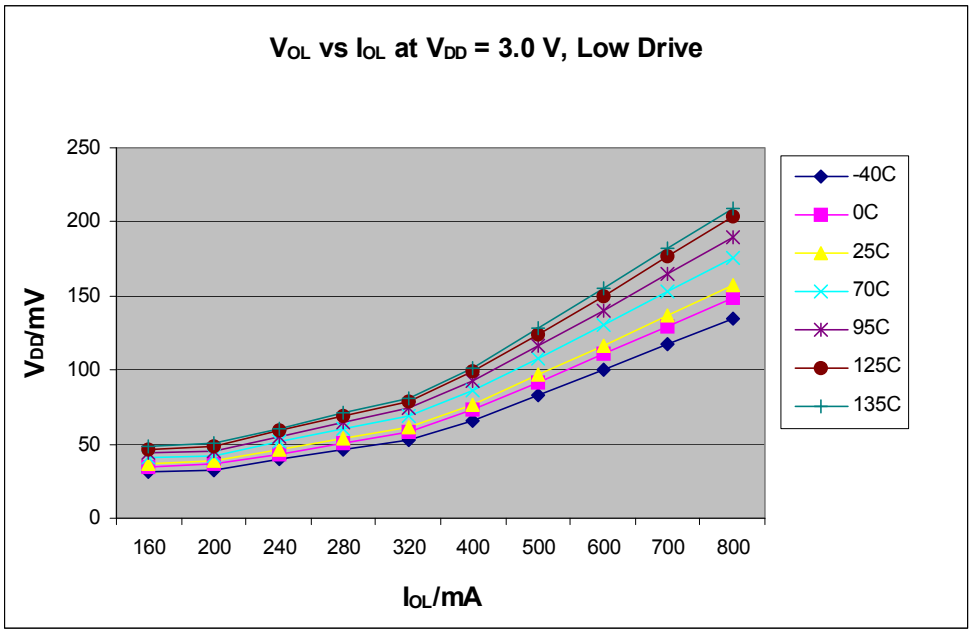


Figure 7. Typical V_{OL} vs. I_{OL} for Low Drive Enabled Pad (V_{DD} = 3 V)

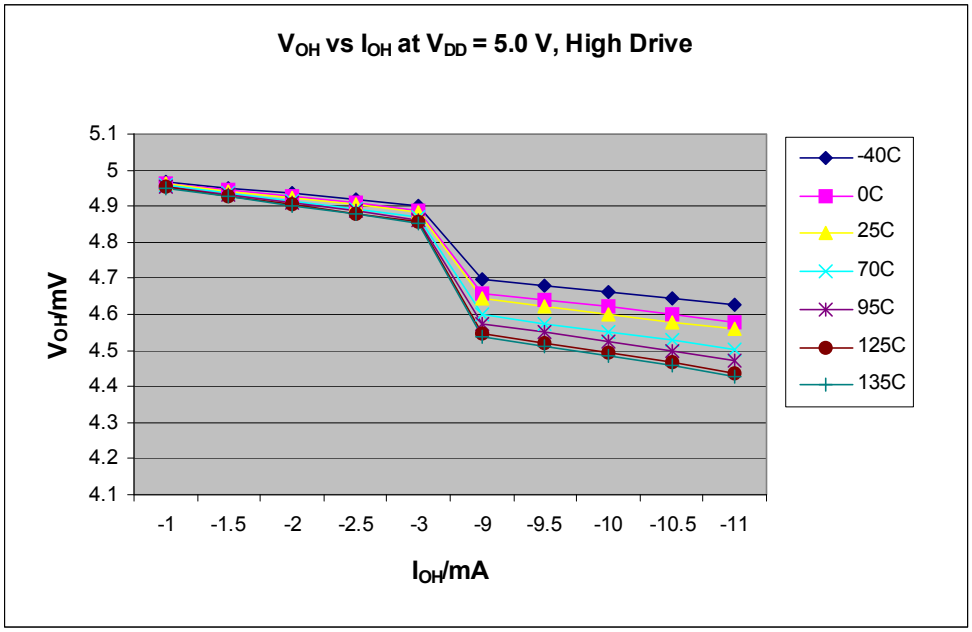


Figure 8. Typical V_{OH} vs. I_{OH} for High Drive Enabled Pad (V_{DD} = 5 V)

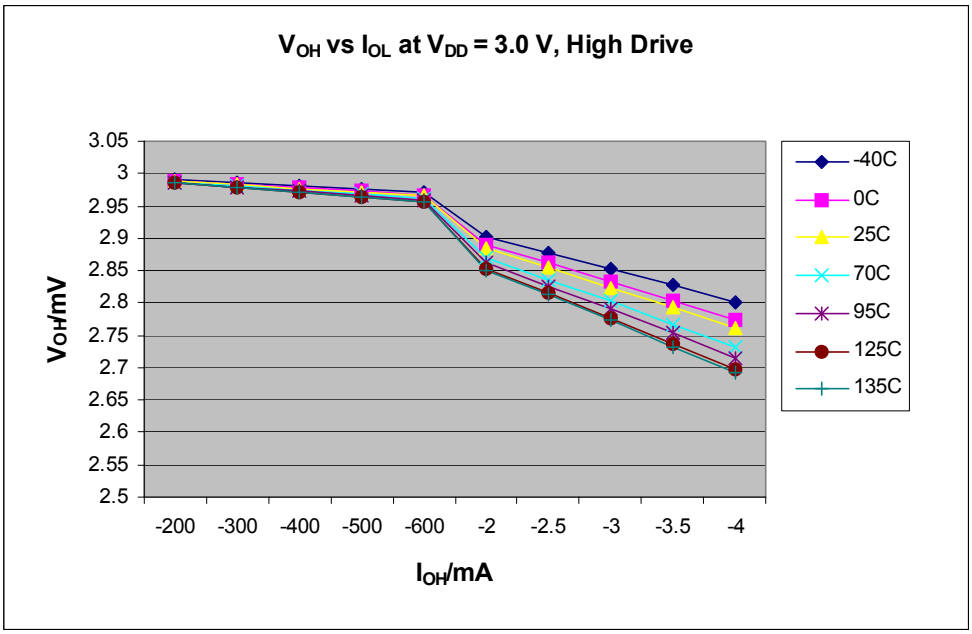


Figure 9. Typical V_{OH} vs. I_{OH} for High Drive Enabled Pad (V_{DD} = 3 V)

Table 8. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max	Unit	Temp (°C)
1	C	Run supply current[2] measured at (CPU clock = 4 MHz, f_{Bus} = 2 MHz)	RI_{DD}	5	2.4	2.72	mA	–40 to 125
				3	2.18	2.26		
2	P	Run supply current[2] measured at (CPU clock = 20 MHz, f_{Bus} = 10 MHz)	RI_{DD}	5	6.35	7.29	mA	–40 to 125
				3	5.79	6.42		
3	P	Wait supply current[2] measured at f_{Bus} = 2 MHz	WI_{DD}	5	1.4	1.56	mA	–40 to 125
				3	1.36	1.53		
4	P	Stop2 mode supply current	$S2I_{DD}$	5	1.4	19 28 45.8	µA	–40 to 85 –40 to 105 –40 to 125
				3	1.3	15 22 37.2	µA	–40 to 85 –40 to 105 –40 to 125
5	P	Stop3 mode supply current	$S3I_{DD}$	5	1.61	23 43 76.1	µA	–40 to 85 –40 to 105 –40 to 125
				3	1.44	19 38 66.4	µA	–40 to 85 –40 to 105 –40 to 125
6	P	RTC adder to stop2 or stop3[3]	$S23I_{DDRTI}$	5	300	500 500	nA	–40 to 85 –40 to 125
				3	300	500 500	nA	–40 to 85 –40 to 125
7	C	LVD adder to stop3 (LVDE = LVDSE = 1)	$S3I_{DDLVD}$	5	122	180	µA	–40 to 125
				3	110	160	µA	–40 to 125
8	C	Adder to stop3 for oscillator enabled[4] (OSCSTEN =1)	$S3I_{DDOSC}$	5,3	5	8	µA	–40 to 125

1 Typical values are based on characterization data at 25 °C unless otherwise stated. See Figure 12 through Figure 13 for typical curves across voltage/temperature.

2 All modules except ADC active, ICS configured for FBE, and does not include any dc loads on port pins.

3 Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode. Wait mode typical is 220 µA at 5 V with f_{Bus} = 1 MHz.

4 Values given under the following conditions: low range operation (RANGE = 0) with a 32.768 kHz crystal and low power mode (HGO = 0).

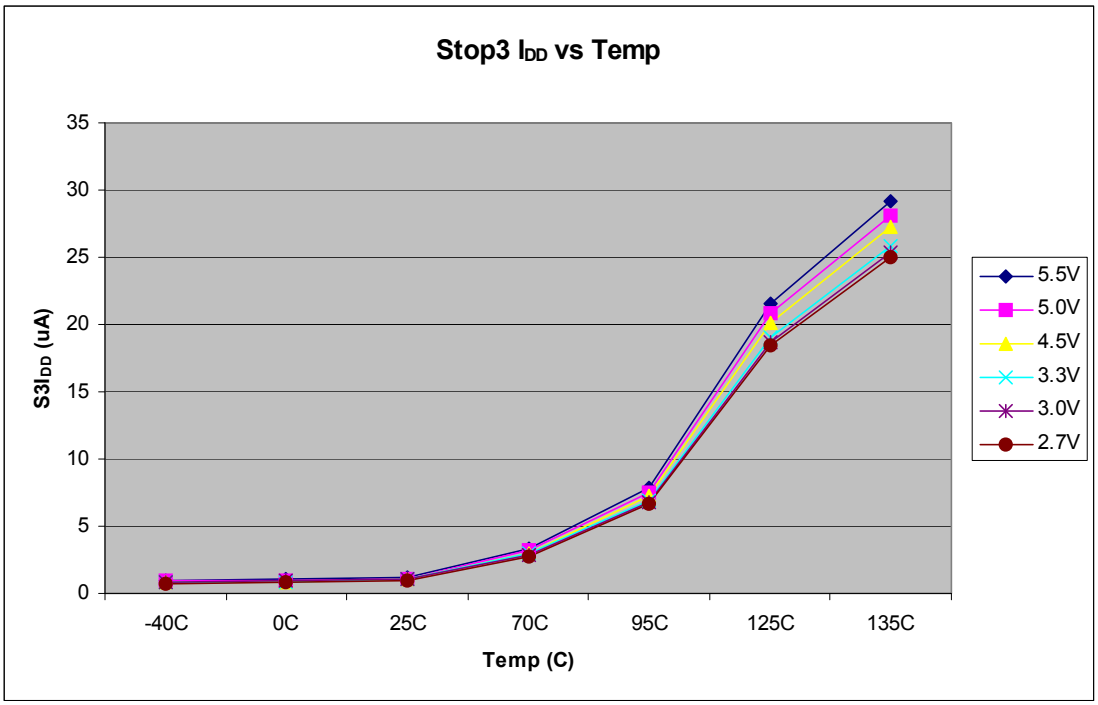


Figure 14. Typical Stop3 I_{DD} Curves

3.7 External Oscillator (XOSC) Characteristics

Table 9. Oscillator electrical specifications (Temperature Range = –40 to 125°C Ambient)

Num	C	Characteristic	Symbol	Min.	Typical[1]	Max.	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1)[2] High range (RANGE = 1), low power (HGO = 0)[2]	 f_{lo} f_{hi-hgo} f_{hi-lp}	 32 1 1	 — — —	 38.4 16 8	 kHz MHz MHz
2	—	Load capacitors	C_1,C_2	See crystal or resonator manufacturer's recommendation			
3	—	Feedback resistor Low range (32 kHz to 100 kHz) High range (1 MHz to 16 MHz)	R_F	 — —	 10 1	 — —	MΩ
4	—	Series resistor Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0)	R_S	 — — —	 0 100 0	 — — —	kΩ
		High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz		 — — —	 0 0 0	 0 10 20	

Table 9. Oscillator electrical specifications (Temperature Range = –40 to 125°C Ambient)

Num	C	Characteristic	Symbol	Min.	Typical[1]	Max.	Unit
5	T	Crystal start-up time[3] Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0)[4] High range, high gain (RANGE = 1, HGO = 1)[4]	 $t_{CSTL-LP}$ $t_{CSTH-HGO}$ $t_{CSTH-LP}$ $t_{CSTH-HGO}$	 — — — —	 200 400 5 15	 — — — —	ms
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE or FBE mode [2] FBELP mode	f_{extal}	0.03125 0	— —	20 20	MHz MHz

1 Typical column was characterized at 5.0 V, 25 °C or is recommended value.

2 The input clock source must be divided using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications. This data will vary based upon the crystal manufacturer and board design. The crystal should be characterized by the crystal manufacturer.

4 4 MHz crystal.

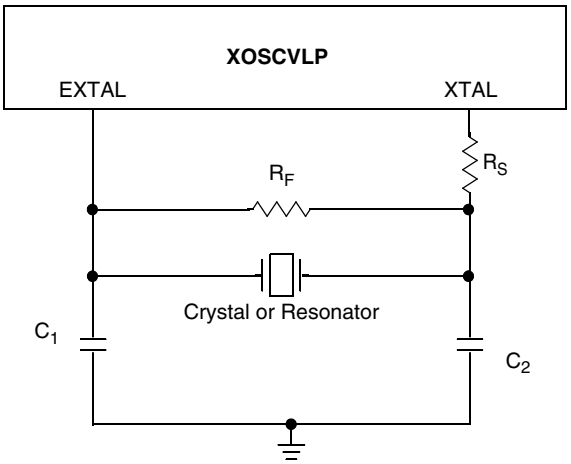


Figure 15. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

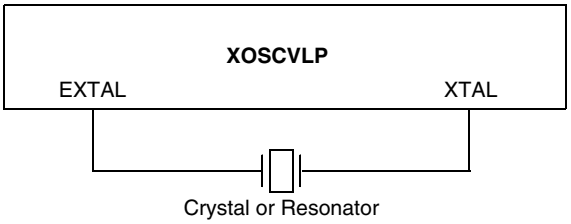


Figure 16. Typical Crystal or Resonator Circuit: Low Range/Low Power

3.8 Internal Clock Source (ICS) Characteristics

Table 10. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic		Symbol	Min.	Typical[1]	Max.	Unit
1	P	Average internal reference frequency — factory trimmed at V_{DD} = 5 V and temperature = 25 °C		f_{int_t}	—	39.0625	—	kHz
2	P	Internal reference frequency — user trimmed		f_{int_ut}	31.25	—	39.06	kHz
3	T	Internal reference start-up time		t_{IRST}	—	60	100	µs
4	D	DCO output frequency range — trimmed[2]	Low range (DRS = 00)	f_{dco_t}	16	—	20	MHz
5	D	DCO output frequency[2] Reference = 32768 Hz and DMX32 = 1		f_{dco_DMX32}	—	59.77	—	MHz
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	$\%f_{dco}$
8	C	Total deviation of DCO output from trimmed frequency[3] Over full voltage and temperature range Over fixed voltage and temperature range of 0 to 70 °C		Δf_{dco_t}	—	–1.0 to 0.5 ±0.5	± 2 ± 1	$\%f_{dco}$
10	C	FLL acquisition time[4]		$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval)[5]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This parameter is characterized and not tested on each device.

4 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

5 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

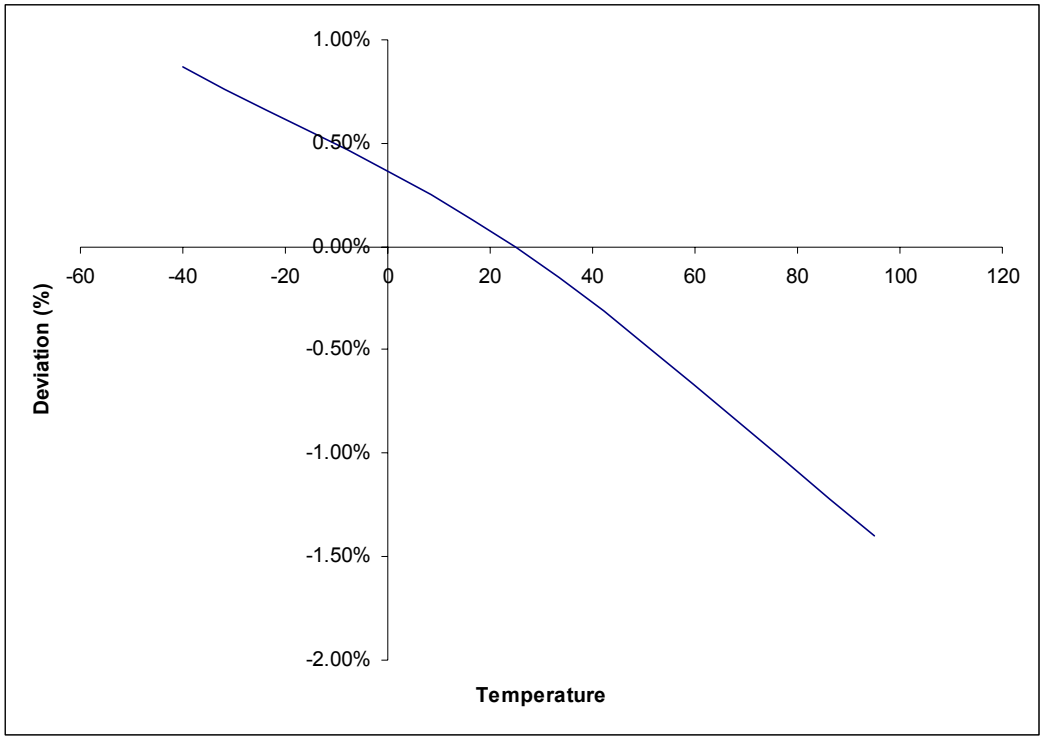


Figure 17. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

3.9 ADC Characteristics

Table 11. 10-Bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	
	Delta to V_{DD} ($V_{DD} - V_{DDA}$)[2]	ΔV_{DDA}	–100	0	100	mV	
Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)[2]	ΔV_{SSA}	–100	0	100	mV	
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	3	5	kΩ	
Analog source resistance	10-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 5 10	kΩ	External to MCU
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock frequency	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low power (ADLPC = 1)		0.4	—	4.0		

1 Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

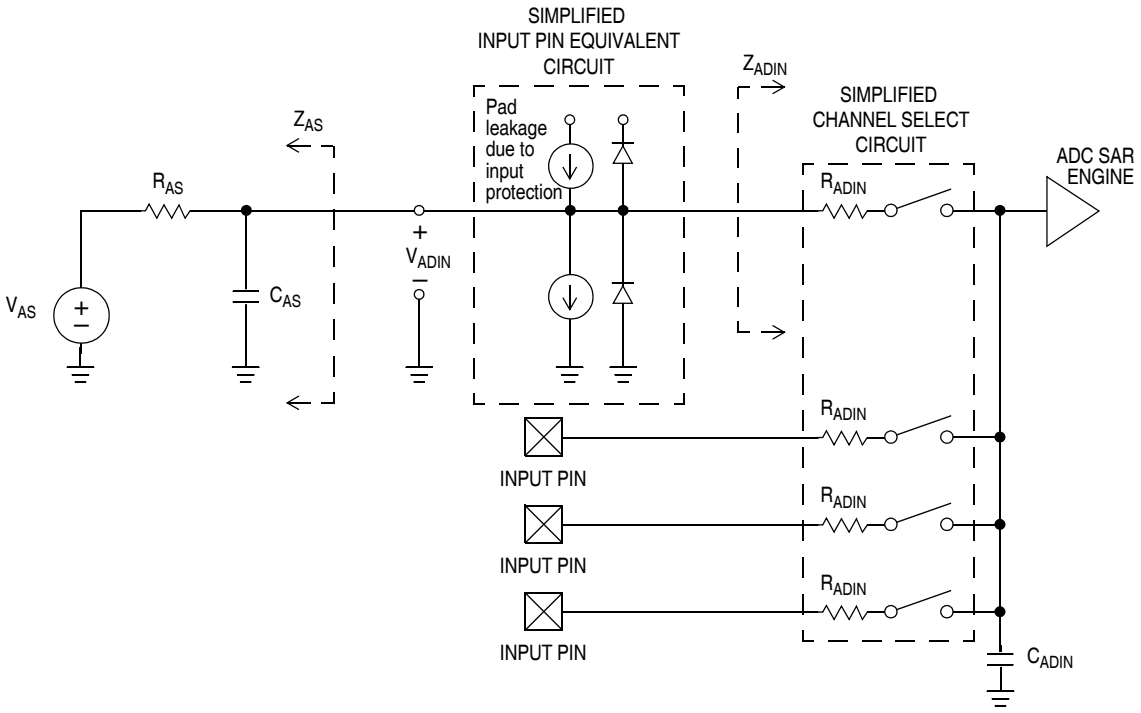


Figure 18. ADC Input Impedance Equivalency Diagram

Table 12. 10-Bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	133	—	µA	
Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	218	—	µA	
Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	327	—	µA	
Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1		D	I_{DDA}	—	0.582	1	mA	
Supply Current	Stop, Reset, Module Off	D	I_{DDA}	—	0.011	1	µA	

Table 12. 10-Bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

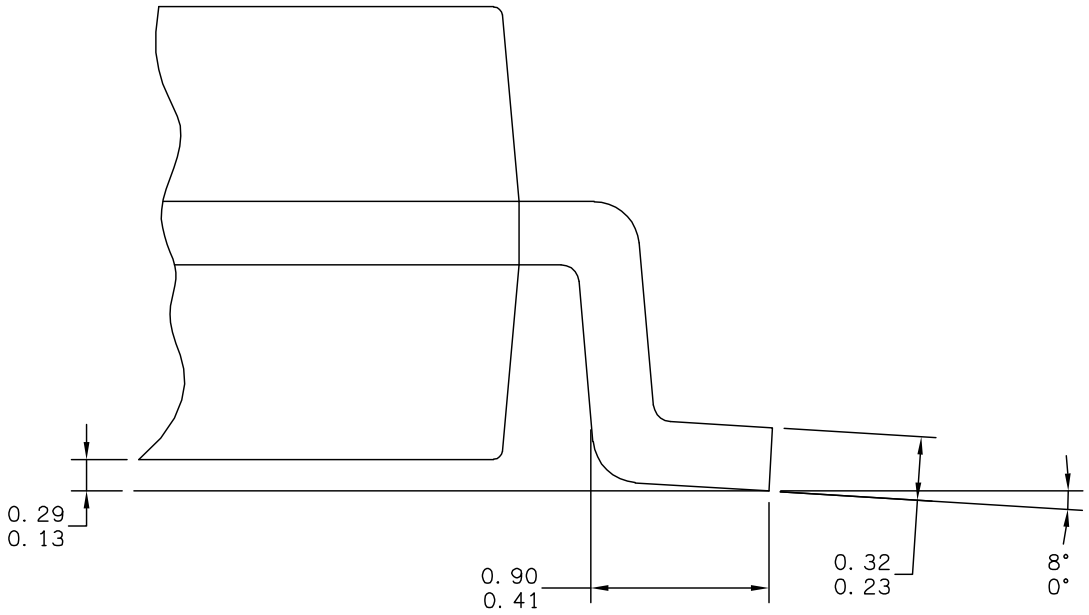
Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
Differential Non-Linearity	10-bit mode[3]	P	DNL	—	±0.5	±1.0	LSB[3]	
	8-bit mode[3]	P		—	±0.3	±0.5		
Integral Non-Linearity	10-bit mode	T	INL	—	±0.5	±1.0	LSB[3]	
	8-bit mode	T		—	±0.3	±0.5		
Zero-Scale Error	10-bit mode	P	E_{ZS}	—	±1.5	±2.1	LSB[3]	V_{ADIN} = V_{SSA}
	8-bit mode	P		—	±0.5	±0.7		
Full-Scale Error	10-bit mode	T	E_{FS}	—	±1	±1.5	LSB[3]	V_{ADIN} = V_{DDA}
	8-bit mode	T		—	±0.5	±0.5		
Quantization Error	10-bit mode	D	E_Q	—	—	±0.5	LSB[3]	
	8-bit mode			—	—	±0.5		
Input Leakage Error	10-bit mode	D	E_{IL}	—	±0.2	±2.5	LSB[3]	Pad leakage[4] * R_{AS}
	8-bit mode			—	±0.1	±1		

1 Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 Monotonicity and No-Missing-Codes guaranteed in 10-bit and 8-bit modes

3 1 LSB =(V_{REFH} – V_{REFL})/2^N

4 Based on input pad leakage current. Refer to pad electricals.



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TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE	DOCUMENT NO: 98ASB42345B	REV: G
	CASE NUMBER: 751F-05	10 MAR 2005
	STANDARD: MS-013AE	

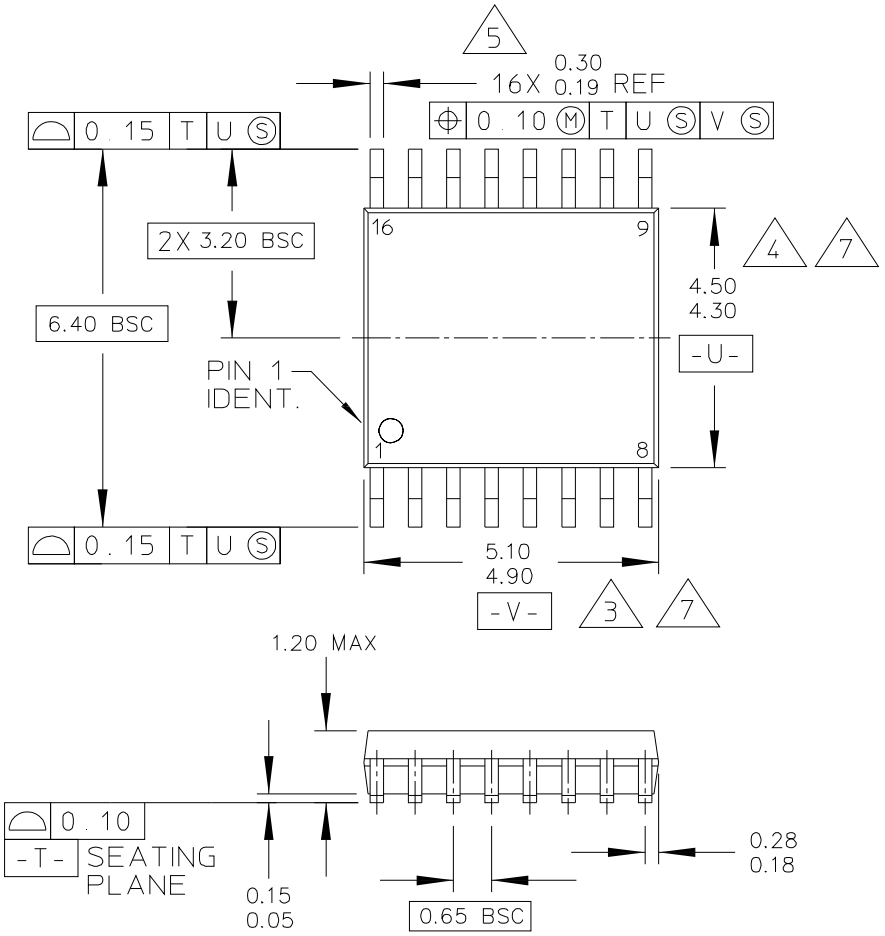
NOTES:

1. POSITIONAL TOLERANCE OF LEADS, SHALL BE WITHIN 0.25 MM (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH.
4. 710-01 OBSOLETE, NEW STD 710-02.
5. CONTROLLING DIMENSION: INCH

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21					
B	0.540	0.560	13.72	14.22					
C	0.155	0.200	3.94	5.08					
D	0.014	0.022	0.36	0.56					
F	0.040	0.060	1.02	1.52					
G	0.100 BSC		2.54 BSC						
H	0.065	0.085	1.65	2.16					
J	0.008	0.015	0.20	0.38					
K	0.115	0.135	2.92	3.43					
L	0.600 BSC		15.24 BSC						
M	0°	15°	0°	15°					
N	0.020	0.040	0.51	1.02					

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42390B	REV: D
28 LD PDIP	CASE NUMBER: 710-02	24 MAY 2005
	STANDARD: NON-JEDEC	



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TITLE: 16 LD TSSOP, PITCH 0.65MM	DOCUMENT NO: 98ASH70247A	REV: B
	CASE NUMBER: 948F-01	19 MAY 2005
	STANDARD: JEDEC	

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