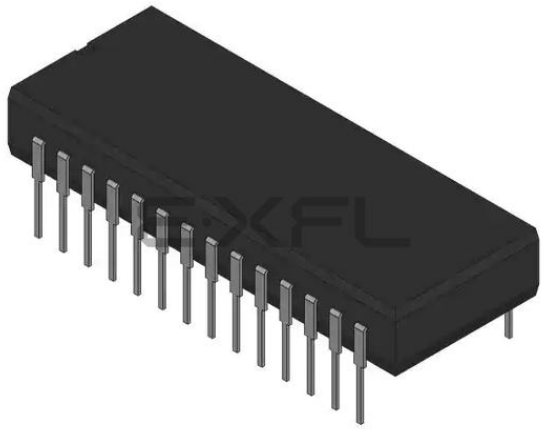

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	LINbus, SCI
Peripherals	LVD, POR, PWM
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-PDIP
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08se8vrl

Table of Contents

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to: freescale.com

The following revision history table summarizes changes contained in this document.

Revision	Date	Description of Changes
1	10/8/2008	Initial public released.
2	1/16/2009	In Table 8, added the Max. of $S2I_{DD}$ and $S3I_{DD}$ in 0–105 °C; changed the Max. of $S2I_{DD}$ and $S3I_{DD}$ in 0–85 °C; changed the typical of $S2I_{DD}$ and $S3I_{DD}$; changed the $S23I_{DDRTI}$ to P.
3	4/7/2009	Added $\lvert I_{OZTOT}\rvert$ in the Table 7. Changed V_{DDAD} to V_{DDA}, V_{SSAD} to V_{SSA}. Updated Table 9, Table 10, Table 11, and Table 12. Updated Figure 13 and Figure 14.
4	4/10/2015	Updated Table 9.

Related Documentation

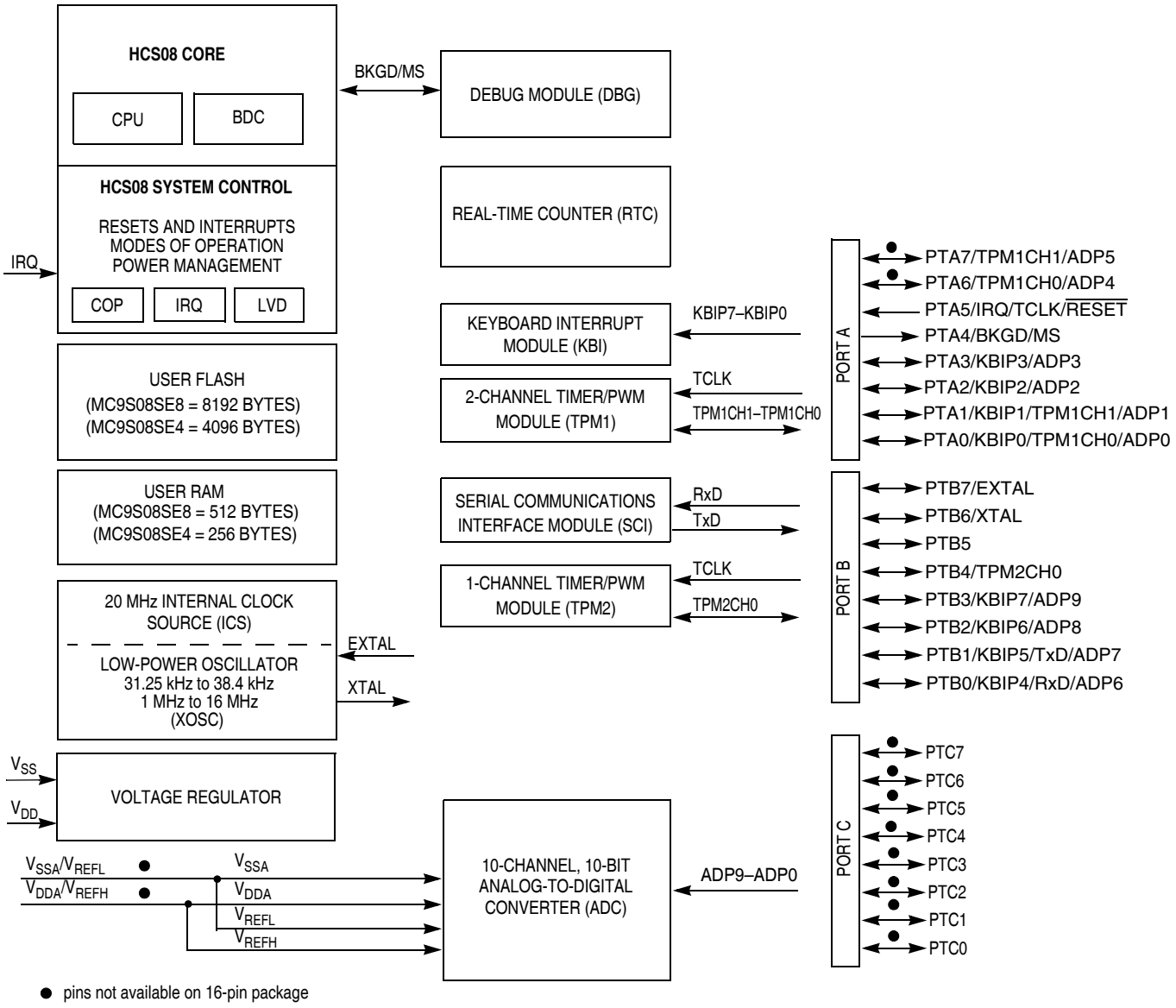
Find the most current versions of all documents at: http://www.freescale.com

Reference Manual (MC9S08SE8RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 MCU Block Diagram

The block diagram, Figure 1, shows the structure of the MC9S08SE8 series MCUs.



● pins not available on 16-pin package

Notes:

When PTA4 is configured as BKGD, pin is bi-directional.

For the 16-pin package: V_{SSA}/V_{REFL} and V_{DDA}/V_{REFH} are double bonded to V_{SS} and V_{DD} respectively.

Figure 1. MC9S08SE8 Series Block Diagram

2 Pin Assignments

This chapter shows the pin assignments in the packages available for the MC9S08SE8 series.

Table 1. Pin Availability by Package Pin-Count

Pin Number (Package)		<-- Lowest **Priority** --> Highest			
28 (SOIC/PDIP)	**16 (TSSOP)**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**
1	—	PTC5			
2	—	PTC4			
3	1	PTA5	IRQ	TCLK	$\overline{\text{RESET}}$
4	2	PTA4		BKGD	MS
5	3				V_{DD}
6	—			V_{DDA}	V_{REFH}
7	—			V_{SSA}	V_{REFL}
8	4				V_{SS}
9	5	PTB7	EXTAL		
10	6	PTB6	XTAL		
11	7	PTB5			
12	8	PTB4		TPM2CH0	
13	—	PTC3			
14	—	PTC2			
15	—	PTC1			
16	—	PTC0			
17	9	PTB3	KBIP7		ADP9
18	10	PTB2	KBIP6		ADP8
19	11	PTB1	KBIP5	TxD	ADP7
20	12	PTB0	KBIP4	RxD	ADP6
21	—	PTA7		TPM1CH1[1]	ADP5
22	—	PTA6		TPM1CH0[1]	ADP4
23	13	PTA3	KBIP3		ADP3
24	14	PTA2	KBIP2		ADP2
25	15	PTA1	KBIP1	TPM1CH1[1]	ADP1
26	16	PTA0	KBIP0	TPM1CH0[1]	ADP0
27	—	PTC7			
28	—	PTC6			

[1] TPM1 pins can be remapped to PTA7, PTA6 and PTA1,PTA0

3 Electrical Characteristics

This chapter contains electrical and timing specifications.

3.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 5. ESD and Latch-up Test Conditions (continued)

Model	Description	Symbol	Value	Unit
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 6. ESD and Latch-up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Machine model (MM)	V_{MM}	±200	—	V
3	Charge device model (CDM)	V_{CDM}	±500	—	V
4	Latch-up current at T_A = 125 °C	I_{LAT}	±100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.5 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 7. DC Characteristics

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
1	—	Operating voltage	—	2.7	—	5.5	V
2	P	Output high voltage — Low drive (PTxDSn = 0) 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –0.6 mA 5 V, I_{Load} = –0.4 mA 3 V, I_{Load} = –0.24 mA	V_{OH}	 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	V
		Output high voltage — High drive (PTxDSn = 1) 5 V, I_{Load} = –10 mA 3 V, I_{Load} = –3 mA 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –0.4 mA		 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	
3	P	Output low voltage — Low drive (PTxDSn = 0) 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 0.6 mA 5 V, I_{Load} = 0.4 mA 3 V, I_{Load} = 0.24 mA	V_{OL}	 1.5 1.5 0.8 0.8	 — — — —	 — — — —	V
		Output low voltage — High drive (PTxDSn = 1) 5 V, I_{Load} = 10 mA 3 V, I_{Load} = 3 mA 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 0.4 mA		 1.5 1.5 0.8 0.8	 — — — —	 — — — —	
4	P	Output high current — Max total I_{OH} for all ports 5 V 3 V	I_{OHT}	 — —	 — —	 100 60	mA

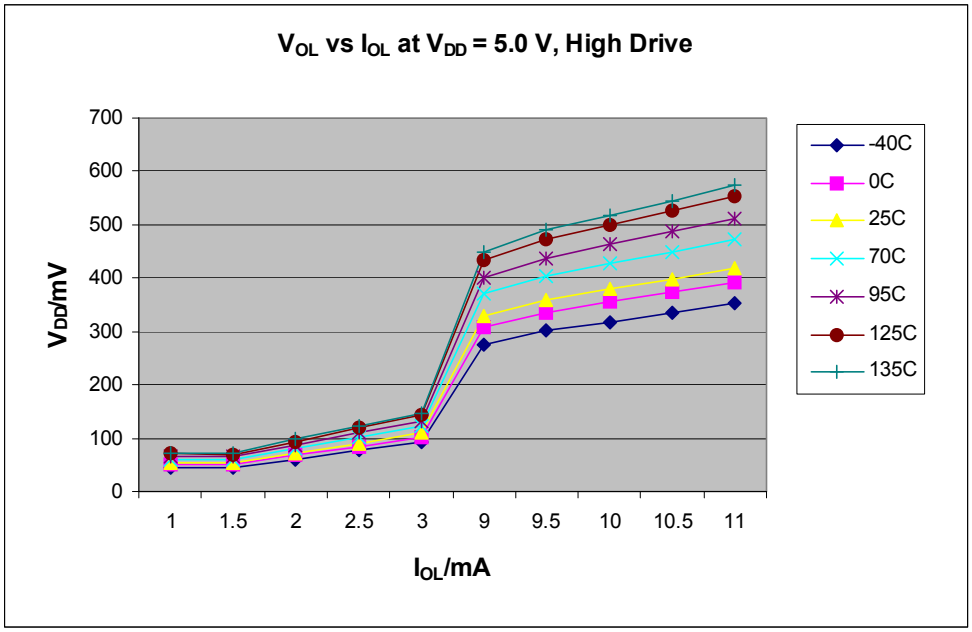


Figure 4. Typical V_{OL} vs. I_{OL} for High Drive Enabled Pad (V_{DD} = 5 V)

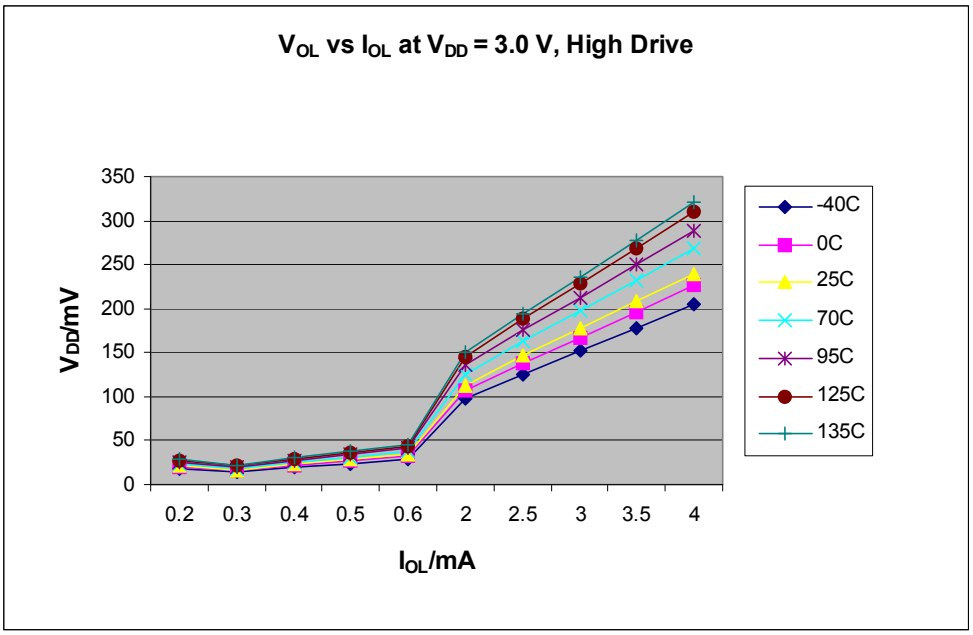


Figure 5. Typical V_{OL} vs. I_{OL} for High Drive Enabled Pad (V_{DD} = 3 V)

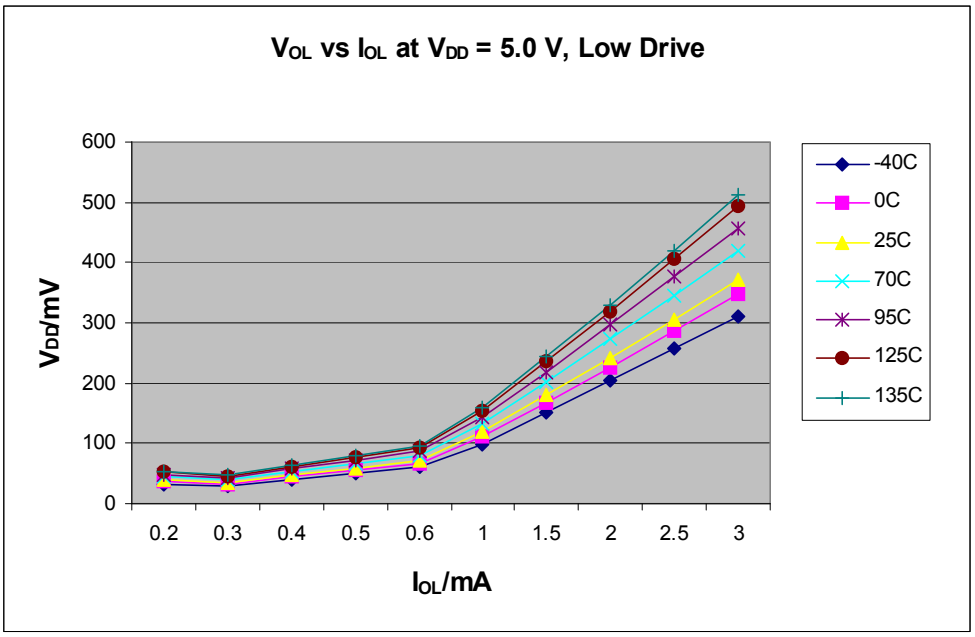


Figure 6. Typical V_{OL} vs. I_{OL} for Low Drive Enabled Pad (V_{DD} = 5 V)

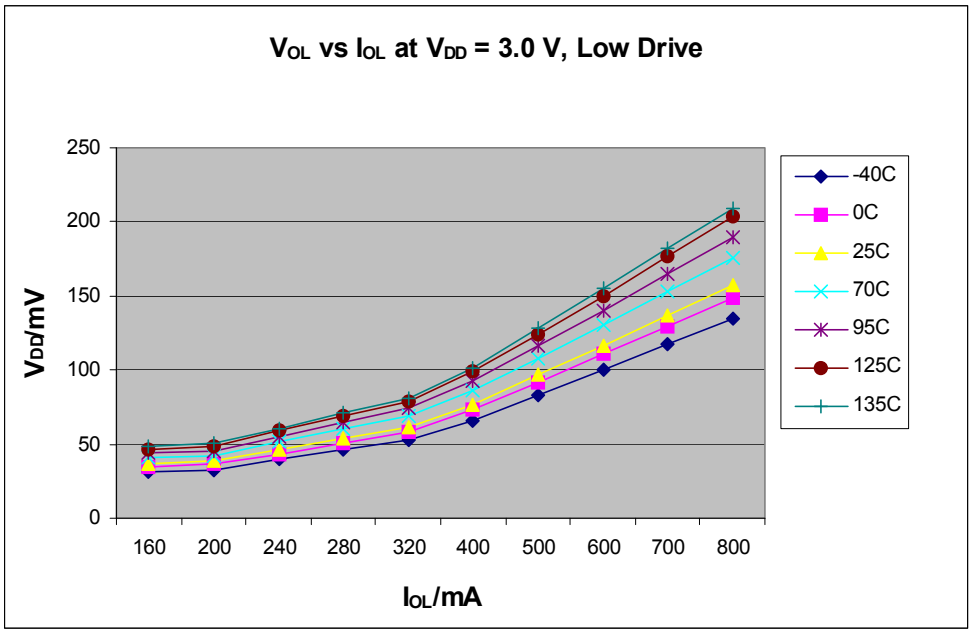


Figure 7. Typical V_{OL} vs. I_{OL} for Low Drive Enabled Pad (V_{DD} = 3 V)

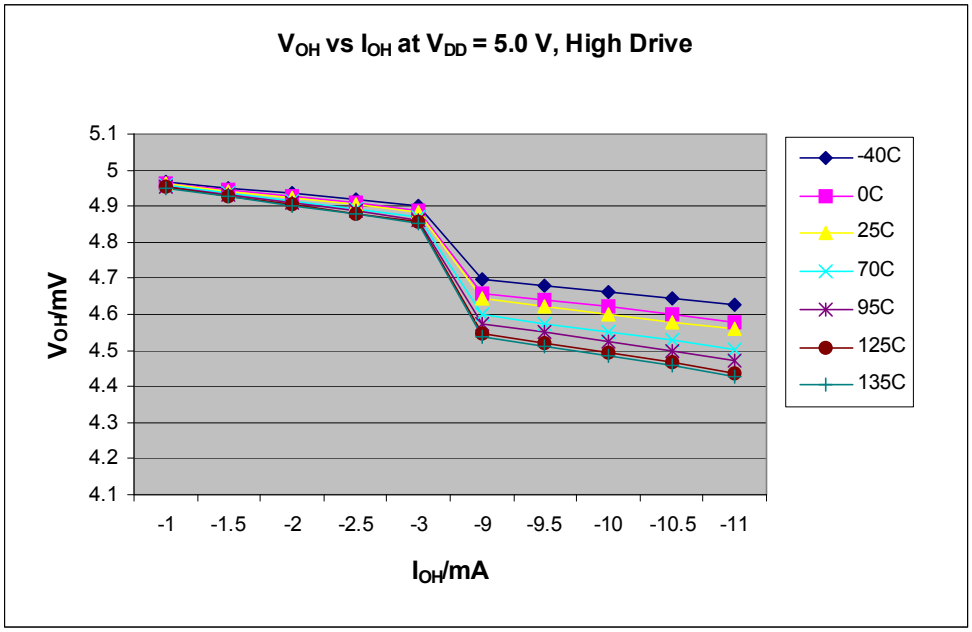


Figure 8. Typical V_{OH} vs. I_{OH} for High Drive Enabled Pad (V_{DD} = 5 V)

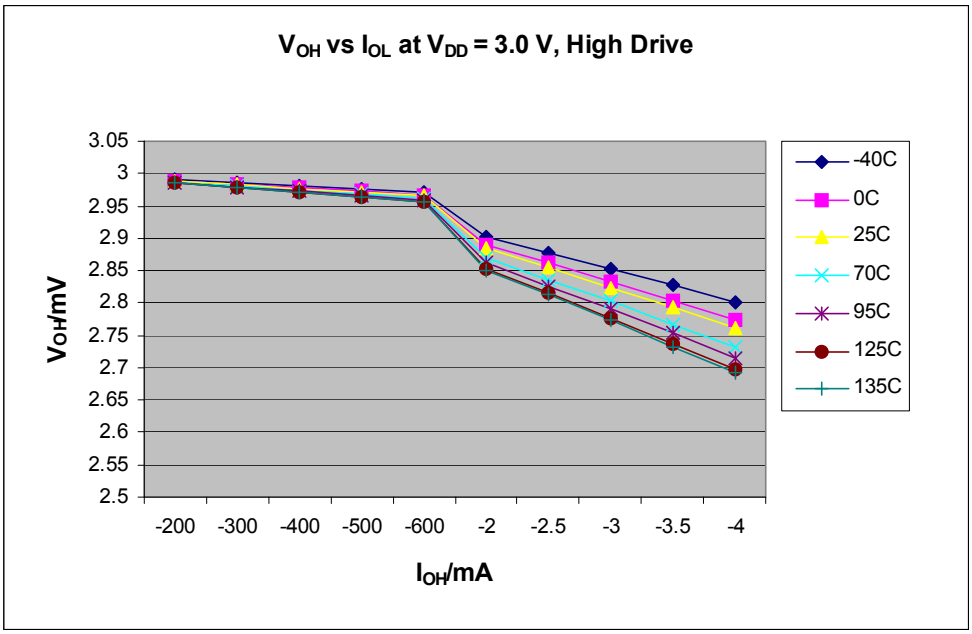


Figure 9. Typical V_{OH} vs. I_{OH} for High Drive Enabled Pad (V_{DD} = 3 V)

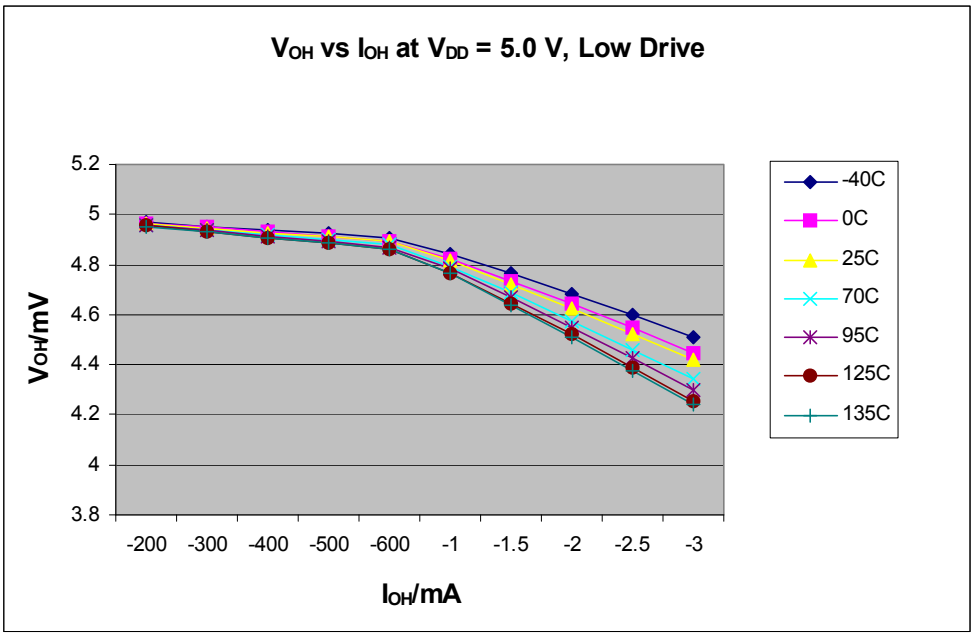


Figure 10. Typical V_{OH} vs. I_{OH} for Low Drive Enabled Pad (V_{DD} = 5 V)

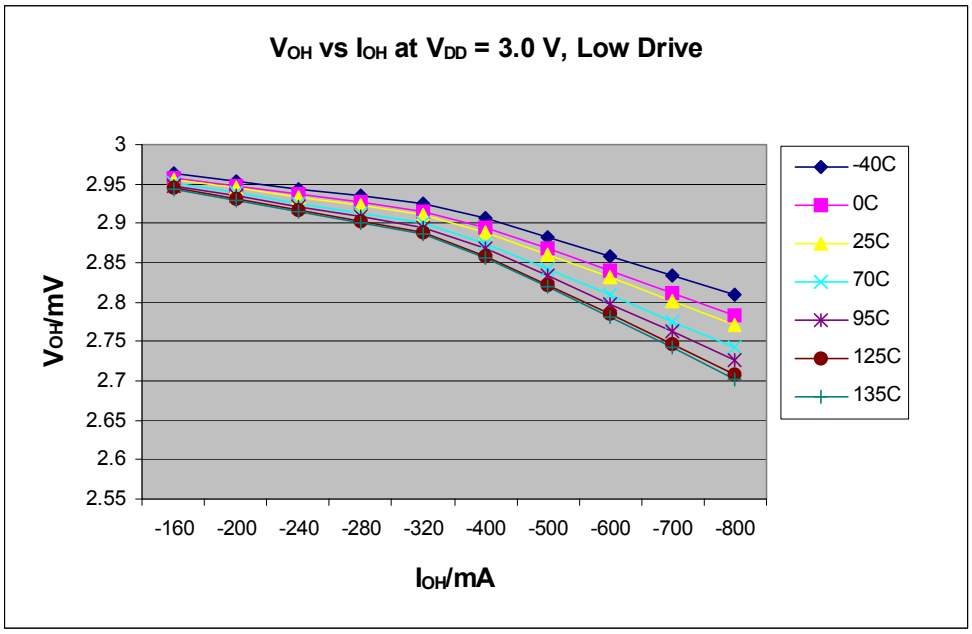


Figure 11. Typical V_{OH} vs. I_{OH} for Low Drive Enabled Pad (V_{DD} = 3 V)

3.6 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

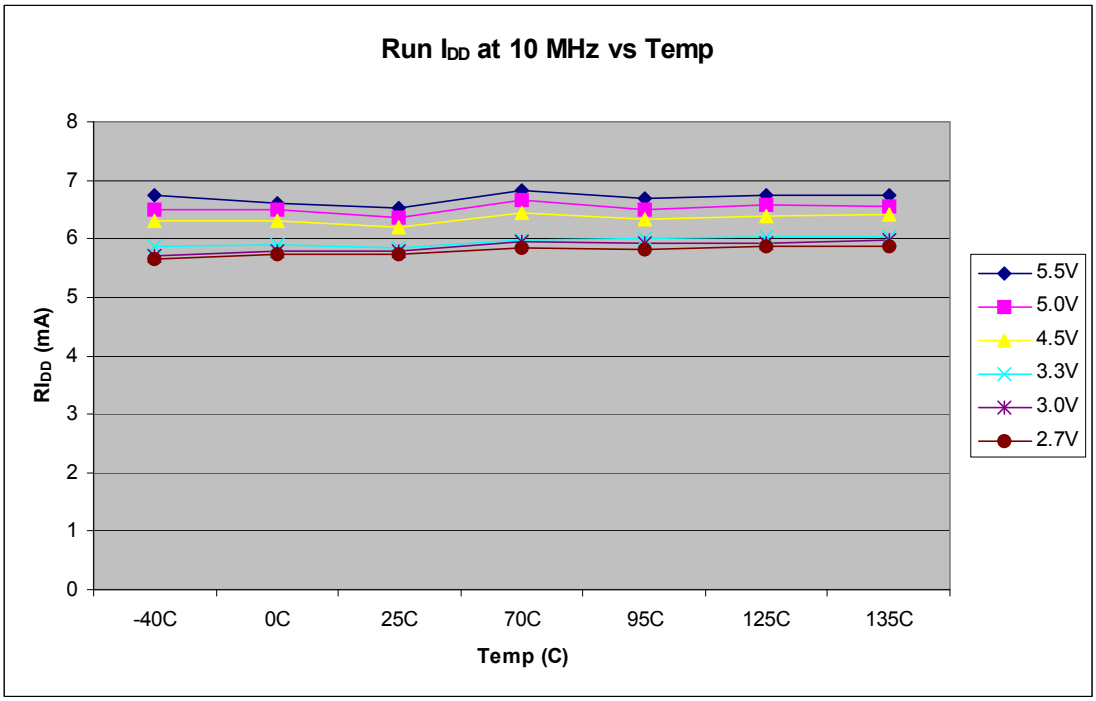


Figure 12. Typical Run I_{DD} Curves

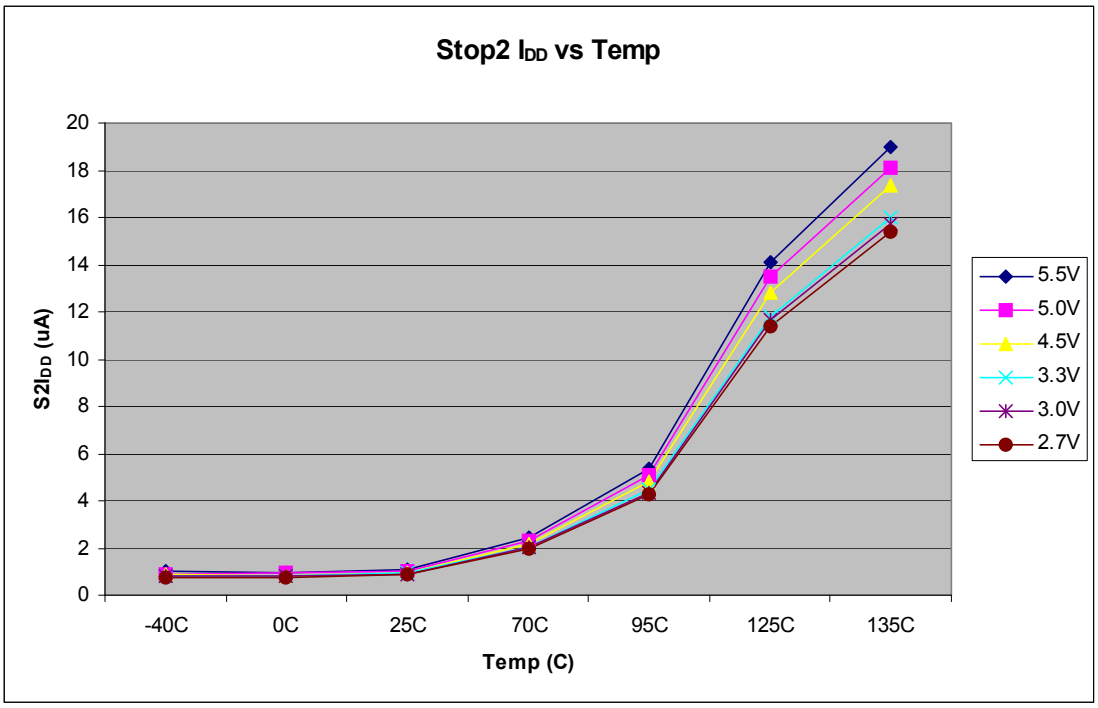


Figure 13. Typical Stop2 I_{DD} Curves

Table 9. Oscillator electrical specifications (Temperature Range = –40 to 125°C Ambient)

Num	C	Characteristic	Symbol	Min.	Typical[1]	Max.	Unit
5	T	Crystal start-up time[3] Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0)[4] High range, high gain (RANGE = 1, HGO = 1)[4]	 $t_{CSTL-LP}$ $t_{CSTH-HGO}$ $t_{CSTH-LP}$ $t_{CSTH-HGO}$	 — — — —	 200 400 5 15	 — — — —	ms
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE or FBE mode [2] FBELP mode	f_{extal}	0.03125 0	— —	20 20	MHz MHz

1 Typical column was characterized at 5.0 V, 25 °C or is recommended value.

2 The input clock source must be divided using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications. This data will vary based upon the crystal manufacturer and board design. The crystal should be characterized by the crystal manufacturer.

4 4 MHz crystal.

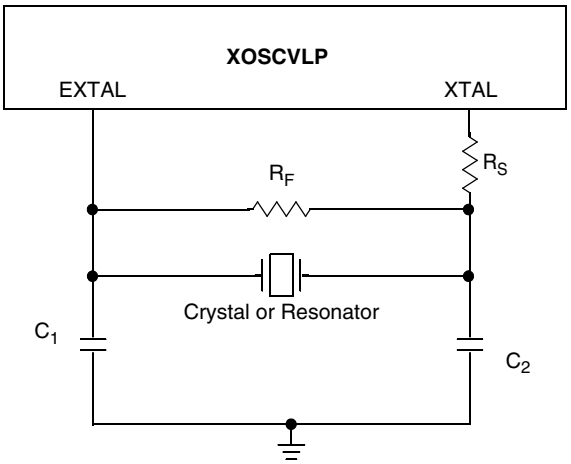


Figure 15. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

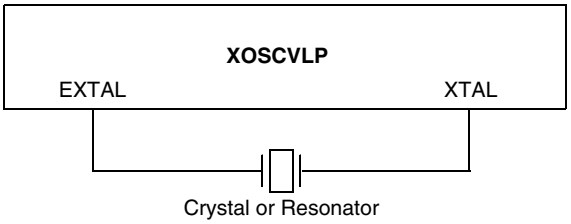


Figure 16. Typical Crystal or Resonator Circuit: Low Range/Low Power

3.8 Internal Clock Source (ICS) Characteristics

Table 10. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic		Symbol	Min.	Typical[1]	Max.	Unit
1	P	Average internal reference frequency — factory trimmed at V_{DD} = 5 V and temperature = 25 °C		f_{int_t}	—	39.0625	—	kHz
2	P	Internal reference frequency — user trimmed		f_{int_ut}	31.25	—	39.06	kHz
3	T	Internal reference start-up time		t_{IRST}	—	60	100	µs
4	D	DCO output frequency range — trimmed[2]	Low range (DRS = 00)	f_{dco_t}	16	—	20	MHz
5	D	DCO output frequency[2] Reference = 32768 Hz and DMX32 = 1		f_{dco_DMX32}	—	59.77	—	MHz
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	$\%f_{dco}$
8	C	Total deviation of DCO output from trimmed frequency[3] Over full voltage and temperature range Over fixed voltage and temperature range of 0 to 70 °C		Δf_{dco_t}	—	–1.0 to 0.5 ±0.5	± 2 ± 1	$\%f_{dco}$
10	C	FLL acquisition time[4]		$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval)[5]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This parameter is characterized and not tested on each device.

4 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

5 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

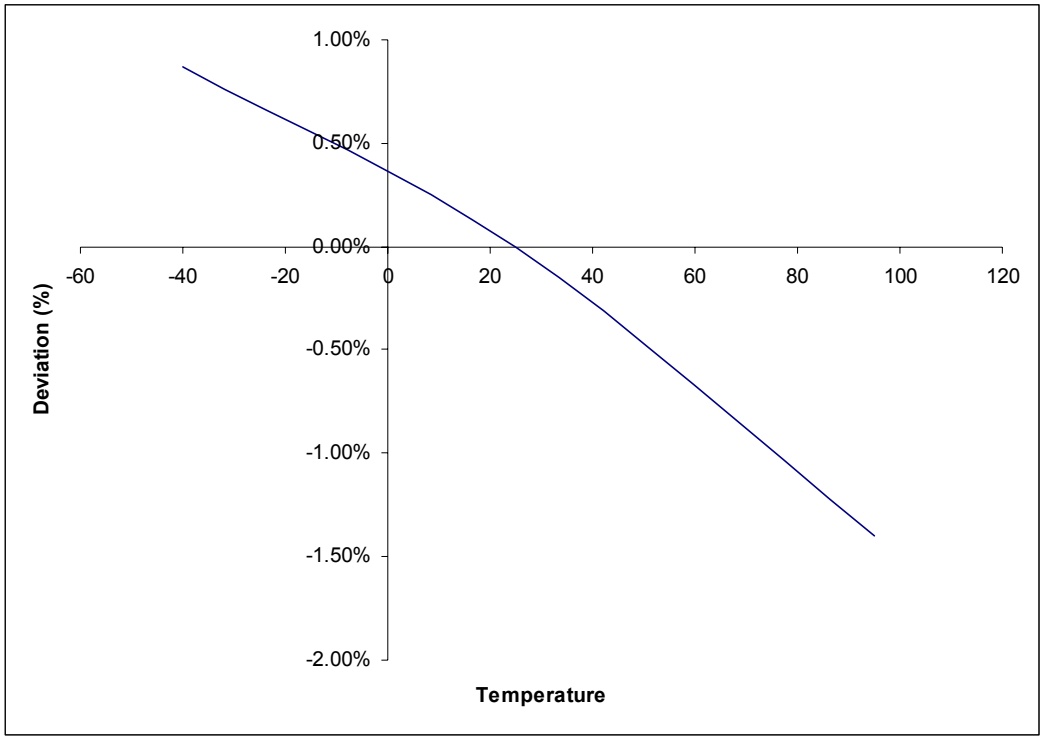


Figure 17. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

3.9 ADC Characteristics

Table 11. 10-Bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	
	Delta to V_{DD} ($V_{DD} - V_{DDA}$)[2]	ΔV_{DDA}	–100	0	100	mV	
Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)[2]	ΔV_{SSA}	–100	0	100	mV	
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	3	5	kΩ	
Analog source resistance	10-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 5 10	kΩ	External to MCU
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock frequency	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low power (ADLPC = 1)		0.4	—	4.0		

1 Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

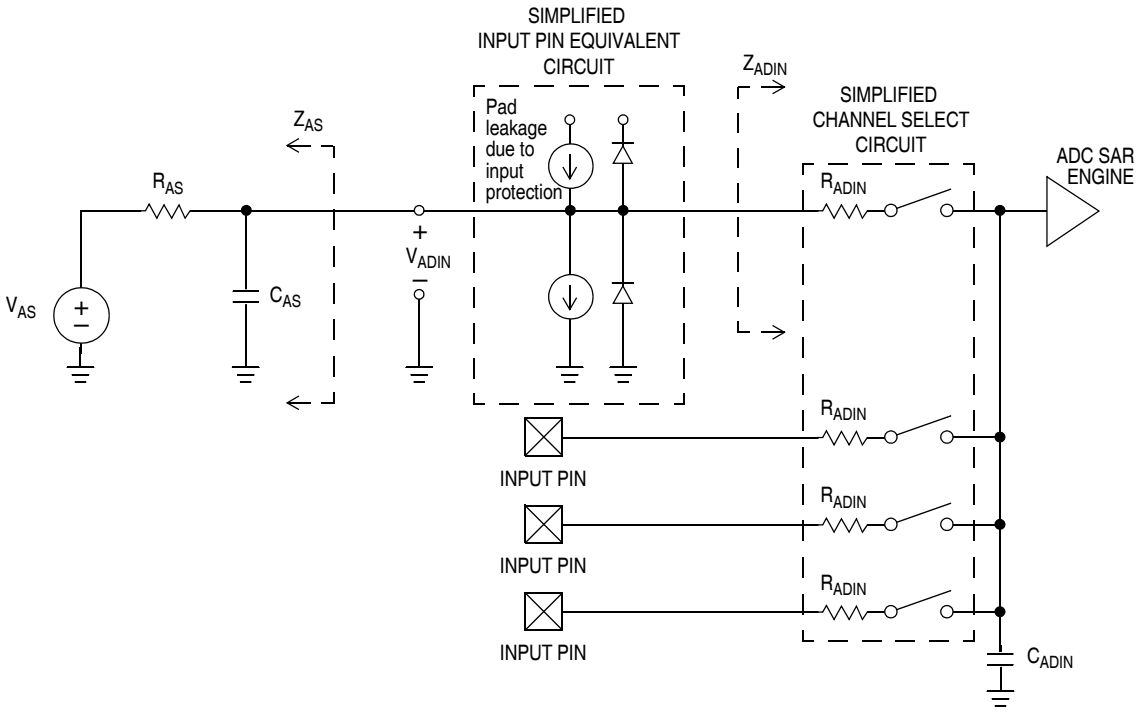


Figure 18. ADC Input Impedance Equivalency Diagram

Table 12. 10-Bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	133	—	µA	
Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	218	—	µA	
Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	327	—	µA	
Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1		D	I_{DDA}	—	0.582	1	mA	
Supply Current	Stop, Reset, Module Off	D	I_{DDA}	—	0.011	1	µA	

Table 12. 10-Bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	D	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
	Low Power (ADLPC = 1)			1.25	2	3.3		
Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	D	t_{ADC}	—	20	—	ADCK cycles	See SE8 reference manual for conversion time variances
	Long Sample (ADLSMP = 1)			—	40	—		
Sample Time	Short Sample (ADLSMP = 0)	D	t_{ADS}	—	3.5	—	ADCK cycles	
	Long Sample (ADLSMP = 1)			—	23.5	—		
Temp Sensor Slope	–40°C– 25°C	D	m	—	3.266	—	mV/°C	
	25°C– 125°C			—	3.638	—		
Temp Sensor Voltage	25°C	D	V_{TEMP25}	—	1.396	—	mV	
Characteristics for 28-pin packages only								
Total Unadjusted Error	10-bit mode	P	E_{TUE}	—	±1	±2.5	LSB[3]	Includes quantization
	8-bit mode	P		—	±0.5	±1.0		
Differential Non-Linearity	10-bit mode[2]	P	DNL	—	±0.5	±1.0	LSB[3]	
	8-bit mode[3]	P		—	±0.3	±0.5		
Integral Non-Linearity	10-bit mode	T	INL	—	±0.5	±1.0	LSB[3]	
	8-bit mode	T		—	±0.3	±0.5		
Zero-Scale Error	10-bit mode	P	E_{ZS}	—	±0.5	±1.5	LSB[3]	V_{ADIN} = V_{SSA}
	8-bit mode	P		—	±0.5	±0.5		
Full-Scale Error	10-bit mode	T	E_{FS}	—	±0.5	±1	LSB[3]	V_{ADIN} = V_{DDA}
	8-bit mode	T		—	±0.5	±0.5		
Quantization Error	10-bit mode	D	E_Q	—	—	±0.5	LSB[3]	
	8-bit mode			—	—	±0.5		
Input Leakage Error	10-bit mode	D	E_{IL}	—	±0.2	±2.5	LSB[3]	Pad leakage[4] * R_{AS}
	8-bit mode			—	±0.1	±1		
Characteristics for 16-pin package only								
Total Unadjusted Error	10-bit mode	P	E_{TUE}	—	±1.5	±3.5	LSB[3]	Includes quantization
	8-bit mode	P		—	±0.7	±1.5		

3.10 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 13. Control Timing

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	DC	—	10	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	µs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive[3]	t_{rstdrv}	$34 \times t_{cyc}$	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes[4]	t_{MSH}	100	—	—	µs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[5]	t_{ILIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	—	—	ns
8	D	Pin interrupt pulse width Asynchronous path[2] Synchronous path[5]	t_{ILIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	—	—	ns
9	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	—	 40 75	—	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF) Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	—	 11 35	—	ns

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 When any reset is initiated, internal circuitry drives the reset pin (if enabled, RSTPE = 1) low for about 34 cycles of t_{cyc}.

4 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

5 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

6 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 125 °C.

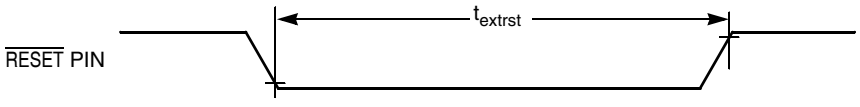
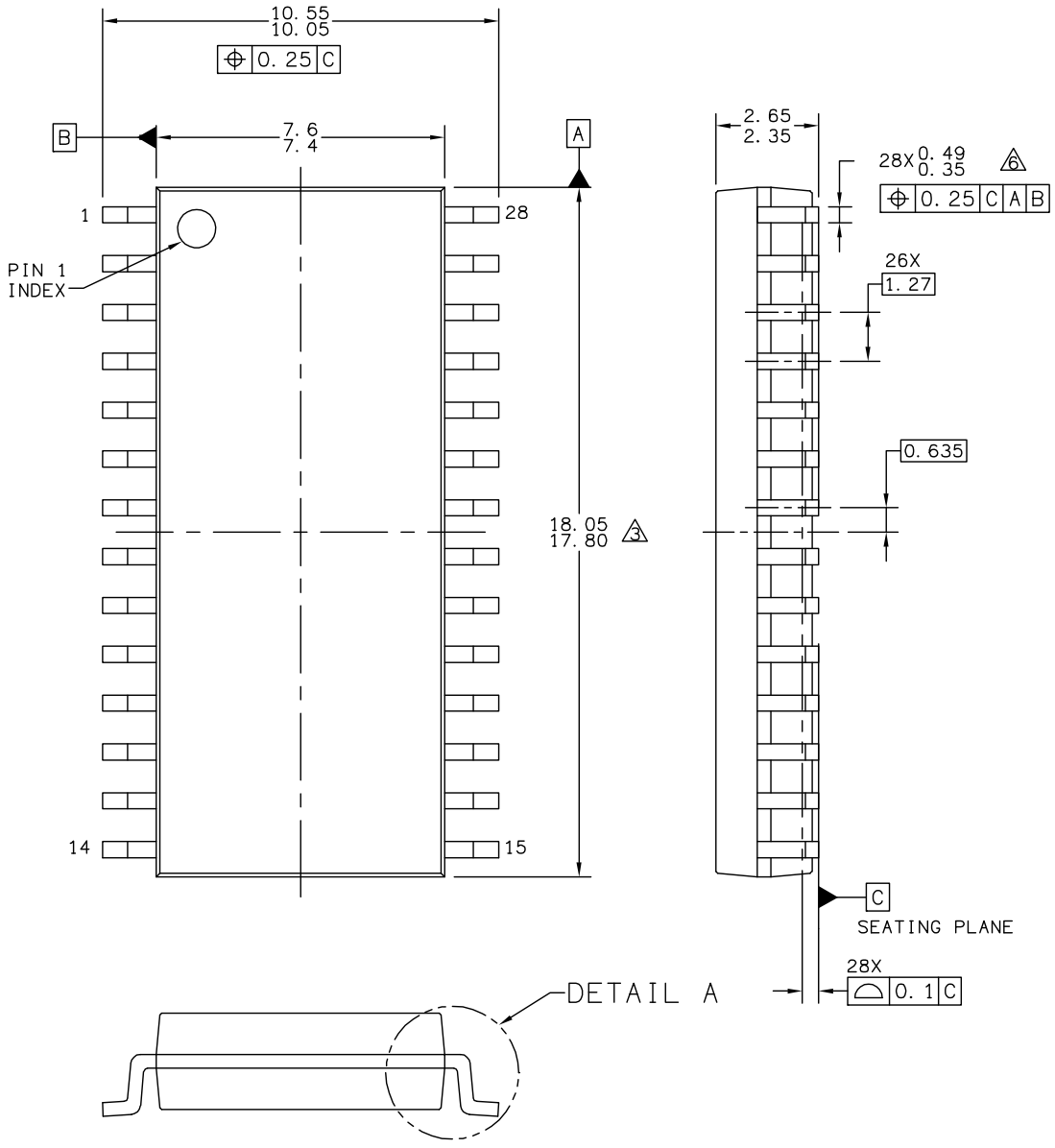


Figure 19. Reset Timing



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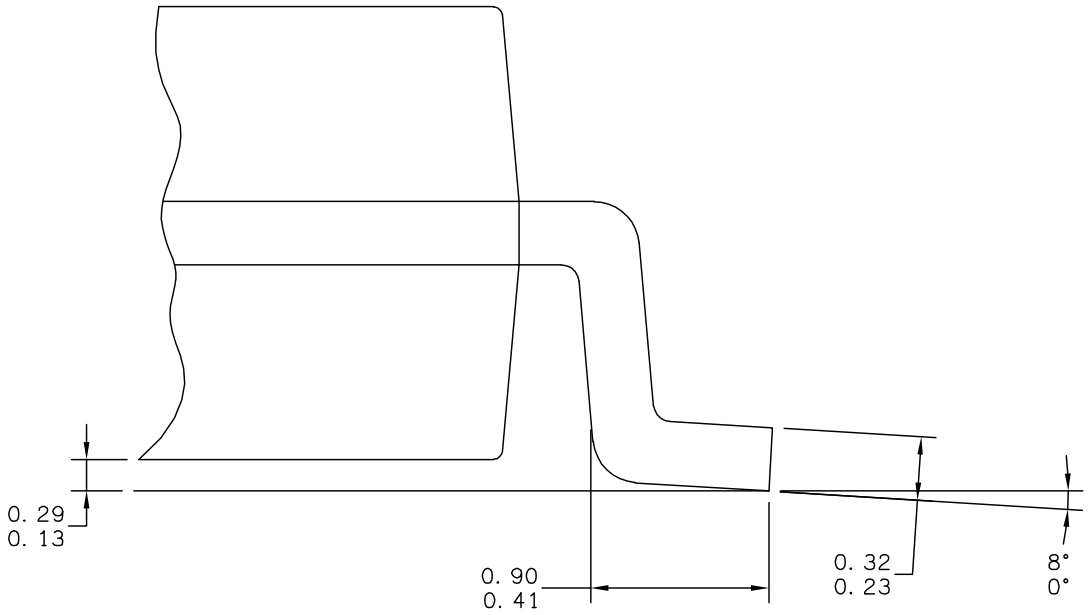
	CASE NUMBER: 751F-05	10 MAR 2005
	STANDARD: MS-013AE	



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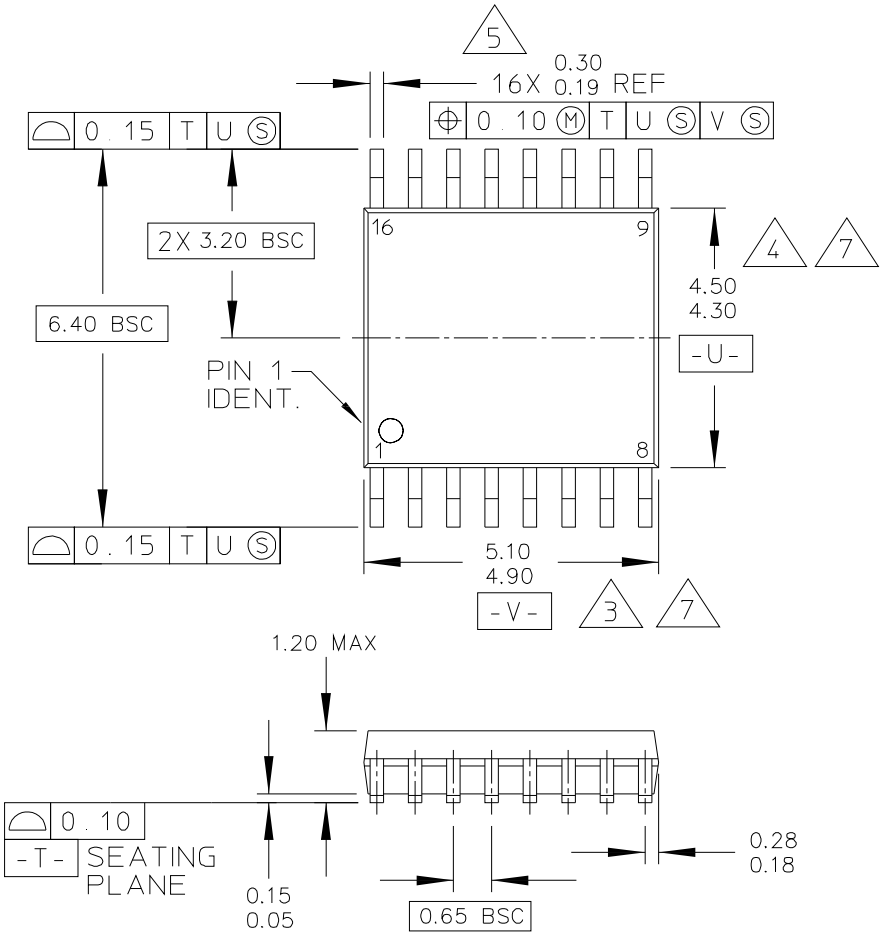

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	CASE NUMBER: 948F-01	19 MAY 2005
	STANDARD: JEDEC	

NOTES:

1. CONTROLLING DIMENSION: MILLIMETER
2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASH70247A	REV: B
16 LD TSSOP, PITCH 0.65MM	CASE NUMBER: 948F-01	19 MAY 2005
	STANDARD: JEDEC	