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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	LINbus, SCI
Peripherals	LVD, POR, PWM
Number of I/O	14
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mc9s08se8vtg">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mc9s08se8vtg</a>

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## Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to: [freescale.com](http://freescale.com)

The following revision history table summarizes changes contained in this document.

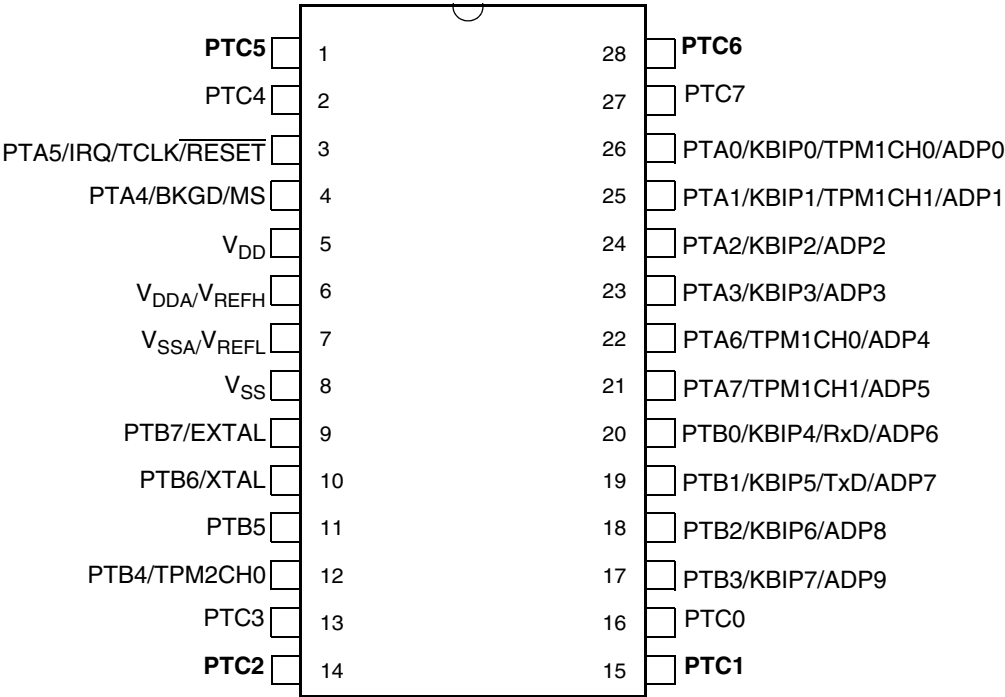
Revision	Date	Description of Changes
1	10/8/2008	Initial public released.
2	1/16/2009	In <a href="#">Table 8</a> , added the Max. of S2I <sub>DD</sub> and S3I <sub>DD</sub> in 0–105 °C; changed the Max. of S2I <sub>DD</sub> and S3I <sub>DD</sub> in 0–85 °C; changed the typical of S2I <sub>DD</sub> and S3I <sub>DD</sub> ; changed the S23I <sub>DDRTI</sub> to P.
3	4/7/2009	Added  I <sub>OZTOT</sub>   in the <a href="#">Table 7</a> . Changed V <sub>DDAD</sub> to V <sub>DDA</sub> , V <sub>SSAD</sub> to V <sub>SSA</sub> . Updated <a href="#">Table 9</a> , <a href="#">Table 10</a> , <a href="#">Table 11</a> , and <a href="#">Table 12</a> . Updated <a href="#">Figure 13</a> and <a href="#">Figure 14</a> .
4	4/10/2015	Updated <a href="#">Table 9</a> .

## Related Documentation

Find the most current versions of all documents at: <http://www.freescale.com>

### Reference Manual (MC9S08SE8RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.



Pins in **bold** are lost in the next lower pin count package.

Figure 2. MC9S08SE8 Series in 28-Pin PDIP/SOIC Package

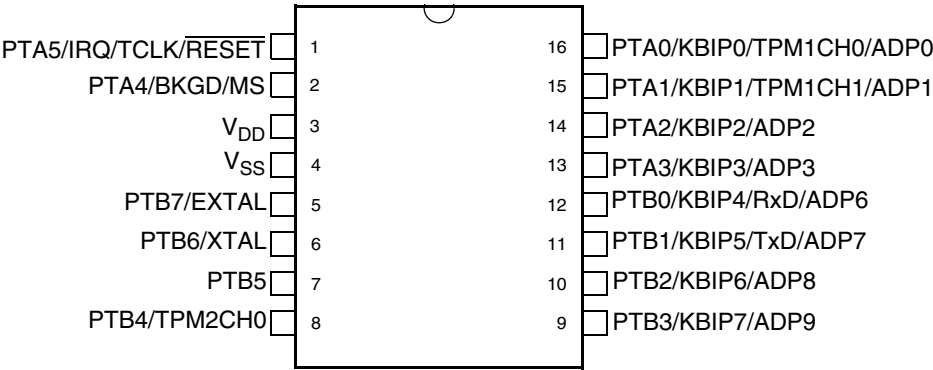


Figure 3. MC9S08SE8 in 16-Pin TSSOP Package

## 3 Electrical Characteristics

This chapter contains electrical and timing specifications.

### 3.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

**Table 2. Parameter Classifications**

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

#### NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

### 3.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in [Table 3](#) may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either  $V_{SS}$  or  $V_{DD}$ ) or the programmable pull-up resistor associated with the pin is enabled.

**Table 3. Absolute Maximum Ratings**

Rating	Symbol	Value	Unit
Supply voltage	$V_{DD}$	−0.3 to 5.8	V
Maximum current into $V_{DD}$	$I_{DD}$	120	mA
Digital input voltage	$V_{In}$	−0.3 to $V_{DD} + 0.3$	V
Instantaneous maximum current Single pin limit (applies to all port pins) <sup>1, 2, 3</sup>	$I_D$	±25	mA
Storage temperature range	$T_{stg}$	−55 to 150	°C

- <sup>1</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive ( $V_{DD}$ ) and negative ( $V_{SS}$ ) clamp voltages, then use the larger of the two resistance values.
- <sup>2</sup> All functional non-supply pins are internally clamped to  $V_{SS}$  and  $V_{DD}$ .
- <sup>3</sup> Power supply must maintain regulation within operating  $V_{DD}$  range during instantaneous and operating maximum current conditions. If positive injection current ( $V_{In} > V_{DD}$ ) is greater than  $I_{DD}$ , the injection current may flow out of  $V_{DD}$  and could result in external power supply going out of regulation. Ensure external  $V_{DD}$  load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

### 3.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take  $P_{I/O}$  into account in power calculations, determine the difference between actual pin voltage and  $V_{SS}$  or  $V_{DD}$  and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and  $V_{SS}$  or  $V_{DD}$  will be very small.

**Table 4. Thermal Characteristics**

Rating		Symbol	Value	Unit
Operating temperature range (packaged)	C	$T_A$	$T_L$ to $T_H$	°C
	V		−40 to 85	
	M		−40 to 105	
	M		−40 to 125	
Maximum junction temperature		$T_{JM}$	135	°C
Thermal resistance single-layer board	28-pin SOIC	$\theta_{JA}$	70	°C/W
	28-pin PDIP		68	
	16-pin TSSOP		129	
Thermal resistance four-layer board	28-pin SOIC		48	°C/W
	28-pin PDIP		49	
	16-pin TSSOP		85	

Table 5. ESD and Latch-up Test Conditions (continued)

Model	Description	Symbol	Value	Unit
Latch-up	Minimum input voltage limit	—	−2.5	V
	Maximum input voltage limit	—	7.5	V

Table 6. ESD and Latch-up Protection Characteristics

No.	Rating <sup>1</sup>	Symbol	Min	Max	Unit
1	Human body model (HBM)	$V_{HBM}$	±2000	—	V
2	Machine model (MM)	$V_{MM}$	±200	—	V
3	Charge device model (CDM)	$V_{CDM}$	±500	—	V
4	Latch-up current at $T_A = 125\text{ °C}$	$I_{LAT}$	±100	—	mA

<sup>1</sup> Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

## 3.5 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 7. DC Characteristics

Num	C	Parameter	Symbol	Min	Typical <sup>1</sup>	Max	Unit
1	—	Operating voltage	—	2.7	—	5.5	V
2	P	Output high voltage — Low drive (PTxDSn = 0) 5 V, $I_{Load} = -2\text{ mA}$ 3 V, $I_{Load} = -0.6\text{ mA}$ 5 V, $I_{Load} = -0.4\text{ mA}$ 3 V, $I_{Load} = -0.24\text{ mA}$	$V_{OH}$	$V_{DD} - 1.5$ $V_{DD} - 1.5$ $V_{DD} - 0.8$ $V_{DD} - 0.8$	— — — —	— — — —	V
		Output high voltage — High drive (PTxDSn = 1) 5 V, $I_{Load} = -10\text{ mA}$ 3 V, $I_{Load} = -3\text{ mA}$ 5 V, $I_{Load} = -2\text{ mA}$ 3 V, $I_{Load} = -0.4\text{ mA}$		$V_{DD} - 1.5$ $V_{DD} - 1.5$ $V_{DD} - 0.8$ $V_{DD} - 0.8$	— — — —	— — — —	
3	P	Output low voltage — Low drive (PTxDSn = 0) 5 V, $I_{Load} = 2\text{ mA}$ 3 V, $I_{Load} = 0.6\text{ mA}$ 5 V, $I_{Load} = 0.4\text{ mA}$ 3 V, $I_{Load} = 0.24\text{ mA}$	$V_{OL}$	1.5 1.5 0.8 0.8	— — — —	— — — —	V
		Output low voltage — High drive (PTxDSn = 1) 5 V, $I_{Load} = 10\text{ mA}$ 3 V, $I_{Load} = 3\text{ mA}$ 5 V, $I_{Load} = 2\text{ mA}$ 3 V, $I_{Load} = 0.4\text{ mA}$		1.5 1.5 0.8 0.8	— — — —	— — — —	
4	P	Output high current — Max total $I_{OH}$ for all ports 5 V 3 V	$I_{OHT}$	— —	— —	100 60	mA

Table 7. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical <sup>1</sup>	Max	Unit
25	T	Low-voltage inhibit reset/recover hysteresis 5 V 3 V	$V_{hys}$	— —	100 60	— —	mV
26	P	Bandgap voltage reference <sup>9</sup>	$V_{BG}$	1.18	1.20	1.21	V

<sup>1</sup> Typical values are measured at 25 °C. Characterized, not tested.

<sup>2</sup> Measured with  $V_{In} = V_{DD}$  or  $V_{SS}$ .

<sup>3</sup> Measured with  $V_{In} = V_{SS}$ .

<sup>4</sup> Measured with  $V_{In} = V_{DD}$ .

<sup>5</sup> All functional non-supply pins are internally clamped to  $V_{SS}$  and  $V_{DD}$ .

<sup>6</sup> Input must be current-limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

<sup>7</sup> Power supply must maintain regulation within operating  $V_{DD}$  range during instantaneous and operating maximum current conditions. If positive injection current ( $V_{In} > V_{DD}$ ) is greater than  $I_{DD}$ , the injection current may flow out of  $V_{DD}$  and could result in external power supply going out of regulation. Ensure external  $V_{DD}$  load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

<sup>8</sup> Maximum is highest voltage that POR is guaranteed.

<sup>9</sup> Factory trimmed at  $V_{DD} = 5.0$  V, Temp = 25 °C.

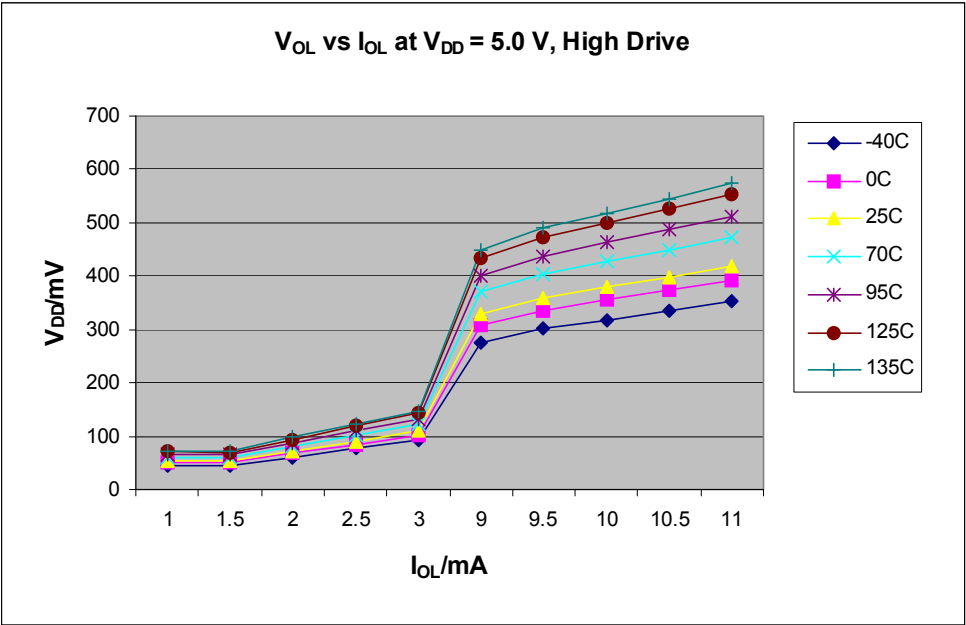


Figure 4. Typical V<sub>OL</sub> vs. I<sub>OL</sub> for High Drive Enabled Pad (V<sub>DD</sub> = 5 V)

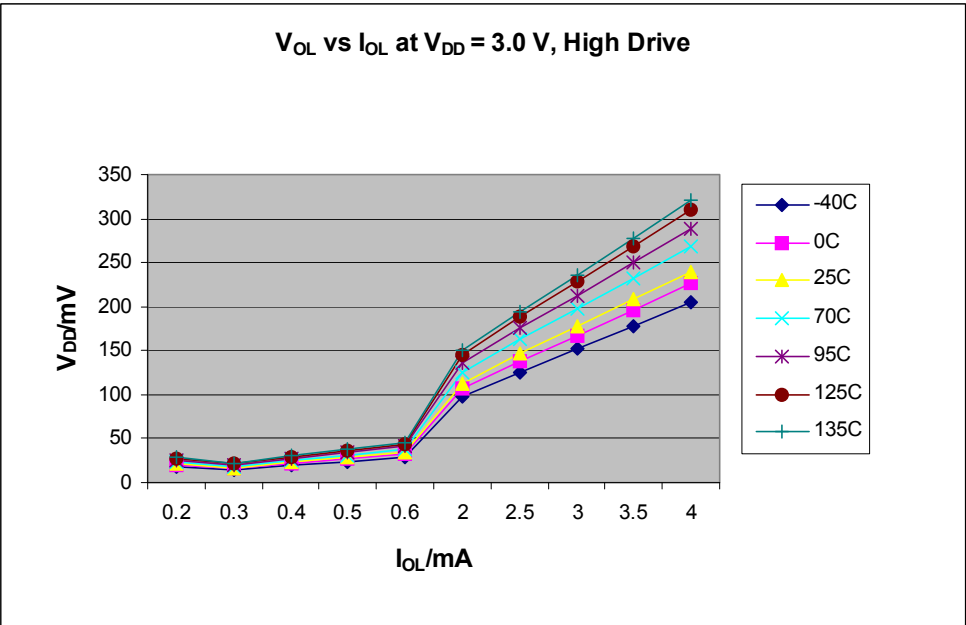


Figure 5. Typical V<sub>OL</sub> vs. I<sub>OL</sub> for High Drive Enabled Pad (V<sub>DD</sub> = 3 V)



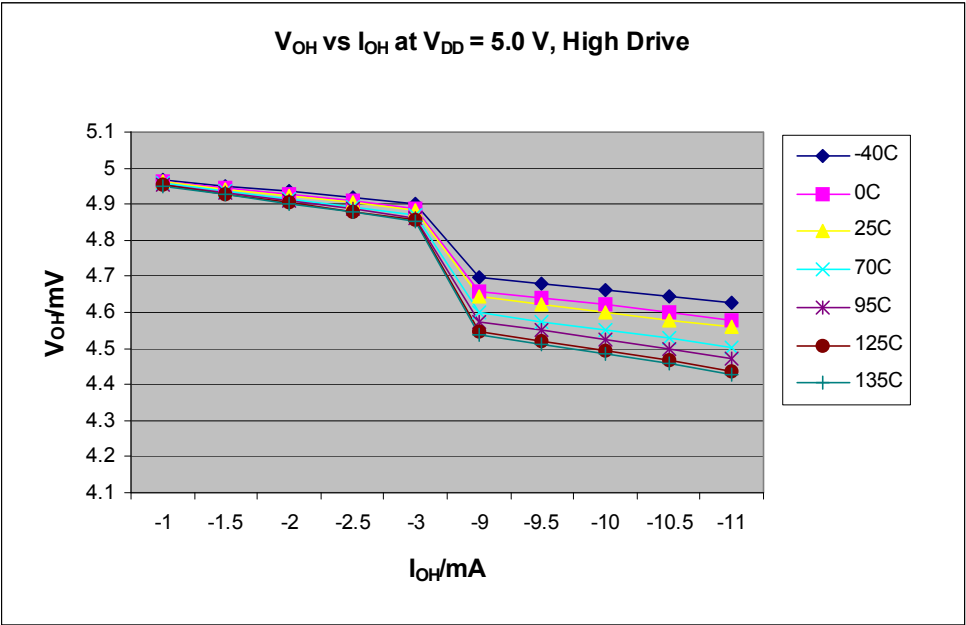


Figure 8. Typical  $V_{OH}$  vs.  $I_{OH}$  for High Drive Enabled Pad ( $V_{DD} = 5$  V)

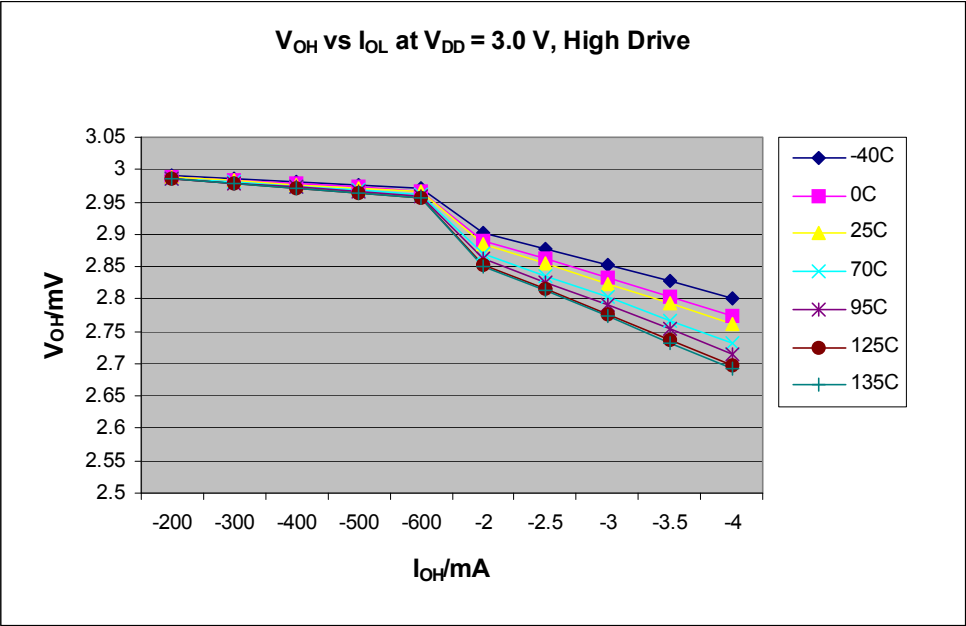


Figure 9. Typical  $V_{OH}$  vs.  $I_{OH}$  for High Drive Enabled Pad ( $V_{DD} = 3$  V)

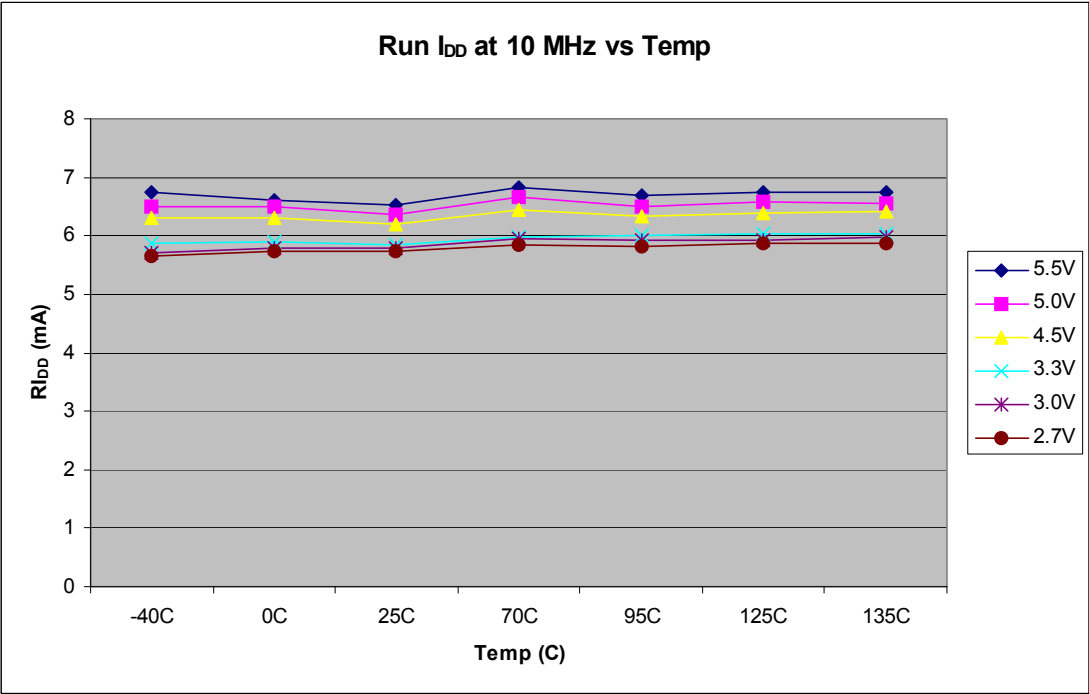


Figure 12. Typical Run  $I_{DD}$  Curves

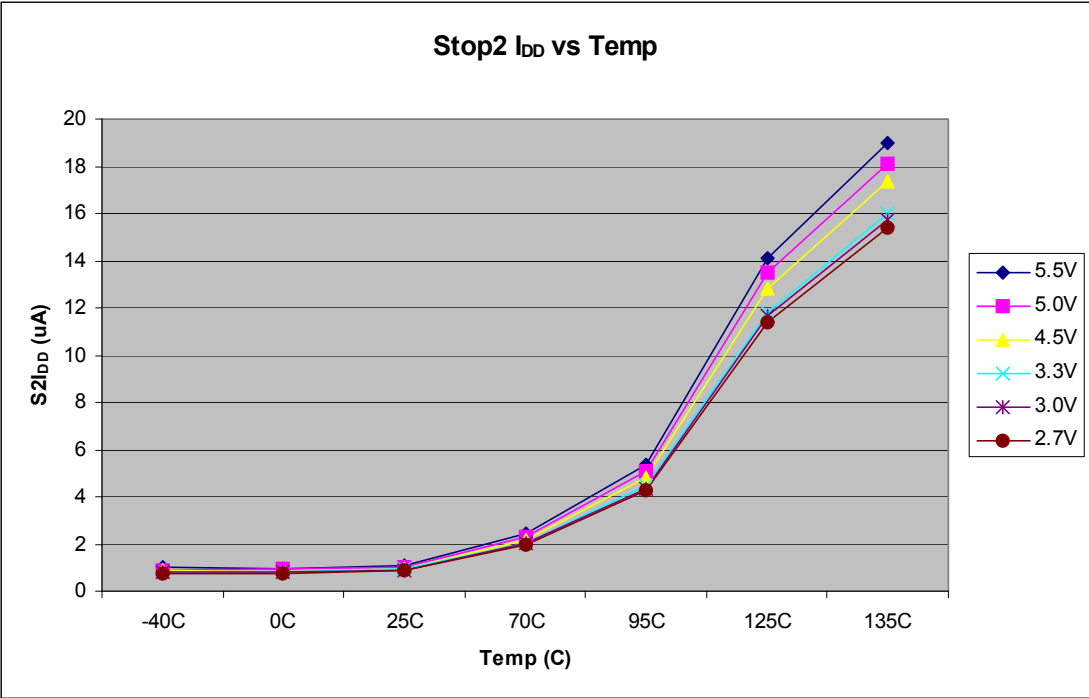
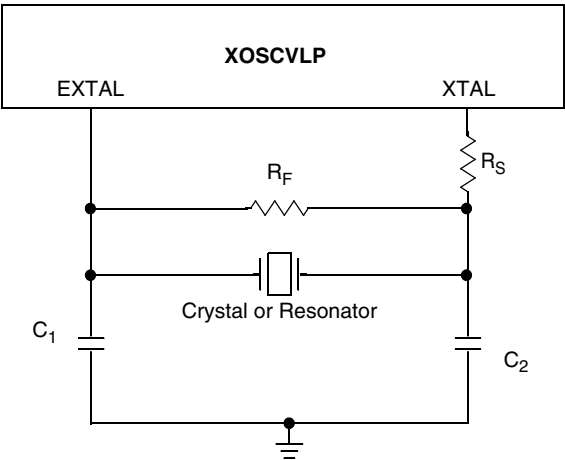


Figure 13. Typical Stop2  $I_{DD}$  Curves

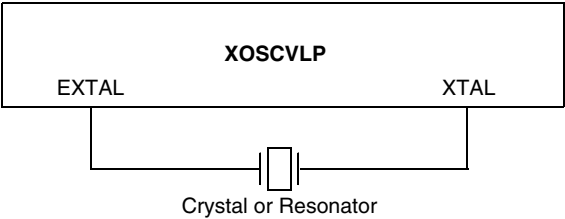
**Table 9. Oscillator electrical specifications (Temperature Range = –40 to 125°C Ambient)**

Num	C	Characteristic	Symbol	Min.	Typical <sup>1</sup>	Max.	Unit
5	T	Crystal start-up time <sup>3</sup>					
		Low range, low gain (RANGE = 0, HGO = 0)	$t_{CSTL-LP}$	—	200	—	ms
		Low range, high gain (RANGE = 0, HGO = 1)	$t_{CSTH-HGO}$	—	400	—	
		High range, low gain (RANGE = 1, HGO = 0) <sup>4</sup>	$t_{CSTH-LP}$	—	5	—	
		High range, high gain (RANGE = 1, HGO = 1) <sup>4</sup>	$t_{CSTH-HGO}$	—	15	—	
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1)					
		FEE or FBE mode <sup>2</sup>	$f_{extal}$	0.03125	—	20	MHz
		FBELP mode		0	—	20	MHz

- <sup>1</sup> Typical column was characterized at 5.0 V, 25 °C or is recommended value.
- <sup>2</sup> The input clock source must be divided using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
- <sup>3</sup> This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications. This data will vary based upon the crystal manufacturer and board design. The crystal should be characterized by the crystal manufacturer.
- <sup>4</sup> 4 MHz crystal.



**Figure 15. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain**



**Figure 16. Typical Crystal or Resonator Circuit: Low Range/Low Power**

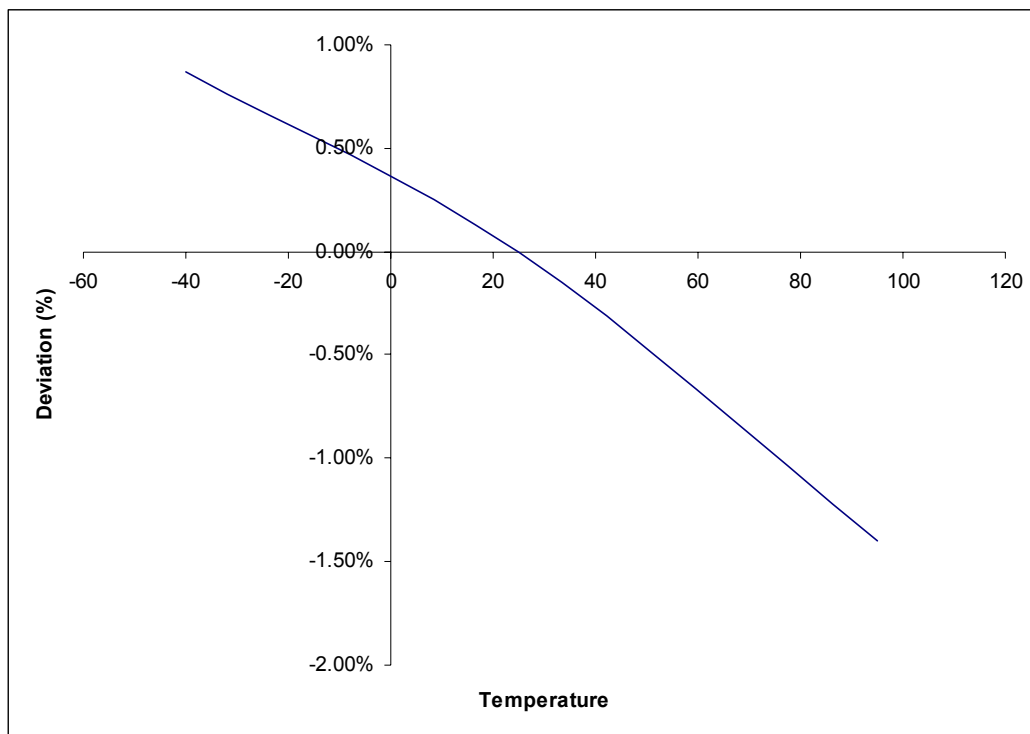


Figure 17. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

### 3.9 ADC Characteristics

Table 11. 10-Bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ <sup>1</sup>	Max	Unit	Comment
Supply voltage	Absolute	$V_{DDA}$	2.7	—	5.5	V	
	Delta to $V_{DD}$ ( $V_{DD} - V_{DDA}$ ) <sup>2</sup>	$\Delta V_{DDA}$	-100	0	100	mV	
Ground voltage	Delta to $V_{SS}$ ( $V_{SS} - V_{SSA}$ ) <sup>2</sup>	$\Delta V_{SSA}$	-100	0	100	mV	
Input voltage		$V_{ADIN}$	$V_{REFL}$	—	$V_{REFH}$	V	
Input capacitance		$C_{ADIN}$	—	4.5	5.5	pF	
Input resistance		$R_{ADIN}$	—	3	5	k $\Omega$	
Analog source resistance	10-bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$	$R_{AS}$	— —	— —	5 10	k $\Omega$	External to MCU
	8-bit mode (all valid $f_{ADCK}$ )		—	—	10		
ADC conversion clock frequency	High speed (ADLPC = 0)	$f_{ADCK}$	0.4	—	8.0	MHz	
	Low power (ADLPC = 1)		0.4	—	4.0		

## Electrical Characteristics

<sup>1</sup> Typical values assume  $V_{DDA} = 5.0$  V, Temp = 25 °C,  $f_{ADCK} = 1.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

<sup>2</sup> DC potential difference.

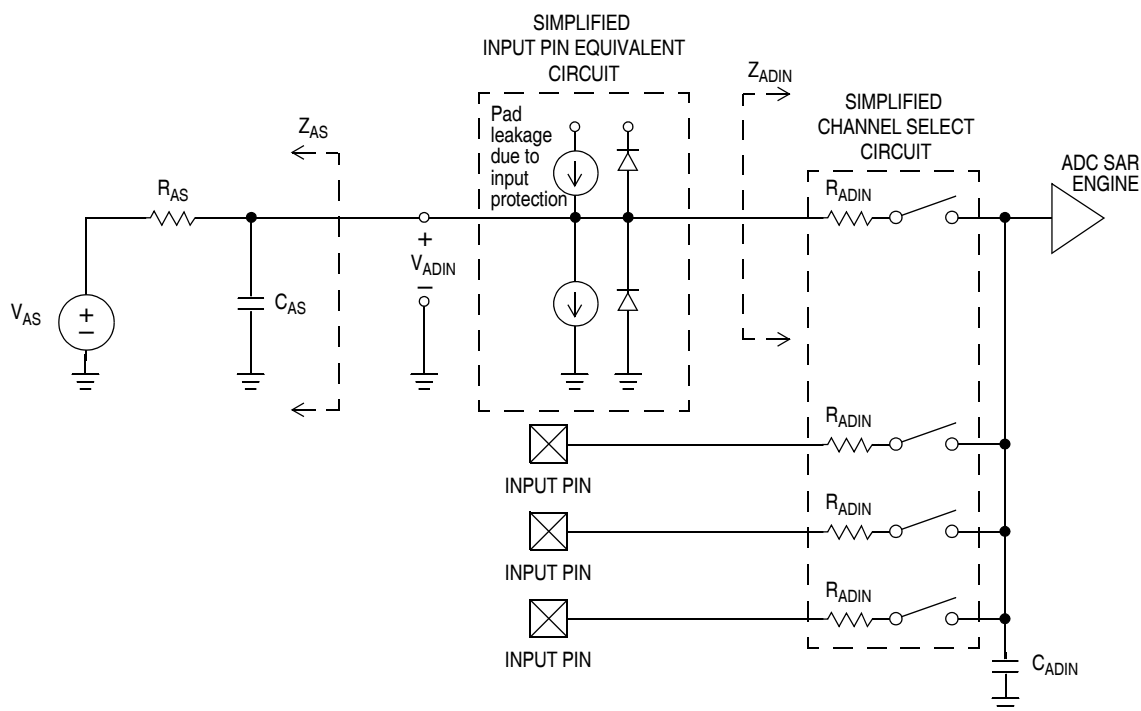


Figure 18. ADC Input Impedance Equivalency Diagram

Table 12. 10-Bit ADC Characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ )

Characteristic	Conditions	C	Symb	Min	Typ <sup>1</sup>	Max	Unit	Comment
Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	$I_{DDA}$	—	133	—	$\mu$ A	
Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	$I_{DDA}$	—	218	—	$\mu$ A	
Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	$I_{DDA}$	—	327	—	$\mu$ A	
Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1		D	$I_{DDA}$	—	0.582	1	mA	
Supply Current	Stop, Reset, Module Off	D	$I_{DDA}$	—	0.011	1	$\mu$ A	

**Table 12. 10-Bit ADC Characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

Characteristic	Conditions	C	Symb	Min	Typ <sup>1</sup>	Max	Unit	Comment
ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	D	f <sub>ADACK</sub>	2	3.3	5	MHz	t <sub>ADACK</sub> = 1/f <sub>ADACK</sub>
	Low Power (ADLPC = 1)			1.25	2	3.3		
Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	D	t <sub>ADC</sub>	—	20	—	ADCK cycles	See SE8 reference manual for conversion time variances
	Long Sample (ADLSMP = 1)			—	40	—		
Sample Time	Short Sample (ADLSMP = 0)	D	t <sub>ADS</sub>	—	3.5	—	ADCK cycles	
	Long Sample (ADLSMP = 1)			—	23.5	—		
Temp Sensor Slope	–40°C– 25°C	D	m	—	3.266	—	mV/°C	
	25°C– 125°C			—	3.638	—		
Temp Sensor Voltage	25°C	D	V <sub>TEMP25</sub>	—	1.396	—	mV	
Characteristics for 28-pin packages only								
Total Unadjusted Error	10-bit mode	P	E <sub>TUE</sub>	—	±1	±2.5	LSB <sup>3</sup>	Includes quantization
	8-bit mode	P		—	±0.5	±1.0		
Differential Non-Linearity	10-bit mode <sup>2</sup>	P	DNL	—	±0.5	±1.0	LSB <sup>3</sup>	
	8-bit mode <sup>3</sup>	P		—	±0.3	±0.5		
Integral Non-Linearity	10-bit mode	T	INL	—	±0.5	±1.0	LSB <sup>3</sup>	
	8-bit mode	T		—	±0.3	±0.5		
Zero-Scale Error	10-bit mode	P	E <sub>ZS</sub>	—	±0.5	±1.5	LSB <sup>3</sup>	V <sub>ADIN</sub> = V <sub>SSA</sub>
	8-bit mode	P		—	±0.5	±0.5		
Full-Scale Error	10-bit mode	T	E <sub>FS</sub>	—	±0.5	±1	LSB <sup>3</sup>	V <sub>ADIN</sub> = V <sub>DDA</sub>
	8-bit mode	T		—	±0.5	±0.5		
Quantization Error	10-bit mode	D	E <sub>Q</sub>	—	—	±0.5	LSB <sup>3</sup>	
	8-bit mode			—	—	±0.5		
Input Leakage Error	10-bit mode	D	E <sub>IL</sub>	—	±0.2	±2.5	LSB <sup>3</sup>	Pad leakage <sup>4</sup> * R <sub>AS</sub>
	8-bit mode			—	±0.1	±1		
Characteristics for 16-pin package only								
Total Unadjusted Error	10-bit mode	P	E <sub>TUE</sub>	—	±1.5	±3.5	LSB <sup>3</sup>	Includes quantization
	8-bit mode	P		—	±0.7	±1.5		

# Electrical Characteristics

**Table 12. 10-Bit ADC Characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

Characteristic	Conditions	C	Symb	Min	Typ <sup>1</sup>	Max	Unit	Comment
Differential Non-Linearity	10-bit mode <sup>3</sup>	P	DNL	—	±0.5	±1.0	LSB <sup>3</sup>	
	8-bit mode <sup>3</sup>	P		—	±0.3	±0.5		
Integral Non-Linearity	10-bit mode	T	INL	—	±0.5	±1.0	LSB <sup>3</sup>	
	8-bit mode	T		—	±0.3	±0.5		
Zero-Scale Error	10-bit mode	P	$E_{ZS}$	—	±1.5	±2.1	LSB <sup>3</sup>	$V_{ADIN} = V_{SSA}$
	8-bit mode	P		—	±0.5	±0.7		
Full-Scale Error	10-bit mode	T	$E_{FS}$	—	±1	±1.5	LSB <sup>3</sup>	$V_{ADIN} = V_{DDA}$
	8-bit mode	T		—	±0.5	±0.5		
Quantization Error	10-bit mode	D	$E_Q$	—	—	±0.5	LSB <sup>3</sup>	
	8-bit mode			—	—	±0.5		
Input Leakage Error	10-bit mode	D	$E_{IL}$	—	±0.2	±2.5	LSB <sup>3</sup>	Pad leakage <sup>4*</sup> $R_{AS}$
	8-bit mode			—	±0.1	±1		

<sup>1</sup> Typical values assume  $V_{DDA} = 5.0$  V, Temp = 25 °C,  $f_{ADCK} = 1.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

<sup>2</sup> Monotonicity and No-Missing-Codes guaranteed in 10-bit and 8-bit modes

<sup>3</sup> 1 LSB =  $(V_{REFH} - V_{REFL})/2^N$

<sup>4</sup> Based on input pad leakage current. Refer to pad electricals.

## 3.10 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

### 3.10.1 Control Timing

**Table 13. Control Timing**

Num	C	Rating	Symbol	Min	Typical <sup>1</sup>	Max	Unit
1	D	Bus frequency ( $t_{cyc} = 1/f_{Bus}$ )	$f_{Bus}$	DC	—	10	MHz
2	D	Internal low power oscillator period	$t_{LPO}$	700	—	1300	$\mu s$
3	D	External reset pulse width <sup>2</sup>	$t_{extrst}$	100	—	—	ns
4	D	Reset low drive <sup>3</sup>	$t_{rstdrv}$	$34 \times t_{cyc}$	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	$t_{MSSU}$	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes <sup>4</sup>	$t_{MSH}$	100	—	—	$\mu s$
7	D	IRQ pulse width Asynchronous path <sup>2</sup> Synchronous path <sup>5</sup>	$t_{LIH}, t_{IHL}$	100 $1.5 \times t_{cyc}$	—	—	ns
8	D	Pin interrupt pulse width Asynchronous path <sup>2</sup> Synchronous path <sup>5</sup>	$t_{LIH}, t_{IHL}$	100 $1.5 \times t_{cyc}$	—	—	ns
9	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF) <sup>6</sup> Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	$t_{Rise}, t_{Fall}$	—	40 75	—	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF) Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	$t_{Rise}, t_{Fall}$	—	11 35	—	ns

<sup>1</sup> Typical values are based on characterization data at  $V_{DD} = 5.0$  V, 25 °C unless otherwise stated.

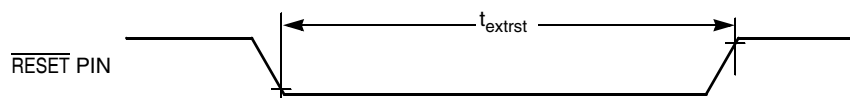
<sup>2</sup> This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

<sup>3</sup> When any reset is initiated, internal circuitry drives the reset pin (if enabled, RSTPE = 1) low for about 34 cycles of  $t_{cyc}$ .

<sup>4</sup> To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of  $t_{MSH}$  after  $V_{DD}$  rises above  $V_{LVD}$ .

<sup>5</sup> This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

<sup>6</sup> Timing is shown with respect to 20%  $V_{DD}$  and 80%  $V_{DD}$  levels. Temperature range –40 °C to 125 °C.



**Figure 19. Reset Timing**



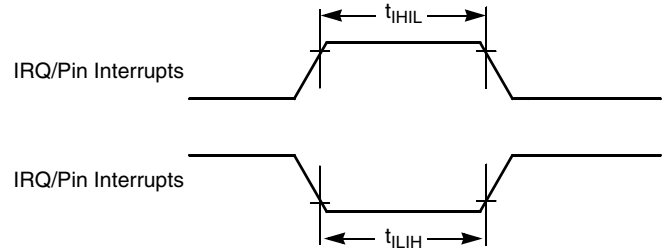


Figure 20. IRQ/Pin Interrupt Timing

### 3.10.2 TPM/MTIM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 14. TPM Input Timing

Num	C	Rating	Symbol	Min	Max	Unit
1	D	External clock frequency	$f_{TPMext}$	DC	$f_{Bus}/4$	MHz
2	D	External clock period	$t_{TPMext}$	4	—	$t_{cyc}$
3	D	External clock high time	$t_{clkh}$	1.5	—	$t_{cyc}$
4	D	External clock low time	$t_{clkl}$	1.5	—	$t_{cyc}$
5	D	Input capture pulse width	$t_{ICPW}$	1.5	—	$t_{cyc}$

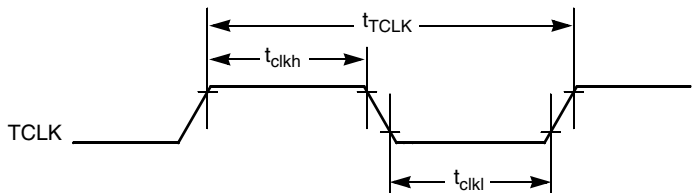


Figure 21. Timer External Clock

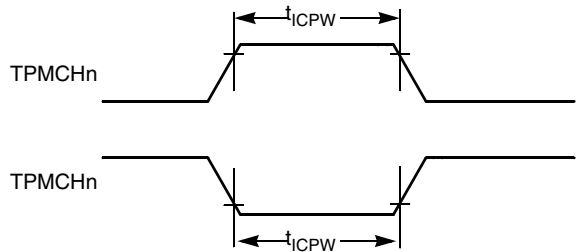


Figure 22. Timer Input Capture Pulse

## 3.11 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal  $V_{DD}$  supply. For more detailed information about program/erase operations, see the Memory section in the reference manual.

**Table 15. Flash Characteristics**

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage for program/erase	$V_{\text{prog/erase}}$	2.7	—	5.5	V
2	D	Supply voltage for read operation	$V_{\text{Read}}$	2.7	—	5.5	V
3	D	Internal FCLK frequency <sup>1</sup>	$f_{\text{FCLK}}$	150	—	200	kHz
4	D	Internal FCLK period (1/FCLK)	$t_{\text{Fcyc}}$	5	—	6.67	$\mu\text{s}$
5	P	Byte program time (random location) <sup>2</sup>	$t_{\text{prog}}$	9			$t_{\text{Fcyc}}$
6	P	Byte program time (burst mode) <sup>2</sup>	$t_{\text{Burst}}$	4			$t_{\text{Fcyc}}$
7	P	Page erase time <sup>2</sup>	$t_{\text{Page}}$	4000			$t_{\text{Fcyc}}$
8	P	Mass erase time <sup>2</sup>	$t_{\text{Mass}}$	20,000			$t_{\text{Fcyc}}$
9	C	Program/erase endurance <sup>3</sup> $T_L$ to $T_H$ = $-40^\circ\text{C}$ to $125^\circ\text{C}$ $T = 25^\circ\text{C}$	$n_{\text{FLPE}}$	10,000	— 100,000	—	cycles
10	C	Data retention <sup>4</sup>	$t_{\text{D\_ret}}$	15	100	—	years

<sup>1</sup> The frequency of this clock is controlled by a software setting.

<sup>2</sup> These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

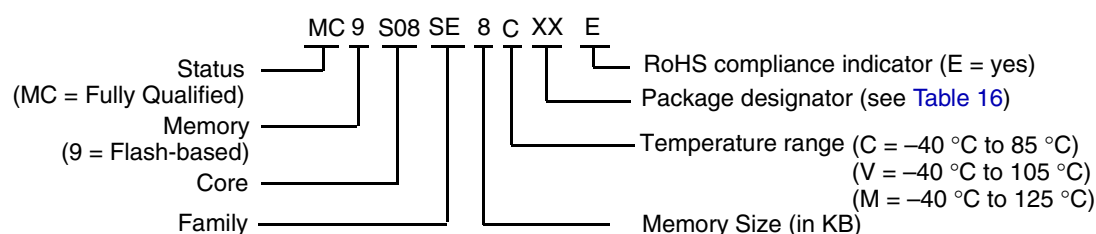
<sup>3</sup> **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory*.

<sup>4</sup> **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to  $25^\circ\text{C}$  using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory*.

## 4 Ordering Information

This chapter contains ordering information for the device numbering system.

Example of the device numbering system:



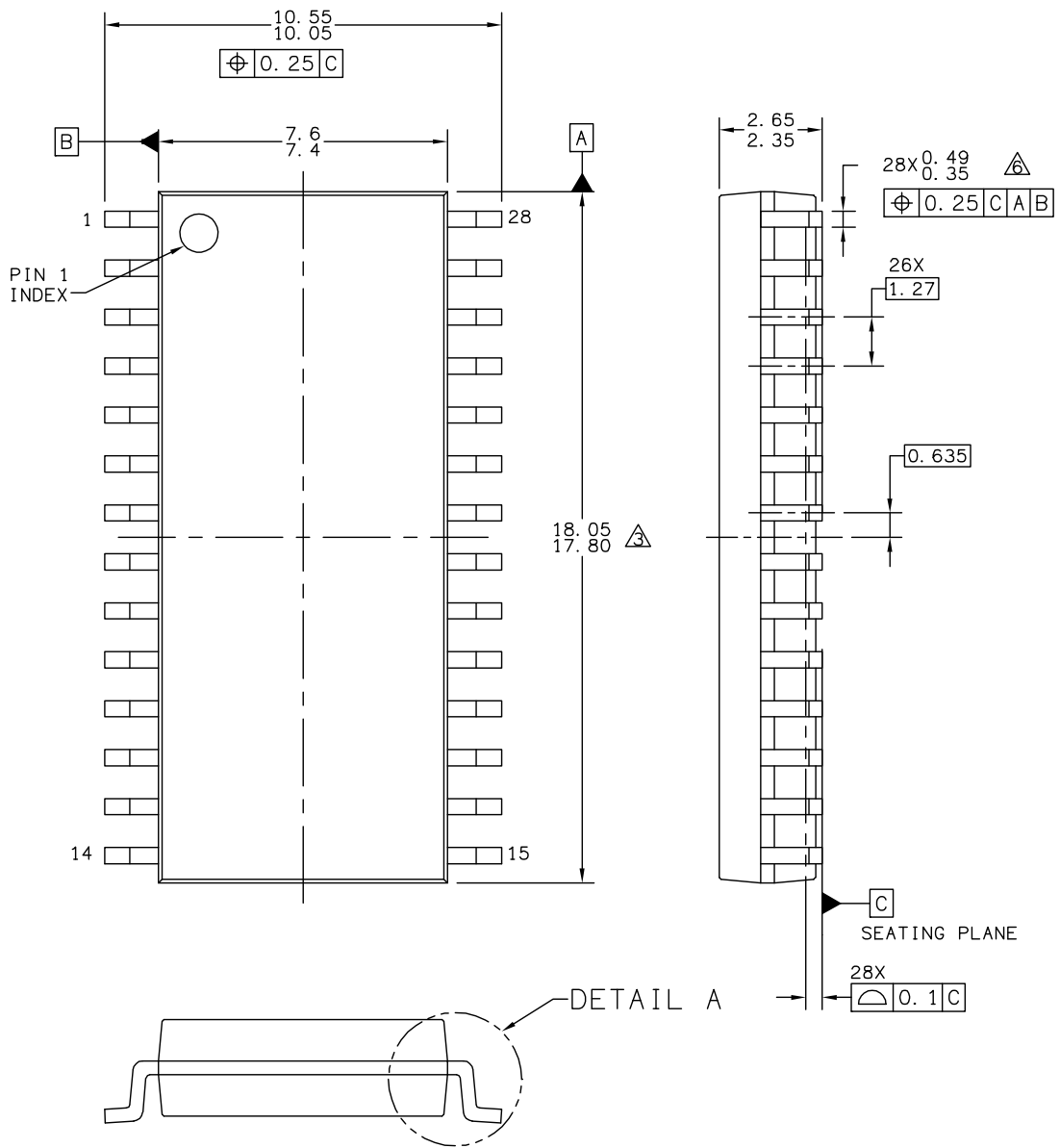
## 4.1 Package Information

**Table 16. Package Descriptions**

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
28	Plastic Dual In-line Pin	PDIP	RL	710	98ASB42390B
28	Small Outline Integrated Circuit	SOIC	WL	751F	98ASB42345B
16	Thin Shrink Small Outline Package	TSSOP	TG	948F	98ASH70247A

## 4.2 Mechanical Drawings

The following pages are mechanical drawings for the packages described in [Table 16](#).



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	TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE		DOCUMENT NO: 98ASB42345B	REV: G
			CASE NUMBER: 751F-05	10 MAR 2005
			STANDARD: MS-013AE	

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