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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	41 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	8-TSSOP, 8-MSOP (0.118", 3.00mm Width)
Supplier Device Package	8-MSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f519-e-ms

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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NOTES:

5.0 FLASH DATA MEMORY CONTROL

The Flash data memory is readable and writable during normal operation (full VDD range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers (SFRs).

5.1 Reading Flash Data Memory

To read a Flash data memory location the user must:

- Write the EEADR register
- Set the RD bit of the EECON register

The value written to the EEADR register determines which Flash data memory location is read. Setting the RD bit of the EECON register initiates the read. Data from the Flash data memory read is available in the EEDATA register immediately. The EEDATA register will hold this value until another read is initiated or it is modified by a write operation. Program execution is suspended while the read cycle is in progress. Execution will continue with the instruction following the one that sets the WR bit. See Example 1 for sample code.

EXAMPLE 1: READING FROM FLASH DATA MEMORY

```
BANKSEL EEADR      ;
MOVF DATA_EE_ADDR, W  ;
MOVWF EEADR        ;Data Memory
                   ;Address to read

BANKSEL EECON1      ;

BSF EECON, RD       ;EE Read
MOVF EEDATA, W      ;W = EEDATA
```

Note: Only a BSF command will work to enable the Flash data memory read documented in Example 1. No other sequence of commands will work, no exceptions.

5.2 Writing and Erasing Flash Data Memory

Flash data memory is erased one row at a time and written one byte at a time. The 64-byte array is made up of eight rows. A row contains eight sequential bytes. Row boundaries exist every eight bytes.

Generally, the procedure to write a byte of data to Flash data memory is:

1. Identify the row containing the address where the byte will be written.
2. If there is other information in that row that must be saved, copy those bytes from Flash data memory to RAM.
3. Perform a row erase of the row of interest.

4. Write the new byte of data and any saved bytes back to the appropriate addresses in Flash data memory.

To prevent accidental corruption of the Flash Data Memory, an unlock sequence is required to initiate a write or erase cycle. This sequence requires that the bit set instructions used to configure the EECON register happen exactly as shown in Example 2 and Example 3, depending on the operation requested.

5.2.1 ERASING FLASH DATA MEMORY

A row must be manually erased before writing new data. The following sequence must be performed for a single row erase.

1. Load EEADR with an address in the row to be erased.
2. Set the FREE bit to enable the erase.
3. Set the WREN bit to enable write access to the array.
4. Set the WR bit to initiate the erase cycle.

If the WREN bit is not set in the instruction cycle after the FREE bit is set, the FREE bit will be cleared in hardware.

If the WR bit is not set in the instruction cycle after the WREN bit is set, the WREN bit will be cleared in hardware.

Sample code that follows this procedure is included in Example 2.

Program execution is suspended while the erase cycle is in progress. Execution will continue with the instruction following the one that sets the WR bit.

EXAMPLE 2: ERASING A FLASH DATA MEMORY ROW

```
BANKSEL EEADR
MOVLW EE_ADR_ERASE ; LOAD ADDRESS OF ROW TO
                   ; ERASE
MOVWF EEADR        ;
BSF EECON, FREE    ; SELECT ERASE
BSF EECON, WREN    ; ENABLE WRITES
BSF EECON, WR      ; INITIATE ERASE
```

Note 1: The FREE bit may be set by any command normally used by the core. However, the WREN and WR bits can only be set using a series of BSF commands, as documented in Example 1. No other sequence of commands will work, no exceptions.

2: Bits <5:3> of the EEADR register indicate which row is to be erased.

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5.2.2 WRITING TO FLASH DATA MEMORY

Once a cell is erased, new data can be written. Program execution is suspended during the write cycle. The following sequence must be performed for a single byte write.

1. Load EEADR with the address.
2. Load EEDATA with the data to write.
3. Set the WREN bit to enable write access to the array.
4. Set the WR bit to initiate the erase cycle.

If the WR bit is not set in the instruction cycle after the WREN bit is set, the WREN bit will be cleared in hardware.

Sample code that follows this procedure is included in Example 3.

EXAMPLE 3: WRITING A FLASH DATA MEMORY ROW

```
BANKSEL    EEADR
MOVLW     EE_ADR_WRITE    ; LOAD ADDRESS
MOVWF     EEADR           ;
MOVLW     EE_DATA_TO_WRITE ; LOAD DATA
MOVWF     EEDATA          ; INTO EEDATA REGISTER
BSF       EECON,WREN      ; ENABLE WRITES
BSF       EECON,WR        ; INITITATE ERASE
```

Note 1: Only a series of BSF commands will work to enable the memory write sequence documented in Example 2. No other sequence of commands will work, no exceptions.

- 2: For reads, erases and writes to the Flash data memory, there is no need to insert a NOP into the user code as is done on mid-range devices. The instruction immediately following the “BSF EECON,WR/RD” will be fetched and executed properly.

5.3 Write Verify

Depending on the application, good programming practice may dictate that data written to the Flash data memory be verified. Example 4 is an example of a write verify.

EXAMPLE 4: WRITE VERIFY OF DATA EEPROM

```
MOVF      EEDATA, W      ;EEDATA has not changed
                                ;from previous write
BSF       EECON, RD      ;Read the value written
XORWF     EEDATA, W      ;
BTFSS     STATUS, Z      ;Is data the same
GOTO      WRITE_ERR      ;No, handle error
                                ;Yes, continue
```

5.4 Code Protection

Code protection does not prevent the CPU from performing read or write operations on the Flash data memory. Refer to the code protection chapter for more information.

6.0 I/O PORT

As with any other register, the I/O register(s) can be written and read under program control. However, read instructions (e.g., `MOVF PORTB, W`) always read the I/O pins independent of the pin's Input/Output modes. On Reset, all I/O ports are defined as input (inputs are at high-impedance) since the I/O control registers are all set.

6.1 GPIO

GPIO is an 8-bit I/O register. Only the low-order 6 bits are used (GP<5:0>). Bits 7 and 6 are unimplemented and read as '0's. Please note that GP3 is an input-only pin. The Configuration Word can set several I/O's to alternate functions. When acting as alternate functions, the pins will read as '0' during a port read. Pins GP0, GP1, and GP3 can be configured with weak pull-ups and also for wake-up on change. The wake-up on change and weak pull-up functions are not pin selectable. If GP3/MCLR is configured as MCLR, weak pull-up is always on and wake-up on change for this pin is not enabled.

6.2 TRIS Registers

The Output Driver Control registers are loaded with the contents of the W Register by executing the `TRIS f` instruction. A '1' from a TRISGPIO Register bit puts the corresponding output driver in a high-impedance (Input) mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer.

The TRISGPIO register is "write-only". Bits <5:0> are set (output drivers disabled) upon Reset.

Note: If the T0CS bit is set to '1', it will override the TRISGPIO function on the T0CKI pin.

TABLE 6-1: WEAK PULL-UP ENABLED PINS

Pin	WPU	WU
GP0	Y	Y
GP1	Y	Y
GP2	N	N
GP3	Y ⁽¹⁾	Y
GP4	N	N
GP5	N	N
GP6	N	N

Note 1: When MCLRE = 1, the weak pull-up on GP3/MCLR is always enabled.

2: WPU = Weak pull-up; WU = Wake-up.

7.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select:
 - Edge select for external clock

Figure 7-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 7-2 and Figure 7-3). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The T0SE bit (OPTION<4>) determines the source edge. Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in **Section 7.1 “Using Timer0 with an External Clock”**.

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. The prescaler assignment is controlled in software by the control bit, PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. **Section 7.2 “Prescaler”** details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 7-1.

The Timer0 contained in the CPU core follows the standard baseline definition.

FIGURE 7-1: TIMER0 BLOCK DIAGRAM

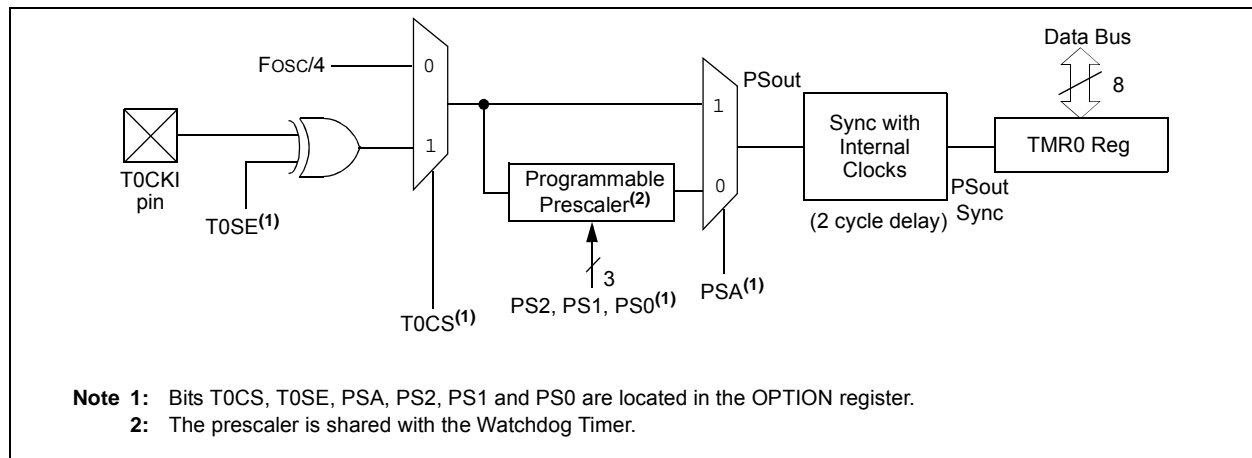


FIGURE 7-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE

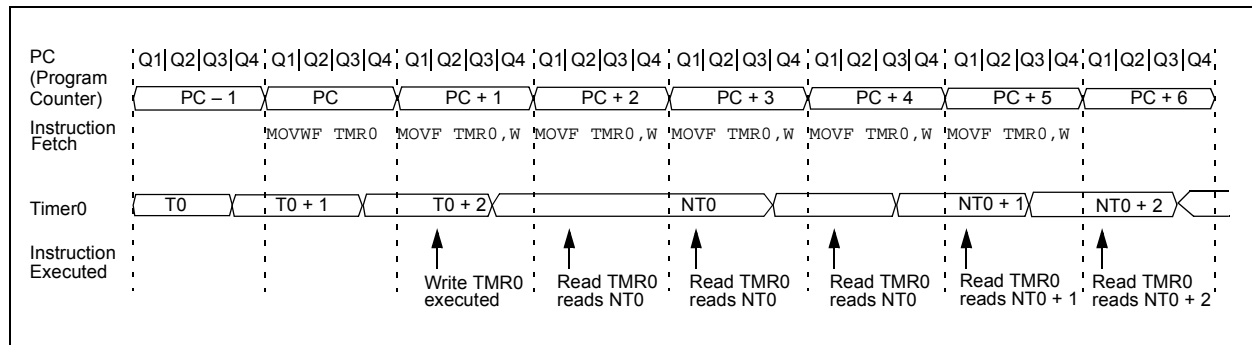
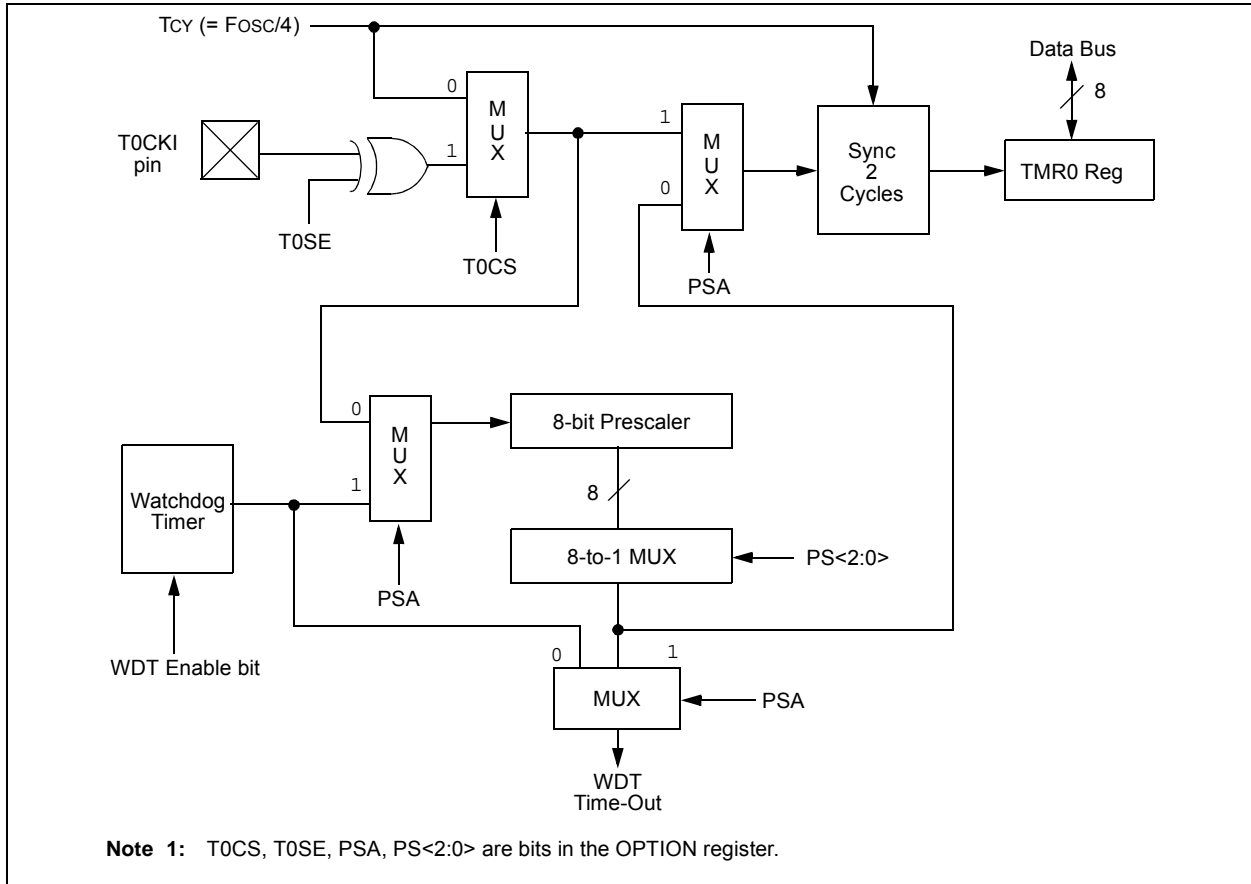


FIGURE 7-5: BLOCK DIAGRAM OF THE TIMER0/ WDT PRESCALER⁽¹⁾



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NOTES:

8.7 Time-out Sequence, Power-down and Wake-up from Sleep Status Bits (\overline{TO} , \overline{PD} , GPWUF)

The \overline{TO} , \overline{PD} and (GPWUF) bits in the STATUS register can be tested to determine if a Reset condition has been caused by a power-up condition, a \overline{MCLR} or Watchdog Timer (WDT) Reset.

TABLE 8-7: $\overline{TO}/\overline{PD}/(GPWUF)$ STATUS AFTER RESET

GPWUF	\overline{TO}	\overline{PD}	Reset Caused By
0	0	0	WDT wake-up from Sleep
0	0	u	WDT time-out (not from Sleep)
0	1	0	\overline{MCLR} wake-up from Sleep
0	1	1	Power-up
0	u	u	\overline{MCLR} not during Sleep
1	1	0	Wake-up from Sleep on pin change

Legend: u = unchanged

Note 1: The \overline{TO} , \overline{PD} and GPWUF bits maintain their status (u) until a Reset occurs. A low-pulse on the \overline{MCLR} input does not change the \overline{TO} , \overline{PD} and GPWUF Status bits.

8.8 Power-down Mode (Sleep)

A device may be powered down (Sleep) and later powered up (wake-up from Sleep).

8.8.1 SLEEP

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the \overline{TO} bit (STATUS<4>) is set, the \overline{PD} bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low or high-impedance).

Note: A Reset generated by a WDT time-out does not drive the \overline{MCLR} pin low.

For lowest current consumption while powered down, the T0CKI input should be at VDD or VSS and the GP3/ \overline{MCLR}/V_{PP} pin must be at a logic high level if \overline{MCLR} is enabled.

8.8.2 WAKE-UP FROM SLEEP

The device can wake-up from Sleep through one of the following events:

5. An external Reset input on GP3/ \overline{MCLR}/V_{PP} pin, when configured as \overline{MCLR} .
6. A Watchdog Timer Time-out Reset (if WDT was enabled).
7. A change on input pin GP0, GP1 and GP3 when wake-up on change is enabled.

These events cause a device Reset. The \overline{TO} , \overline{PD} and GPWUF bits can be used to determine the cause of device Reset. The \overline{TO} bit is cleared if a WDT time-out occurred (and caused wake-up). The \overline{PD} bit, which is set on power-up, is cleared when SLEEP is invoked. The GPWUF bit indicates a change in state while in Sleep at pins GP0, GP1 and GP3 (since the last file or bit operation on GPIO port).

Note: **Caution:** Right before entering Sleep, read the input pins. When in Sleep, wake up occurs when the values at the pins change from the state they were in at the last reading. If a wake-up on change occurs and the pins are not read before re-entering Sleep, a wake-up will occur immediately even if no pins change while in Sleep mode.

The WDT is cleared when the device wakes from Sleep, regardless of the wake-up source.

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8.9 Program Verification/Code Protection

If the code protection bits have not been programmed, the on-chip program and data memory can be read out for verification purposes.

The first 64 locations and the last location (OSCCAL) can be read, regardless of the setting of the program memory's code protection bit. If the code protect bit specific to the FLASH data memory is programmed, then none of the contents of this memory region can be verified externally.

8.10 ID Locations

Four memory locations are designated as ID locations where users can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during program/verify.

Use only the lower 4 bits of the ID locations. The upper bits should be programmed as 0s.

8.11 In-Circuit Serial Programming™

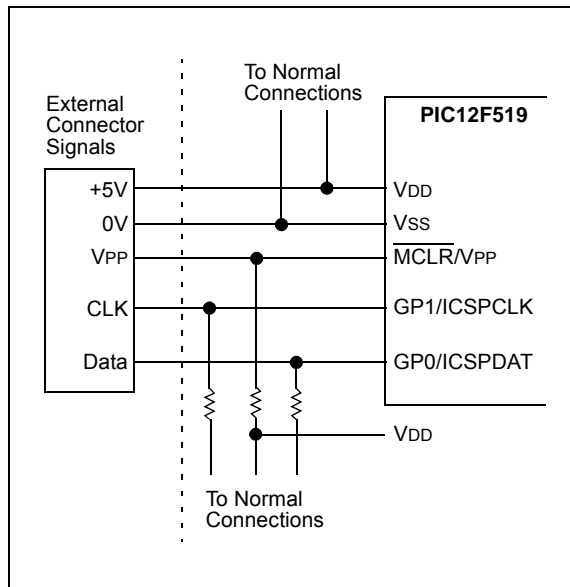
The PIC12F519 device can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground and the programming voltage. This allows users to manufacture boards with unprogrammed PIC12F519 device and then program the PIC12F519 device just before shipping the product. This also allows the most recent firmware, or a custom firmware, to be programmed.

The PIC12F519 device is placed into a Program/Verify mode by holding the GP1 and GP0 pins low while raising the MCLR (VPP) pin from VIL to VIH (see programming specification). The GP1 pin becomes the programming clock, and the GP0 pin becomes the programming data. Both GP1 and GP0 pins are Schmitt Trigger inputs in this mode.

After Reset, a 6-bit command is then supplied to the device. Depending on the command, 14 bits of program data are then supplied to or from the device, depending if the command was a Load or a Read. For complete details of serial programming, please refer to the "PIC12F519 Memory Programming Specification," (DS41316).

A typical In-Circuit Serial Programming connection is shown in Figure 8-12.

FIGURE 8-12: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



RETLW Return with Literal in W

Syntax: [*label*] RETLW *k*

Operands: $0 \leq k \leq 255$

Operation: $k \rightarrow (W)$;
TOS \rightarrow PC

Status Affected: None

Description: The W register is loaded with the eight-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

SLEEP Enter SLEEP Mode

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h \rightarrow WDT;
0 \rightarrow WDT prescaler;
1 \rightarrow \overline{TO} ;
0 \rightarrow PD

Status Affected: \overline{TO} , PD, GPWUF

Description: Time-out Status bit (\overline{TO}) is set. The Power-down Status bit (PD) is cleared.
GPWUF is unaffected.
The WDT and its prescaler are cleared.
The processor is put into Sleep mode with the oscillator stopped.
See **Section 8.8 "Power-down Mode (Sleep)"** on Sleep for more details.

RLF Rotate Left f through Carry

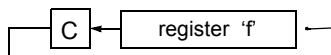
Syntax: [*label*] RLF *f*,*d*

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.



SUBWF Subtract W from f

Syntax: [*label*] SUBWF *f*,*d*

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(f) - (W) \rightarrow (\text{dest})$

Status Affected: C, DC, Z

Description: Subtract (two's complement method) the W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

RRF Rotate Right f through Carry

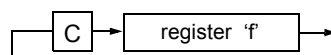
Syntax: [*label*] RRF *f*,*d*

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.



SWAPF Swap Nibbles in f

Syntax: [*label*] SWAPF *f*,*d*

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(f<3:0>) \rightarrow (\text{dest}<7:4>)$;
 $(f<7:4>) \rightarrow (\text{dest}<3:0>)$

Status Affected: None

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in W register. If 'd' is '1', the result is placed in register 'f'.

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TRIS Load TRIS Register

Syntax: [*label*] TRIS *f*
Operands: *f* = 6
Operation: (*W*) → TRIS register *f*
Status Affected: None
Description: TRIS register '*f*' (*f* = 6 or 7) is loaded with the contents of the *W* register.

XORLW Exclusive OR literal with W

Syntax: [*label*] XORLW *k*
Operands: $0 \leq k \leq 255$
Operation: (*W*) .XOR. *k* → (*W*)
Status Affected: Z
Description: The contents of the *W* register are XOR'ed with the eight-bit literal '*k*'. The result is placed in the *W* register.

XORWF Exclusive OR W with f

Syntax: [*label*] XORWF *f*,*d*
Operands: $0 \leq f \leq 31$
 d ∈ [0,1]
Operation: (*W*) .XOR. (*f*) → (*dest*)
Status Affected: Z
Description: Exclusive OR the contents of the *W* register with register '*f*'. If '*d*' is '0', the result is stored in the *W* register. If '*d*' is '1', the result is stored back in register '*f*'.

10.7 MPLAB ICE 2000 High-Performance In-Circuit Emulator

The MPLAB ICE 2000 In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers. Software control of the MPLAB ICE 2000 In-Circuit Emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The architecture of the MPLAB ICE 2000 In-Circuit Emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE 2000 In-Circuit Emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft® Windows® 32-bit operating system were chosen to best make these features available in a simple, unified application.

10.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC® and MCU devices. It debugs and programs PIC® and dsPIC® Flash microcontrollers with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The MPLAB REAL ICE probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with the popular MPLAB ICD 2 system (RJ11) or with the new high speed, noise tolerant, low-voltage differential signal (LVDS) interconnection (CAT5).

MPLAB REAL ICE is field upgradeable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added, such as software breakpoints and assembly code trace. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, real-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

10.9 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low-cost, run-time development tool, connecting to the host PC via an RS-232 or high-speed USB interface. This tool is based on the Flash PIC MCUs and can be used to develop for these and other PIC MCUs and dsPIC DSCs. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the Flash devices. This feature, along with Microchip's In-Circuit Serial Programming™ (ICSP™) protocol, offers cost-effective, in-circuit Flash debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single stepping and watching variables, and CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real time. MPLAB ICD 2 also serves as a development programmer for selected PIC devices.

10.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an SD/MMC card for file storage and secure data applications.

10.11 PICSTART Plus Development Programmer

The PICSTART Plus Development Programmer is an easy-to-use, low-cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus Development Programmer supports most PIC devices in DIP packages up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus Development Programmer is CE compliant.

10.12 PICkit 2 Development Programmer

The PICkit™ 2 Development Programmer is a low-cost programmer and selected Flash device debugger with an easy-to-use interface for programming many of Microchip's baseline, mid-range and PIC18F families of Flash memory microcontrollers. The PICkit 2 Starter Kit includes a prototyping development board, twelve sequential lessons, software and HI-TECH's PICC™ Lite C compiler, and is designed to help get up to speed quickly using PIC® microcontrollers. The kit provides everything needed to program, evaluate and develop applications using Microchip's powerful, mid-range Flash memory family of microcontrollers.

10.13 Demonstration, Development and Evaluation Boards

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Check the Microchip web page (www.microchip.com) and the latest "Product Selector Guide" (DS00148) for the complete list of demonstration, development and evaluation kits.

PIC12F519

11.3 AC Characteristics

TABLE 11-5: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial), $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) Operating Voltage V_{DD} range is described in Section 11.0 “Electrical Characteristics”				
Param No.	Sym.	Characteristic	Min.	Typ ⁽¹⁾	Max.	Units	Conditions
1A	FOSC	External CLKIN Frequency ⁽²⁾	DC	—	4	MHz	XT Oscillator mode
			DC	—	200	kHz	LP Oscillator mode
		Oscillator Frequency ⁽²⁾	DC	—	4	MHz	EXTRC Oscillator mode
			0.1	—	4	MHz	XT Oscillator mode
1	TOSC	External CLKIN Period ⁽²⁾	DC	—	200	kHz	LP Oscillator mode
			250	—	—	ns	XT Oscillator mode
		Oscillator Period ⁽²⁾	5	—	—	μs	LP Oscillator mode
			250	—	—	ns	EXTRC Oscillator mode
2	Tcy	Instruction Cycle Time	250	—	10,000	ns	XT Oscillator mode
			5	—	—	μs	LP Oscillator mode
3	TosL, TosH	Clock in (OSC1) Low or High Time	200	4/FOSC	DC	ns	
			50*	—	—	ns	XT Oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	—	μs	LP Oscillator
			—	—	25*	ns	XT Oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	50*	ns	LP Oscillator
			—	—	—	ns	LP Oscillator

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- 2:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the “max” cycle time limit is “DC” (no clock) for all devices.

TABLE 11-6: CALIBRATED INTERNAL RC FREQUENCIES

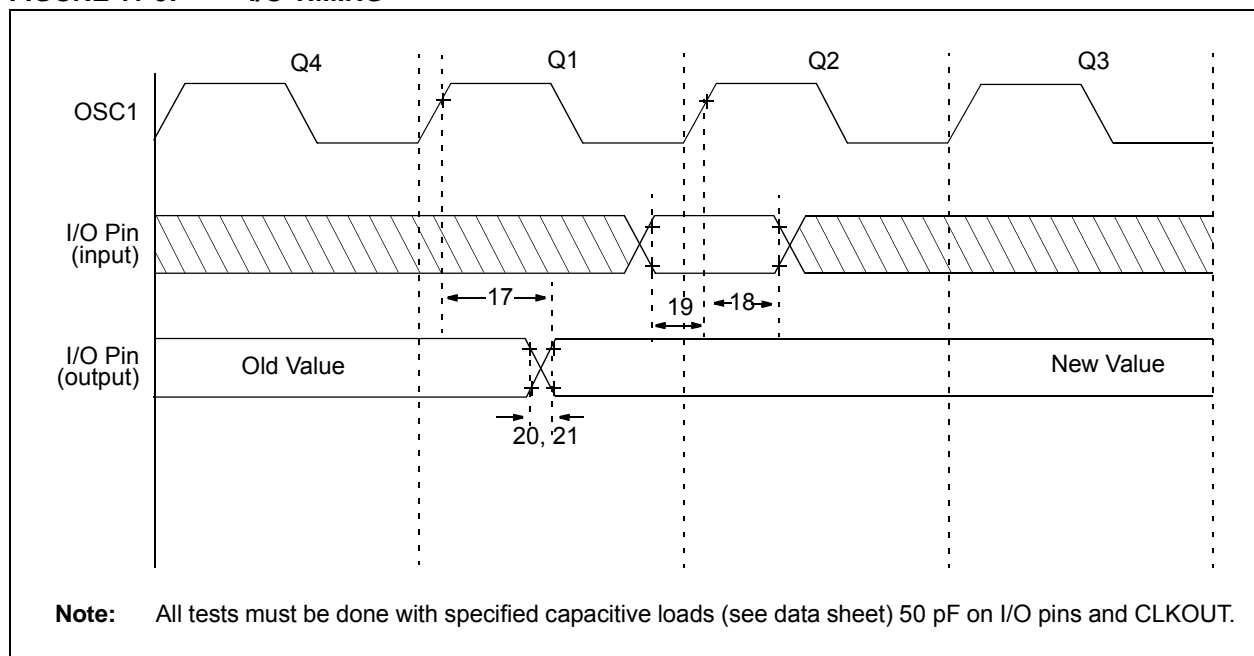
AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified)					
			Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial), $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended)					
			Operating Voltage V_{DD} range is described in Section 10.1					
Param No.	Sym.	Characteristic	Freq. Tolerance	Min.	Typ†	Max.	Units	Conditions
F10	FOSC	Internal Calibrated INTOSC Frequency ⁽¹⁾	$\pm 1\%$	7.92	8.00	8.08	MHz	3.5V, 25°C
			$\pm 2\%$	7.84	8.00	8.16	MHz	$2.5\text{V} \leq V_{DD} \leq 5.5\text{V}$ $0^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$
			$\pm 5\%$	7.60	8.00	8.40	MHz	$2.0\text{V} \leq V_{DD} \leq 5.5\text{V}$ $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (Ind.) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (Ext.)

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: To ensure these oscillator frequency tolerances, V_{DD} and V_{SS} must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

FIGURE 11-5: I/O TIMING



12.0 DC AND AC CHARACTERISTICS GRAPHS AND CHARTS

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified V_{DD} range). This is for **information only** and devices are ensured to operate properly only within the specified range.

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

“Typical” represents the mean of the distribution at 25°C. “Maximum” or “minimum” represents (mean + 3 σ) or (mean - 3 σ) respectively, where σ is a standard deviation, over each temperature range.

FIGURE 12-1: TYPICAL I_{DD} vs. F_{osc} OVER V_{DD} (XT, EXTRC mode)

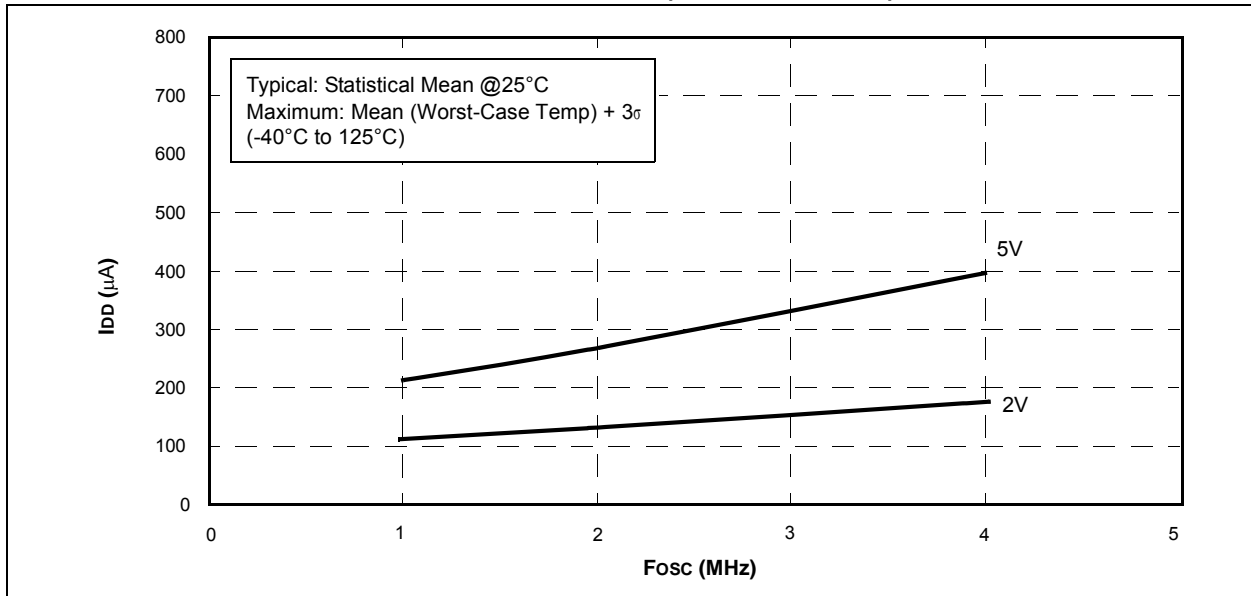
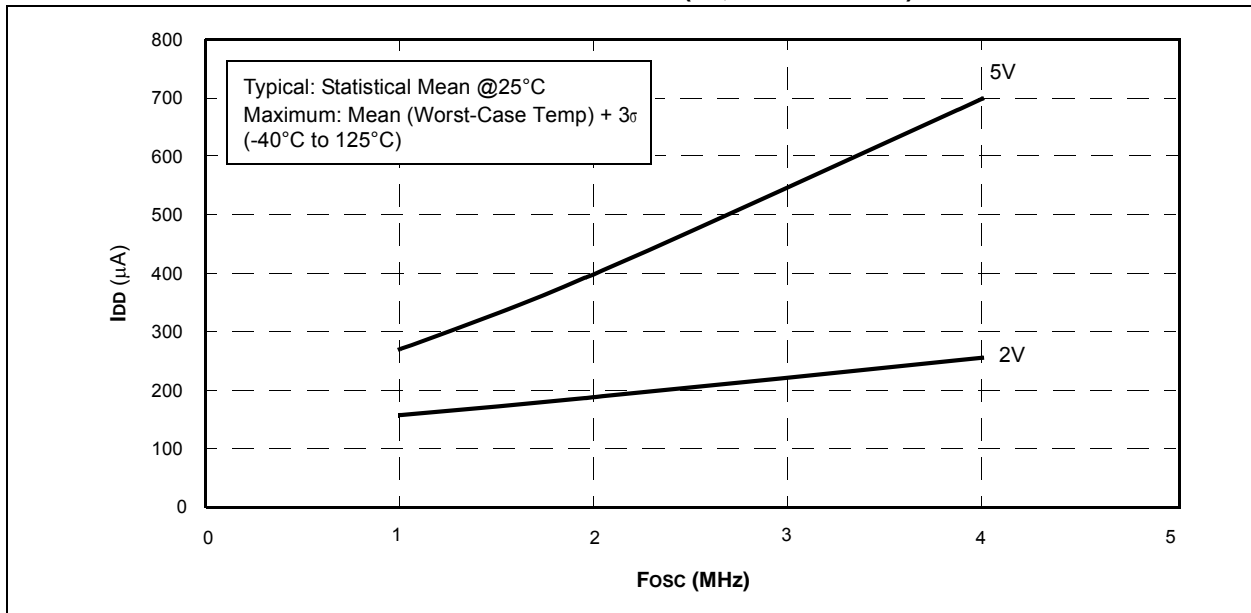


FIGURE 12-2: MAXIMUM I_{DD} vs. F_{osc} OVER V_{DD} (XT, EXTRC mode)



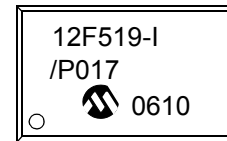
13.0 PACKAGING INFORMATION

13.1 Package Marking Information

8-Lead PDIP



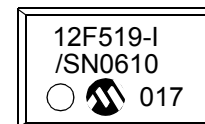
Example



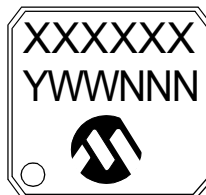
8-Lead SOIC (3.90 mm)



Example



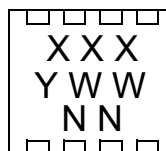
8-Lead MSOP



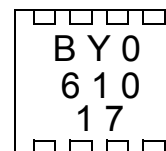
Example



8-Lead 2x3 DFN*



Example



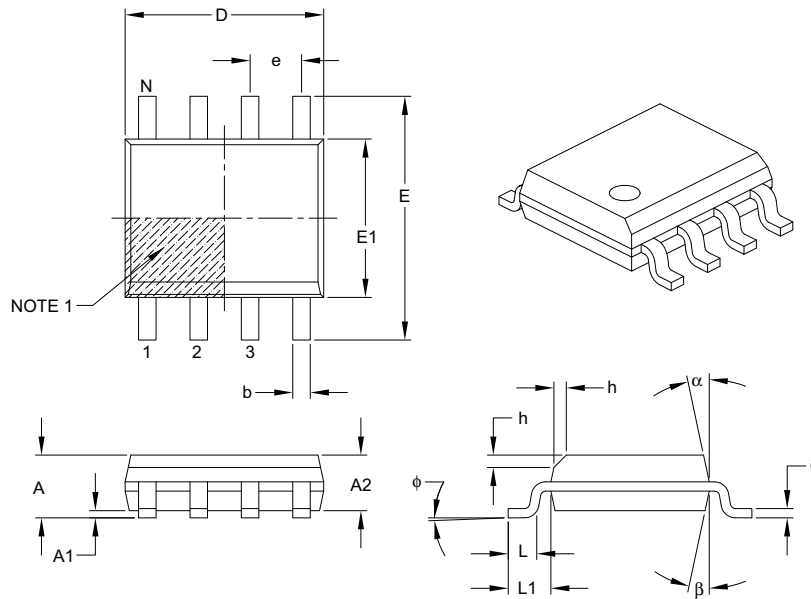
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

* Standard PIC® device marking consists of Microchip part number, year code, week code, and traceability code. For PIC device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

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