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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

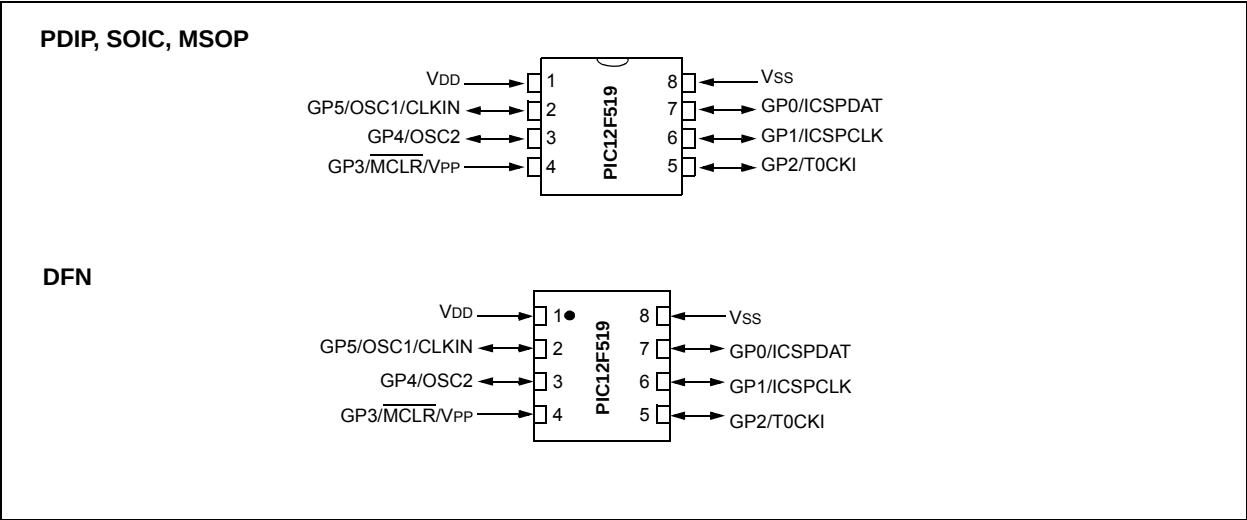
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |                                                                                                                                                                 |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Active                                                                                                                                                          |
| Core Processor             | PIC                                                                                                                                                             |
| Core Size                  | 8-Bit                                                                                                                                                           |
| Speed                      | 8MHz                                                                                                                                                            |
| Connectivity               | -                                                                                                                                                               |
| Peripherals                | POR, WDT                                                                                                                                                        |
| Number of I/O              | 5                                                                                                                                                               |
| Program Memory Size        | 1.5KB (1K x 12)                                                                                                                                                 |
| Program Memory Type        | FLASH                                                                                                                                                           |
| EEPROM Size                | -                                                                                                                                                               |
| RAM Size                   | 41 x 8                                                                                                                                                          |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 5.5V                                                                                                                                                       |
| Data Converters            | -                                                                                                                                                               |
| Oscillator Type            | Internal                                                                                                                                                        |
| Operating Temperature      | -40°C ~ 85°C (TA)                                                                                                                                               |
| Mounting Type              | Surface Mount                                                                                                                                                   |
| Package / Case             | 8-TSSOP, 8-MSOP (0.118", 3.00mm Width)                                                                                                                          |
| Supplier Device Package    | 8-MSOP                                                                                                                                                          |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/microchip-technology/pic12f519-i-ms">https://www.e-xfl.com/product-detail/microchip-technology/pic12f519-i-ms</a> |

# PIC12F519

FIGURE 1: PIC12F519 8-PIN PDIP, SOIC, MSOP, 2X3 DFN DIAGRAM



| Device    | Program Memory | Data Memory  |               | I/O | Timers 8-bit |
|-----------|----------------|--------------|---------------|-----|--------------|
|           | Flash (words)  | SRAM (bytes) | Flash (bytes) |     |              |
| PIC12F519 | 1024           | 41           | 64            | 6   | 1            |

# PIC12F519

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NOTES:

# PIC12F519

**FIGURE 3-1: PIC12F519 ARCHITECTURAL BLOCK DIAGRAM**

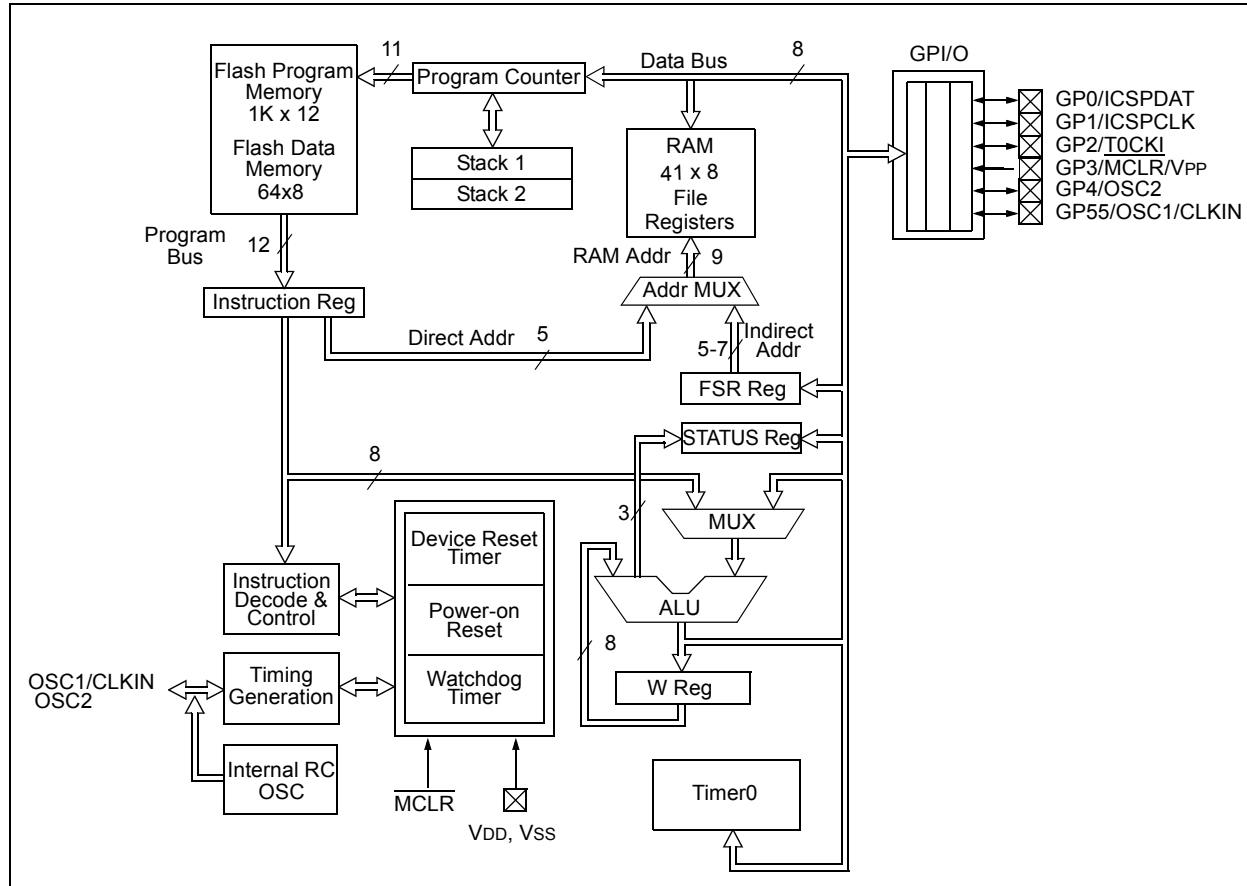


FIGURE 6-5: GP3 (WITH WEAK PULL-UP AND WAKE-UP ON CHANGE)

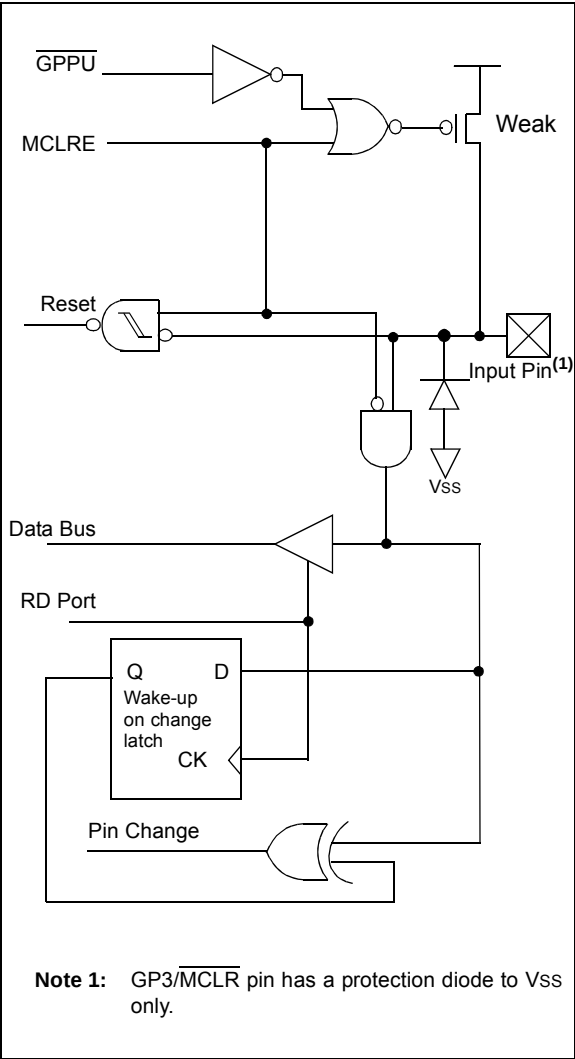


TABLE 6-2: SUMMARY OF PORT REGISTERS

| Name     | Bit 7             | Bit 6             | Bit 5     | Bit 4           | Bit 3           | Bit 2     | Bit 1     | Bit 0     | Value on POR | Value on all other Resets |
|----------|-------------------|-------------------|-----------|-----------------|-----------------|-----------|-----------|-----------|--------------|---------------------------|
| GPIO     | —                 | —                 | GP5       | GP4             | GP3             | GP2       | GP1       | GP0       | --xx xxxx    | --uu uuuu                 |
| TRISGPIO | —                 | —                 | TRISGPIO5 | TRISGPIO4       | TRISGPIO3       | TRISGPIO2 | TRISGPIO1 | TRISGPIO0 | --11 1111    | --11 1111                 |
| STATUS   | GPWUF             | —                 | PA0       | $\overline{TO}$ | $\overline{PD}$ | Z         | DC        | C         | 0-01 1xxx    | q-0q quuu                 |
| OPTION   | $\overline{GPWU}$ | $\overline{GPPU}$ | T0CS      | T0SE            | PSA             | PS2       | PS1       | PS0       | 1111 1111    | 1111 1111                 |

**Legend:** x = unknown, u = unchanged, — = unimplemented, read as '0', Shaded cells = unimplemented, read as '0', q = depends on the condition

## 7.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

### 7.1.1 EXTERNAL CLOCK SYNCHRONIZATION

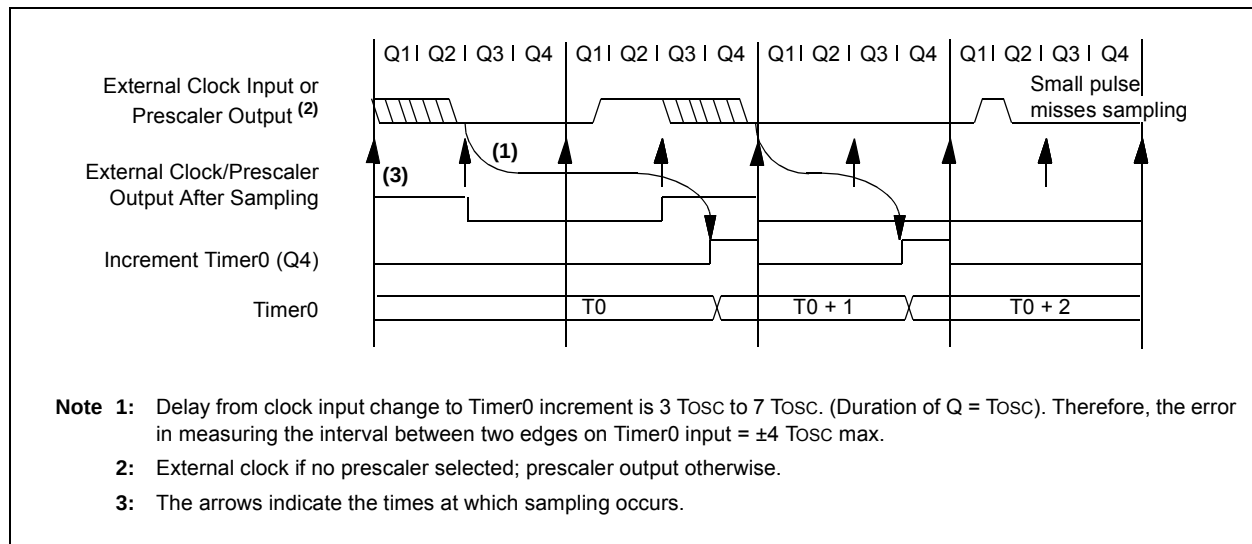
When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 7-4). Therefore, it is necessary for T0CKI to be high for at least 2 Tosc (and a small RC delay of 2 Tt0H) and low for at least 2 Tosc (and a small RC delay of 2 Tt0H). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler, so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4 Tosc (and a small RC delay of 4 Tt0H) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of Tt0H. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

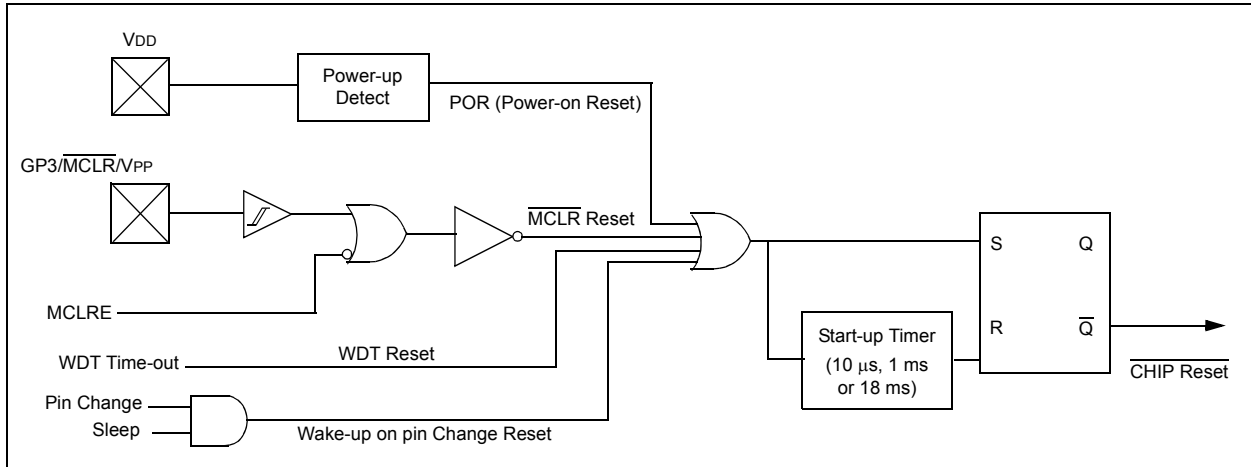
### 7.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 7-4 shows the delay from the external clock edge to the timer incrementing.

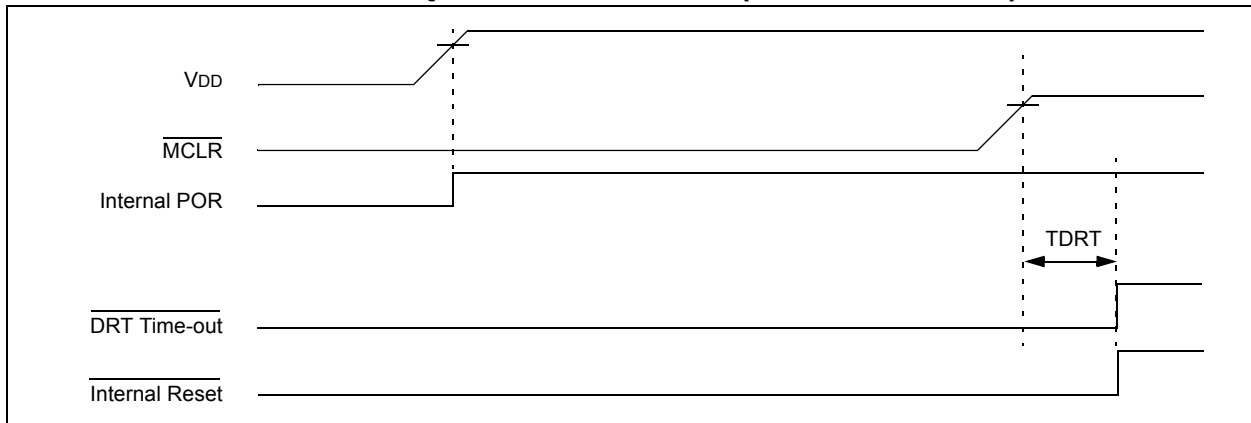
**FIGURE 7-4: TIMER0 TIMING WITH EXTERNAL CLOCK**



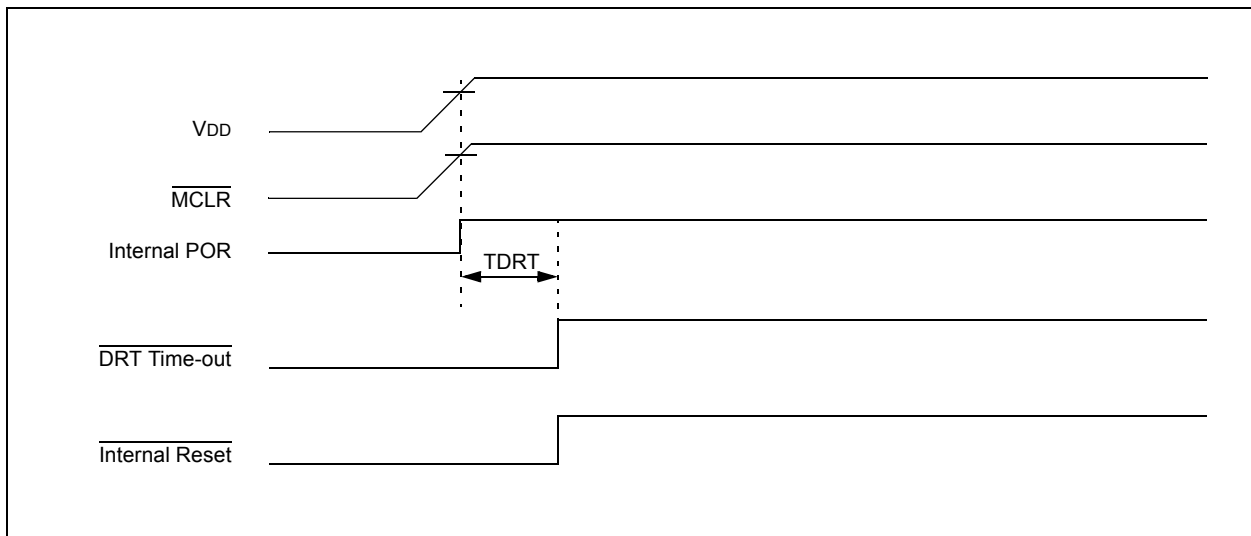
**FIGURE 8-7: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT**



**FIGURE 8-8: TIME-OUT SEQUENCE ON POWER-UP ( $\overline{\text{MCLR}}$  PULLED LOW)**



**FIGURE 8-9: TIME-OUT SEQUENCE ON POWER-UP ( $\overline{\text{MCLR}}$  TIED TO VDD): FAST VDD RISE TIME**



## 8.5 Device Reset Timer (DRT)

On the PIC12F519 device, the DRT runs any time the device is powered up. DRT runs from Reset and varies based on oscillator selection and Reset type (see Table 8-5).

The DRT operates on an internal RC oscillator. The processor is kept in Reset as long as the DRT is active. The DRT delay allows VDD to rise above VDD min. and for the oscillator to stabilize.

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the devices in a Reset condition after MCLR has reached a logic high (VIH MCLR) level. Programming GP3/MCLR/VPP as MCLR and using an external RC network connected to the MCLR input is not required in most cases. This allows savings in cost-sensitive and/or space restricted applications, as well as allowing the use of the GP3/MCLR/VPP pin as a general purpose input.

The Device Reset Time delays will vary from chip-to-chip due to VDD, temperature and process variation. See AC parameters for details.

The DRT will also be triggered upon a Watchdog Timer time-out from Sleep. This is particularly important for applications using the WDT to wake from Sleep mode automatically.

Reset sources are POR, MCLR, WDT time-out and wake-up on pin change. See Section 8.8.2 "Wake-up from Sleep", Notes 1, 2 and 3.

**TABLE 8-5: DRT (DEVICE RESET TIMER PERIOD)**

| Oscillator Configuration | POR Reset       | Subsequent Resets |
|--------------------------|-----------------|-------------------|
| INTOSC, EXTRC            | 1 ms (typical)  | 10 μs (typical)   |
| LP, XT                   | 18 ms (typical) | 18 ms (typical)   |

## 8.6 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator, which does not require any external components. This RC oscillator is separate from the external RC oscillator of the (GP5)/OSC1/CLKIN pin and the internal 4 or 8 MHz oscillator. This means that the WDT will run even if the main processor clock has been stopped, for example, by execution of a SLEEP instruction. During normal operation or Sleep, a WDT Reset or wake-up Reset, generates a device Reset.

The TO bit (STATUS<4>) will be cleared upon a Watchdog Timer Reset.

The WDT can be permanently disabled by programming the configuration WDTE as a '0' (see Section 8.1 "Configuration Bits"). Refer to the PIC12F519 Programming Specification (DS41316) to determine how to access the Configuration Word.

### 8.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, a time-out period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see DC specs).

Under worst-case conditions (VDD = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

### 8.6.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDI instruction clears the WDT and the postscaler, if assigned to the WDT, and prevents it from timing out and generating a device Reset.

The SLEEP instruction resets the WDT and the postscaler, if assigned to the WDT. This gives the maximum Sleep time before a WDT wake-up Reset.

# PIC12F519

FIGURE 8-11: WATCHDOG TIMER BLOCK DIAGRAM

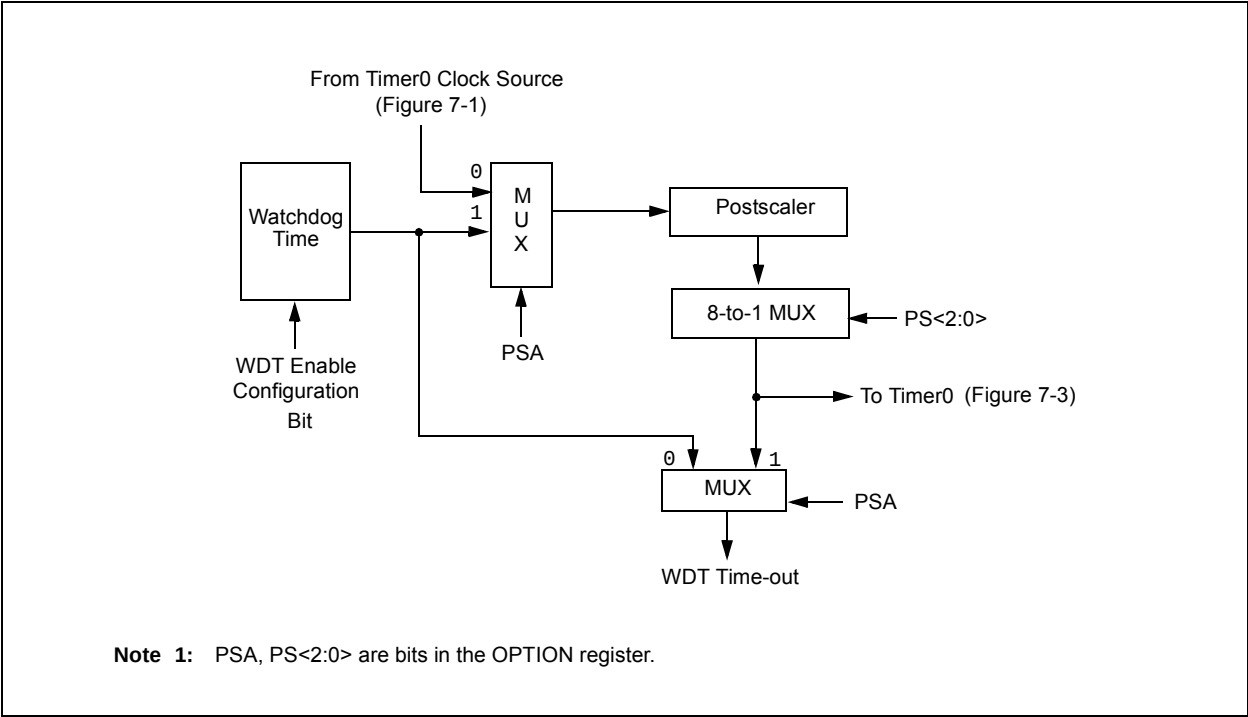


TABLE 8-6: SUMMARY OF REGISTER ASSOCIATED WITH THE WATCHDOG TIMER

| Name   | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------------------|---------------------------|
| OPTION | GPWU  | GPPU  | T0CS  | T0SE  | PSA   | PS2   | PS1   | PS0   | 1111 1111         | 1111 1111                 |

Legend: Shaded boxes = Not used by Watchdog Timer.

## 9.0 INSTRUCTION SET SUMMARY

The PIC12F519 instruction set is highly orthogonal and is comprised of three basic categories.

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC12F519 instruction is a 12-bit word divided into an **opcode**, which specifies the instruction type, and one or more **operands** which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 9-1, while the various opcode fields are summarized in Table 9-1.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

**TABLE 9-1: OPCODE FIELD DESCRIPTIONS**

| Field           | Description                                                                                                                                                           |
|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| f               | Register file address (0x00 to 0x7F)                                                                                                                                  |
| W               | Working register (accumulator)                                                                                                                                        |
| b               | Bit address within an 8-bit file register                                                                                                                             |
| k               | Literal field, constant data or label                                                                                                                                 |
| x               | Don't care location (= 0 or 1)<br>The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools. |
| d               | Destination select;<br>d = 0 (store result in W)<br>d = 1 (store result in file register 'f')<br>Default is d = 1                                                     |
| label           | Label name                                                                                                                                                            |
| TOS             | Top-of-Stack                                                                                                                                                          |
| PC              | Program Counter                                                                                                                                                       |
| WDT             | Watchdog Timer counter                                                                                                                                                |
| $\overline{TO}$ | Time-out bit                                                                                                                                                          |
| PD              | Power-down bit                                                                                                                                                        |
| dest            | Destination, either the W register or the specified register file location                                                                                            |
| [ ]             | Options                                                                                                                                                               |
| ( )             | Contents                                                                                                                                                              |
| →               | Assigned to                                                                                                                                                           |
| < >             | Register bit field                                                                                                                                                    |
| ∈               | In the set of                                                                                                                                                         |
| <i>italics</i>  | User defined term (font is courier)                                                                                                                                   |

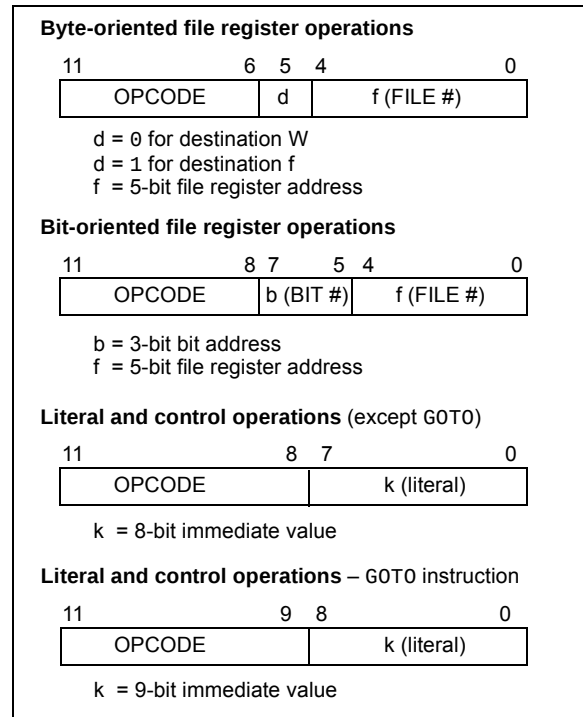
All instructions are executed within a single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1  $\mu$ s. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2  $\mu$ s.

Figure 9-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

**FIGURE 9-1: GENERAL FORMAT FOR INSTRUCTIONS**



# PIC12F519

**TABLE 9-2: INSTRUCTION SET SUMMARY**

| Mnemonic,<br>Operands                 |      | Description                  | Cycles           | 12-Bit Opcode |      |      | Status<br>Affected | Notes   |
|---------------------------------------|------|------------------------------|------------------|---------------|------|------|--------------------|---------|
|                                       |      |                              |                  | MSb           | LSb  |      |                    |         |
| ADDWF                                 | f, d | Add W and f                  | 1                | 0001          | 11df | ffff | C, DC, Z           | 1, 2, 4 |
| ANDWF                                 | f, d | AND W with f                 | 1                | 0001          | 01df | ffff | Z                  | 2, 4    |
| CLRF                                  | f    | Clear f                      | 1                | 0000          | 011f | ffff | Z                  | 4       |
| CLRW                                  | —    | Clear W                      | 1                | 0000          | 0100 | 0000 | Z                  |         |
| COMF                                  | f, d | Complement f                 | 1                | 0010          | 01df | ffff | Z                  |         |
| DECF                                  | f, d | Decrement f                  | 1                | 0000          | 11df | ffff | Z                  | 2, 4    |
| DECFSZ                                | f, d | Decrement f, Skip if 0       | 1 <sup>(2)</sup> | 0010          | 11df | ffff | None               | 2, 4    |
| INCF                                  | f, d | Increment f                  | 1                | 0010          | 10df | ffff | Z                  | 2, 4    |
| INCFSZ                                | f, d | Increment f, Skip if 0       | 1 <sup>(2)</sup> | 0011          | 11df | ffff | None               | 2, 4    |
| IORWF                                 | f, d | Inclusive OR W with f        | 1                | 0001          | 00df | ffff | Z                  | 2, 4    |
| MOVF                                  | f, d | Move f                       | 1                | 0010          | 00df | ffff | Z                  | 2, 4    |
| MOVWF                                 | f    | Move W to f                  | 1                | 0000          | 001f | ffff | None               | 1, 4    |
| NOP                                   | —    | No Operation                 | 1                | 0000          | 0000 | 0000 | None               |         |
| RLF                                   | f, d | Rotate left f through Carry  | 1                | 0011          | 01df | ffff | C                  | 2, 4    |
| RRF                                   | f, d | Rotate right f through Carry | 1                | 0011          | 00df | ffff | C                  | 2, 4    |
| SUBWF                                 | f, d | Subtract W from f            | 1                | 0000          | 10df | ffff | C, DC, Z           | 1, 2, 4 |
| SWAPF                                 | f, d | Swap f                       | 1                | 0011          | 10df | ffff | None               | 2, 4    |
| XORWF                                 | f, d | Exclusive OR W with f        | 1                | 0001          | 10df | ffff | Z                  | 2, 4    |
| BIT-ORIENTED FILE REGISTER OPERATIONS |      |                              |                  |               |      |      |                    |         |
| BCF                                   | f, b | Bit Clear f                  | 1                | 0100          | bbbf | ffff | None               | 2, 4    |
| BSF                                   | f, b | Bit Set f                    | 1                | 0101          | bbbf | ffff | None               | 2, 4    |
| BTFSC                                 | f, b | Bit Test f, Skip if Clear    | 1 <sup>(2)</sup> | 0110          | bbbf | ffff | None               |         |
| BTFSS                                 | f, b | Bit Test f, Skip if Set      | 1 <sup>(2)</sup> | 0111          | bbbf | ffff | None               |         |
| LITERAL AND CONTROL OPERATIONS        |      |                              |                  |               |      |      |                    |         |
| ANDLW                                 | k    | AND literal with W           | 1                | 1110          | kkkk | kkkk | Z                  |         |
| CALL                                  | k    | Call Subroutine              | 2                | 1001          | kkkk | kkkk | None               | 1       |
| CLRWDT                                | —    | Clear Watchdog Timer         | 1                | 0000          | 0000 | 0100 | TO, PD             |         |
| GOTO                                  | k    | Unconditional branch         | 2                | 101k          | kkkk | kkkk | None               |         |
| IORLW                                 | k    | Inclusive OR literal with W  | 1                | 1101          | kkkk | kkkk | Z                  |         |
| MOVLW                                 | k    | Move literal to W            | 1                | 1100          | kkkk | kkkk | None               |         |
| OPTION                                | —    | Load OPTION register         | 1                | 0000          | 0000 | 0010 | None               |         |
| RETLW                                 | k    | Return, place literal in W   | 2                | 1000          | kkkk | kkkk | None               |         |
| SLEEP                                 | —    | Go into Standby mode         | 1                | 0000          | 0000 | 0011 | TO, PD             |         |
| TRISGPIO                              | f    | Load TRISGPIO register       | 1                | 0000          | 0000 | 0fff | None               | 3       |
| XORLW                                 | k    | Exclusive OR literal to W    | 1                | 1111          | kkkk | kkkk | Z                  |         |

**Note 1:** The 9th bit of the program counter will be forced to a '0' by any instruction that writes to the PC except for GOTO. See **Section 4.6 "Program Counter"**.

- When an I/O register is modified as a function of itself (e.g. MOVF GPIO, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- The instruction TRIS f, where f = 6, causes the contents of the W register to be written to the tri-state latches of GPIO. A '1' forces the pin to a high-impedance state and disables the output buffers.
- If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared (if assigned to TMR0).

# PIC12F519

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---

**IORWF**      **Inclusive OR W with f**

---

Syntax:      [ *label* ]   IORWF   f,d

Operands:     $0 \leq f \leq 31$   
               $d \in [0,1]$

Operation:    (W).OR. (f)  $\rightarrow$  (dest)

Status Affected: Z

Description:   Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

---

**MOVWF**      **Move W to f**

---

Syntax:      [ *label* ]   MOVWF   f

Operands:     $0 \leq f \leq 31$

Operation:    (W)  $\rightarrow$  (f)

Status Affected: None

Description:   Move data from the W register to register 'f'.

---

**MOVF**      **Move f**

---

Syntax:      [ *label* ]   MOVF   f,d

Operands:     $0 \leq f \leq 31$   
               $d \in [0,1]$

Operation:    (f)  $\rightarrow$  (dest)

Status Affected: Z

Description:   The contents of register 'f' are moved to destination 'd'. If 'd' is '0', destination is the W register. If 'd' is '1', the destination is file register 'f'. 'd' = 1 is useful as a test of a file register, since status flag Z is affected.

---

**NOP**      **No Operation**

---

Syntax:      [ *label* ]   NOP

Operands:    None

Operation:    No operation

Status Affected: None

Description:   No operation.

---

**MOVLW**      **Move Literal to W**

---

Syntax:      [ *label* ]   MOVLW   k

Operands:     $0 \leq k \leq 255$

Operation:     $k \rightarrow$  (W)

Status Affected: None

Description:   The eight-bit literal 'k' is loaded into the W register. The "don't cares" will assembled as '0's.

---

**OPTION**      **Load OPTION Register**

---

Syntax:      [ *label* ]   OPTION

Operands:    None

Operation:    (W)  $\rightarrow$  Option

Status Affected: None

Description:   The content of the W register is loaded into the OPTION register.

## 10.2 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for all PIC MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

## 10.3 MPLAB C18 and MPLAB C30 C Compilers

The MPLAB C18 and MPLAB C30 Code Development Systems are complete ANSI C compilers for Microchip's PIC18 and PIC24 families of microcontrollers and the dsPIC30 and dsPIC33 family of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

## 10.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

## 10.5 MPLAB ASM30 Assembler, Linker and Librarian

MPLAB ASM30 Assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire dsPIC30F instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

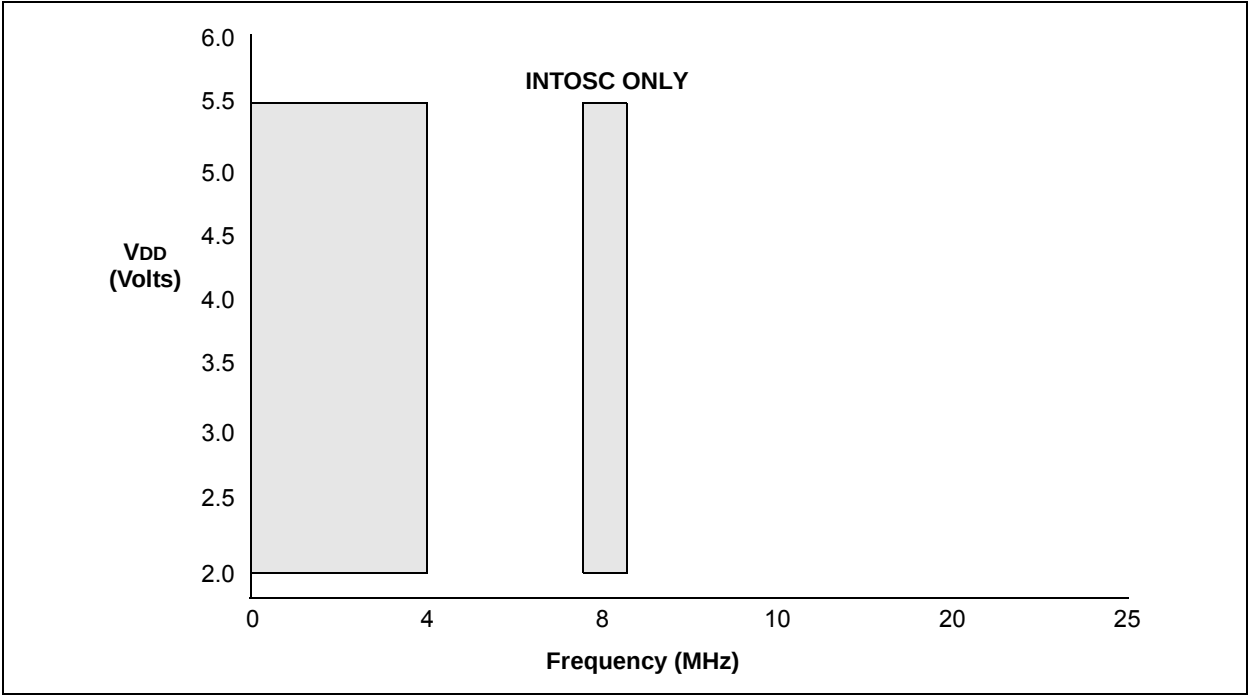
## 10.6 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

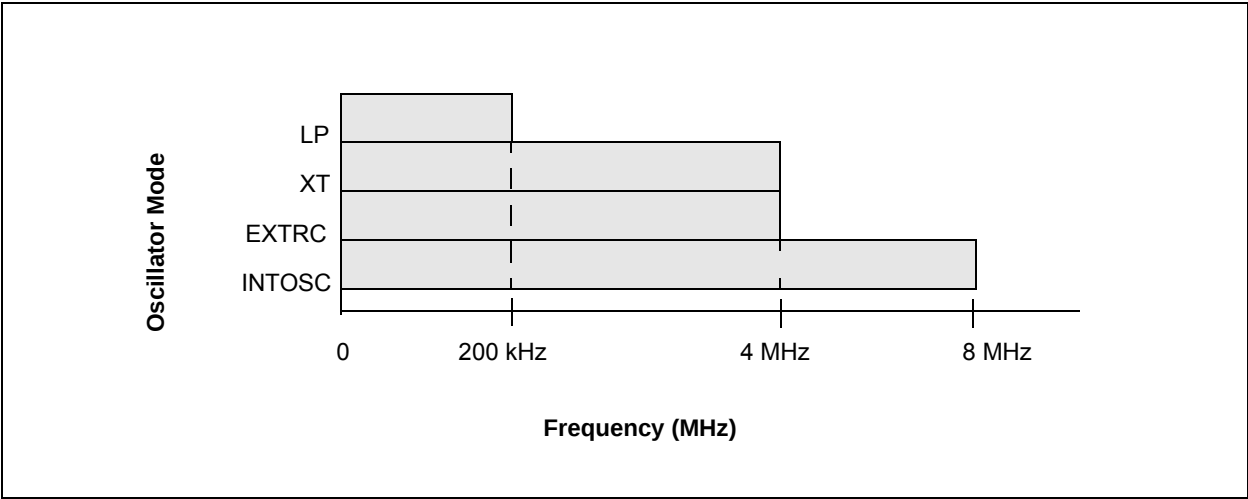
The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C18 and MPLAB C30 C Compilers, and the MPASM and MPLAB ASM30 Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

# PIC12F519

**FIGURE 11-1: PIC12F519 VOLTAGE-FREQUENCY GRAPH,  $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$**



**FIGURE 11-2: MAXIMUM OSCILLATOR FREQUENCY TABLE**



# PIC12F519

TABLE 11-4: PULL-UP RESISTOR RANGES

| V <sub>DD</sub> (Volts) | Temperature (°C) | Min. | Typ. | Max. | Units |
|-------------------------|------------------|------|------|------|-------|
| <b>GP0/GP1</b>          |                  |      |      |      |       |
| 2.0                     | –40              | 73K  | 105K | 186K | Ω     |
|                         | 25               | 73K  | 113K | 187K | Ω     |
|                         | 85               | 82K  | 123K | 190K | Ω     |
|                         | 125              | 86K  | 132K | 190K | Ω     |
| 5.5                     | –40              | 15K  | 21K  | 33K  | Ω     |
|                         | 25               | 15K  | 22K  | 34K  | Ω     |
|                         | 85               | 19K  | 26K  | 35K  | Ω     |
|                         | 125              | 23K  | 29K  | 35K  | Ω     |
| <b>GP3</b>              |                  |      |      |      |       |
| 2.0                     | –40              | 63K  | 81K  | 96K  | Ω     |
|                         | 25               | 77K  | 93K  | 116K | Ω     |
|                         | 85               | 82K  | 96K  | 116K | Ω     |
|                         | 125              | 86K  | 100K | 119K | Ω     |
| 5.5                     | –40              | 16K  | 20K  | 22K  | Ω     |
|                         | 25               | 16K  | 21K  | 23K  | Ω     |
|                         | 85               | 24K  | 25K  | 28K  | Ω     |
|                         | 125              | 26K  | 27K  | 29K  | Ω     |

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**TABLE 11-7: TIMING REQUIREMENTS**

| AC CHARACTERISTICS |          | Standard Operating Conditions (unless otherwise specified)                                                                                                        |      |                    |      |       |
|--------------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|--------------------|------|-------|
|                    |          | Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial)<br>$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) |      |                    |      |       |
|                    |          | Operating Voltage $V_{DD}$ range is described in                                                                                                                  |      |                    |      |       |
| Param No.          | Sym.     | Characteristic                                                                                                                                                    | Min. | Typ <sup>(1)</sup> | Max. | Units |
| 17                 | TosH2IoV | OSC1 $\uparrow$ (Q1 cycle) to Port Out Valid <sup>(2), (3)</sup>                                                                                                  | —    | —                  | 100* | ns    |
| 18                 | TosH2IoI | OSC1 $\uparrow$ (Q2 cycle) to Port Input Invalid (I/O in hold time) <sup>(2)</sup>                                                                                | 50   | —                  | —    | ns    |
| 19                 | TioV2osH | Port Input Valid to OSC1 $\uparrow$ (I/O in setup time)                                                                                                           | 20   | —                  | —    | ns    |
| 20                 | TioR     | Port Output Rise Time <sup>(3)</sup>                                                                                                                              | —    | 10                 | 50** | ns    |
| 21                 | TioF     | Port Output Fall Time <sup>(3)</sup>                                                                                                                              | —    | 10                 | 50** | ns    |

TBD = To be determined.

\* These parameters are characterized but not tested.

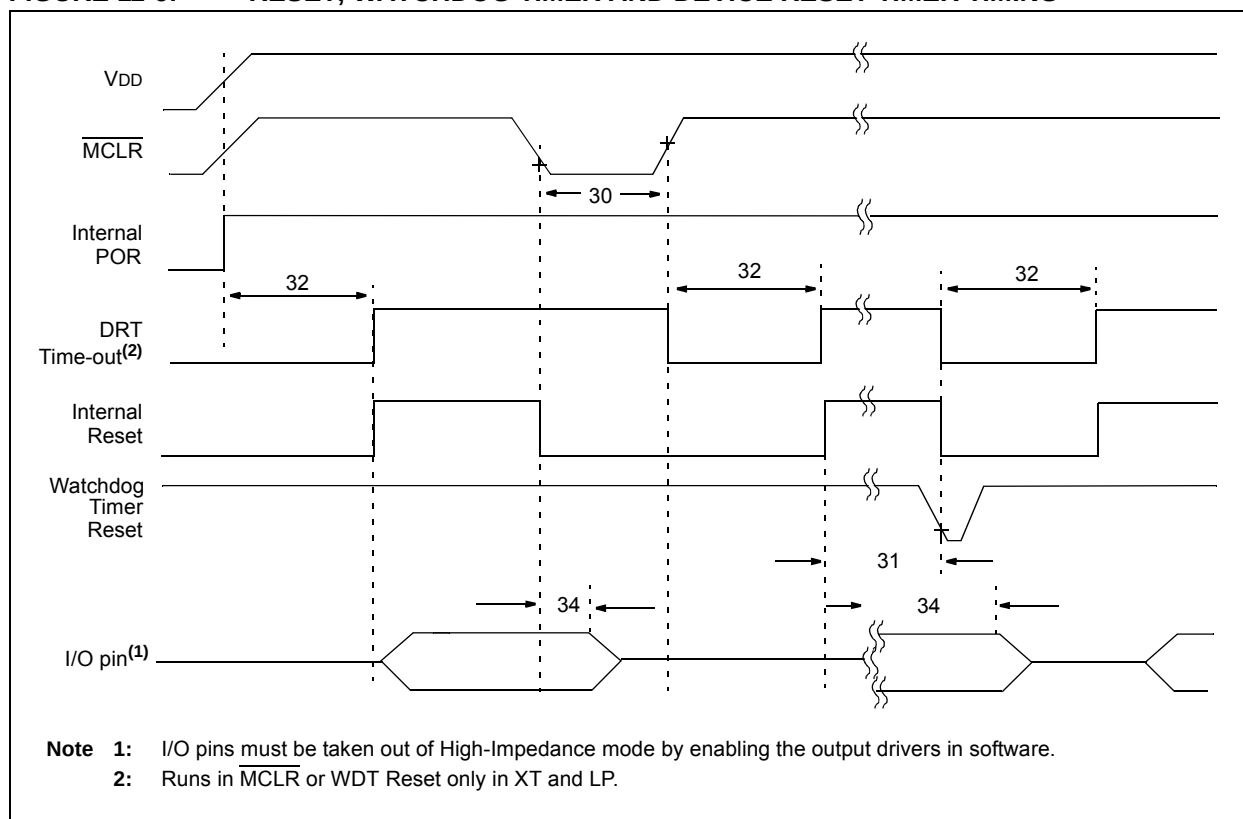
\*\* These parameters are design targets and are not tested.

**Note 1:** Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**2:** Measurements are taken in EXTRC mode.

**3:** See Figure 11-3 for loading conditions.

**FIGURE 11-6: RESET, WATCHDOG TIMER AND DEVICE RESET TIMER TIMING**



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**TABLE 11-10: TIMER0 CLOCK REQUIREMENTS**

| AC CHARACTERISTICS |      |                        |                | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial)<br>$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended)<br>Operating Voltage $V_{DD}$ range is described in<br><b>Section TABLE 11-3: “DC CHARACTERISTICS: PIC12F519 (Industrial, Extended)”</b> |                    |      |       |                                                                             |
|--------------------|------|------------------------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|------|-------|-----------------------------------------------------------------------------|
| Param No.          | Sym. | Characteristic         |                | Min.                                                                                                                                                                                                                                                                                                                                                                     | Typ <sup>(1)</sup> | Max. | Units | Conditions                                                                  |
| 40                 | Tt0H | T0CKI High Pulse Width | No Prescaler   | $0.5 T_{CY} + 20^*$                                                                                                                                                                                                                                                                                                                                                      | —                  | —    | ns    |                                                                             |
|                    |      |                        | With Prescaler | $10^*$                                                                                                                                                                                                                                                                                                                                                                   | —                  | —    | ns    |                                                                             |
| 41                 | Tt0L | T0CKI Low Pulse Width  | No Prescaler   | $0.5 T_{CY} + 20^*$                                                                                                                                                                                                                                                                                                                                                      | —                  | —    | ns    |                                                                             |
|                    |      |                        | With Prescaler | $10^*$                                                                                                                                                                                                                                                                                                                                                                   | —                  | —    | ns    |                                                                             |
| 42                 | Tt0P | T0CKI Period           |                | $20 \text{ or } T_{CY} + 40^* N$                                                                                                                                                                                                                                                                                                                                         | —                  | —    | ns    | Whichever is greater.<br>$N = \text{Prescale Value}$<br>(1, 2, 4, ..., 256) |

\* These parameters are characterized but not tested.

**Note 1:** Data in the Typical (“Typ”) column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

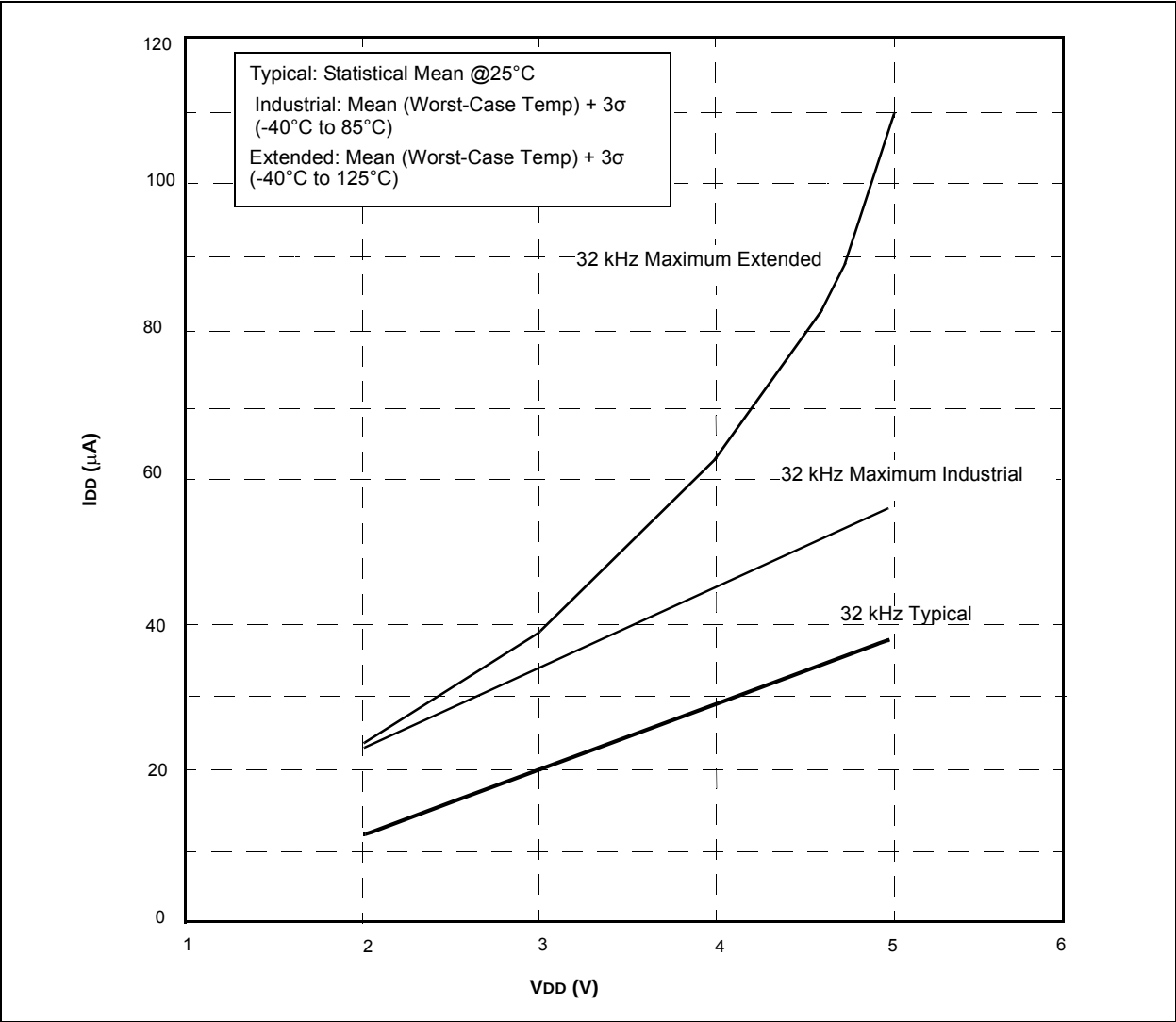
**TABLE 11-11: FLASH DATA MEMORY WRITE/ERASE REQUIREMENTS**

| AC CHARACTERISTICS |                 |                                    | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial)<br>$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended)<br>Operating Voltage $V_{DD}$ range is described in<br><b>Section TABLE 11-3: “DC CHARACTERISTICS: PIC12F519 (Industrial, Extended)”</b> |                    |      |       |            |
|--------------------|-----------------|------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|------|-------|------------|
| Param No.          | Sym.            | Characteristic                     | Min.                                                                                                                                                                                                                                                                                                                                                                     | Typ <sup>(1)</sup> | Max. | Units | Conditions |
| 43                 | T <sub>DW</sub> | Flash Data Memory Write Cycle Time | 2                                                                                                                                                                                                                                                                                                                                                                        | 3.5                | 5    | ms    |            |
| 44                 | T <sub>DE</sub> | Flash Data Memory Erase Cycle Time | 2                                                                                                                                                                                                                                                                                                                                                                        | 3                  | 4    | ms    |            |

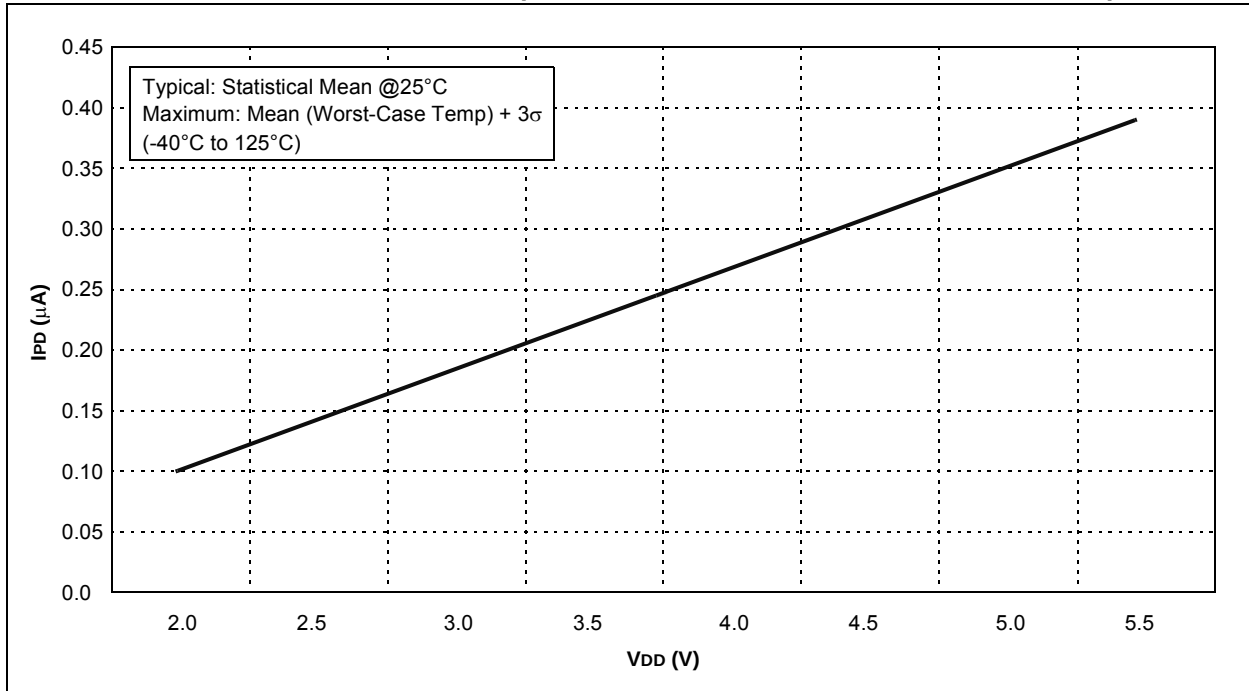
\* These parameters are characterized but not tested.

**Note 1:** Data in the Typical (“Typ”) column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

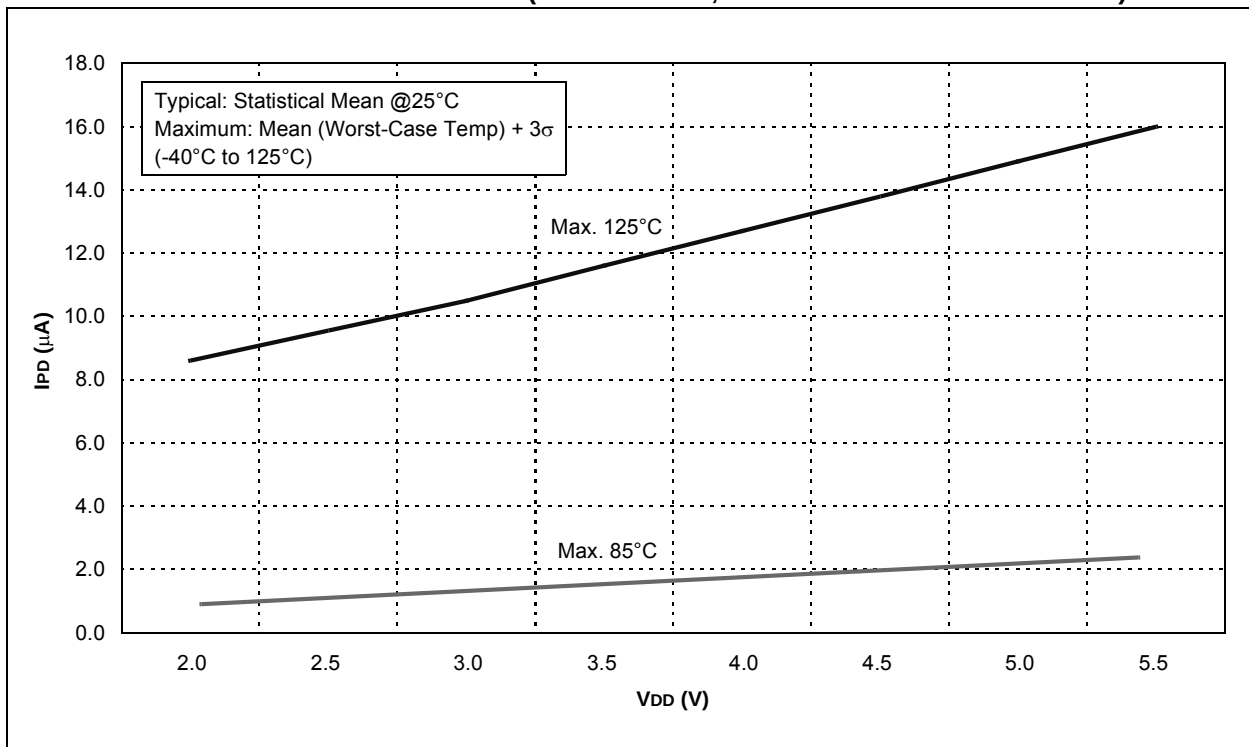
FIGURE 12-3: I<sub>DD</sub> vs. V<sub>DD</sub> OVER F<sub>osc</sub> (LP MODE)



**FIGURE 12-4: TYPICAL  $I_{PD}$  vs.  $V_{DD}$  (SLEEP MODE, ALL PERIPHERALS DISABLED)**



**FIGURE 12-5: MAXIMUM  $I_{PD}$  vs.  $V_{DD}$  (SLEEP MODE, ALL PERIPHERALS DISABLED)**



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FIGURE 12-10:  $V_{OL}$  vs.  $I_{OL}$  OVER TEMPERATURE ( $V_{DD} = 5.0V$ )

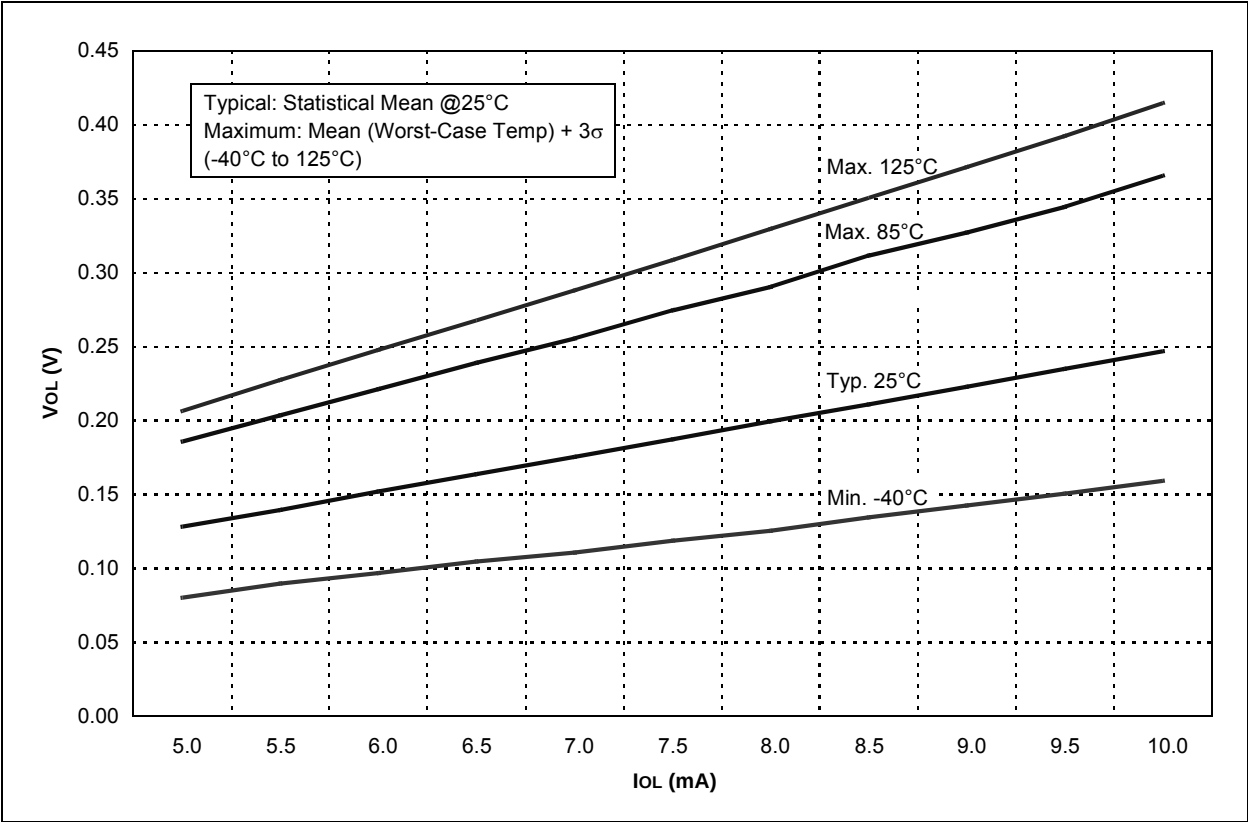
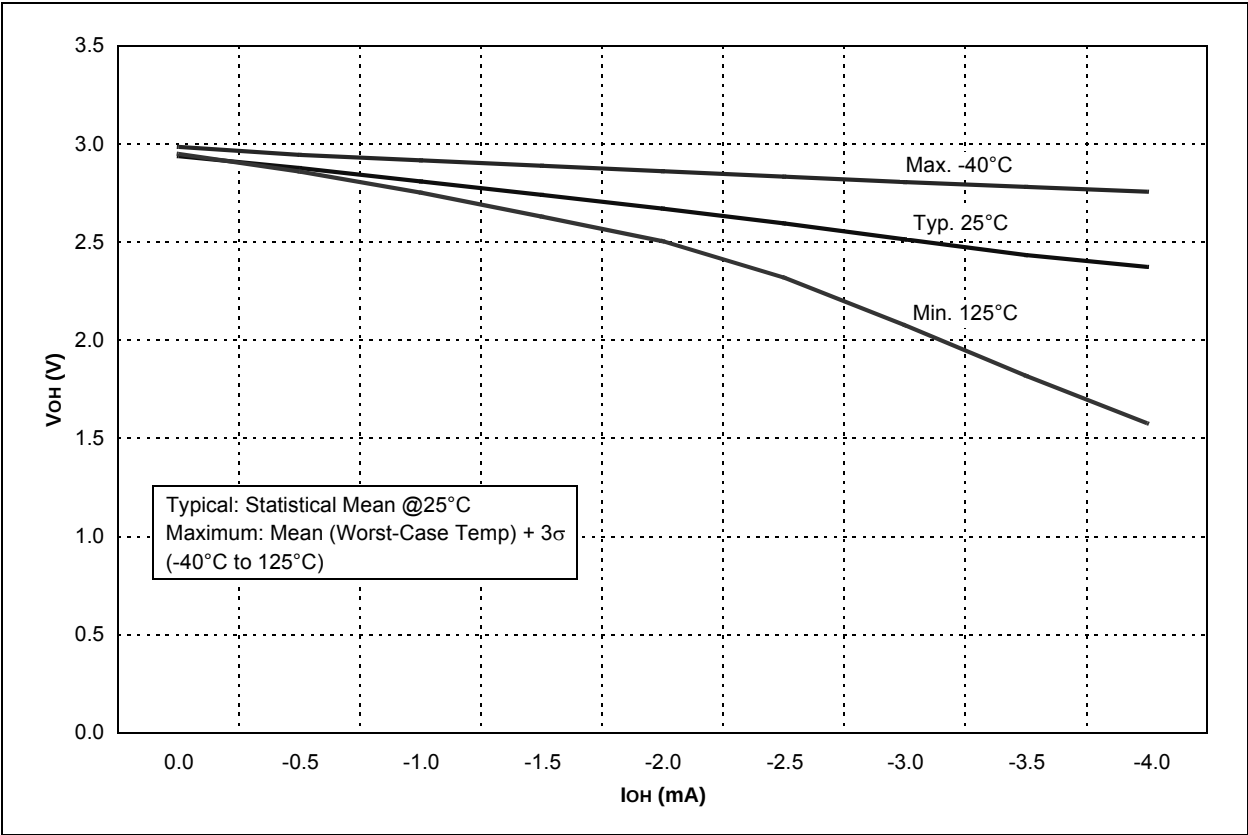


FIGURE 12-11:  $V_{OH}$  vs.  $I_{OH}$  OVER TEMPERATURE ( $V_{DD} = 3.0V$ )



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