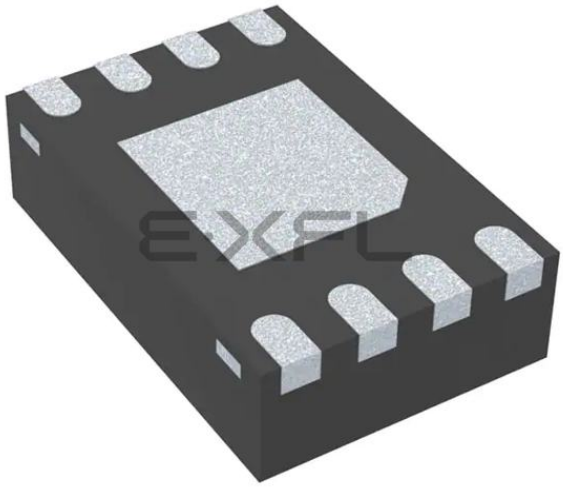


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | - |
| Peripherals | POR, WDT |
| Number of I/O | 5 |
| Program Memory Size | 1.5KB (1K x 12) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 41 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 8-VFDFN Exposed Pad |
| Supplier Device Package | 8-DFN (2x3) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic12f519t-i-mc |

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.



**Trademarks**

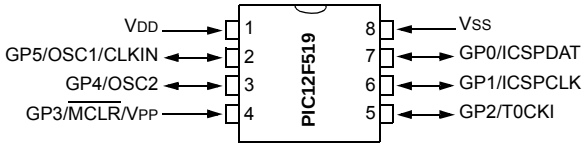


QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

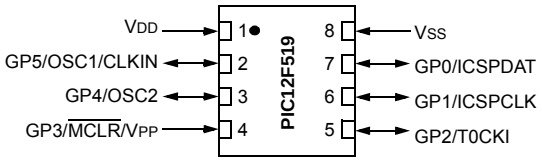
*Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*

**FIGURE 1: PIC12F519 8-PIN PDIP, SOIC, MSOP, 2X3 DFN DIAGRAM**

**PDIP, SOIC, MSOP**




**DFN**




| Device | Program Memory | Data Memory | | I/O | Timers 8-bit |
|---|---|---|---|---|---|
| | Flash (words) | SRAM (bytes) | Flash (bytes) | | |
| PIC12F519 | 1024 | 41 | 64 | 6 | 1 |

**NOTES:**

**TABLE 3-2: PIC12F519 PINOUT DESCRIPTION**

| Name | Function | Type | Input Type | Output Type | Description |
|---|---|---|---|---|---|
| GP0/ICSPDAT | GP0 | I/O | TTL | CMOS | Bidirectional I/O port with weak pull-up |
| | ICSPDAT | I/O | ST | CMOS | ICSP™ mode Schmitt Trigger |
| GP1/ICSPCLK | GP1 | I/O | TTL | CMOS | Bidirectional I/O port with weak pull-up |
| | ICSPCLK | I | ST | — | ICSP™ mode Schmitt Trigger |
| GP2/T0CKI | GP2 | I/O | TTL | CMOS | Bidirectional I/O port |
| | T0CKI | I | ST | — | Timer0 clock input |
| GP3/$\overline{\text{MCLR}}$/$V_{PP}$ | GP3 | I | TTL | — | Standard TTL input with weak pull-up |
| | $\overline{\text{MCLR}}$ | I | ST | — | $\overline{\text{MCLR}}$ input (Weak pull-up always enabled in this mode) |
| | $V_{PP}$ | I | High Voltage | — | Test mode high voltage pin |
| GP4/OSC2 | GP4 | I/O | TTL | CMOS | Bidirectional I/O port |
| | OSC2 | O | — | XTAL | XTAL oscillator output pin |
| GP5/OSC1/ CLKIN | GP5 | I/O | TTL | CMOS | Bidirectional I/O port |
| | OSC1 | I | XTAL | — | XTAL oscillator input pin |
| | CLKIN | I | ST | — | EXTRC Schmitt Trigger input |
| $V_{DD}$ | $V_{DD}$ | P | — | — | Positive supply for logic and I/O pins |
| $V_{SS}$ | $V_{SS}$ | P | — | — | Ground reference for logic and I/O pins |

**Legend:** I = Input, O = Output, I/O = Input/Output, P = Power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input, AN = Analog Voltage

## 3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the PC is incremented every Q1 and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2 and Example 3-1.

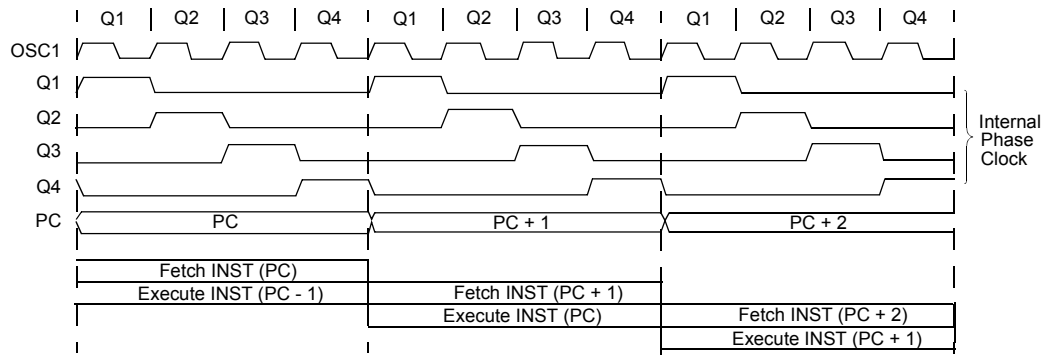
## 3.2 Instruction Flow/Pipelining

An instruction cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute take another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the PC to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the PC incrementing in Q1.

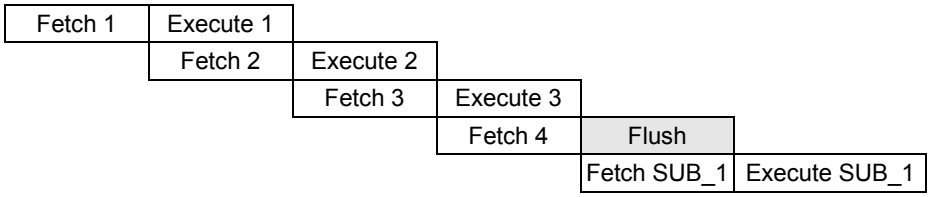
In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

**FIGURE 3-2: CLOCK/INSTRUCTION CYCLE**




**EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW**

```
1. MOVLW 03H
2. MOVWF GPIO
3. CALL  SUB_1
4. BSF  GPIO, 1
```




All instructions are single cycle, except for any program branches. These take two cycles, since the fetch instruction is “flushed” from the pipeline, while the new instruction is being fetched and then executed.

## 4.5 OSCCAL Register

The Oscillator Calibration (OSCCAL) register is used to calibrate the 8 MHz internal oscillator macro. It contains 7 bits of calibration that uses a two's complement scheme for controlling the oscillator speed. See Register 4-3 for details.

**REGISTER 4-3: OSCCAL: OSCILLATOR CALIBRATION REGISTER**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | U-0 |
|---|---|---|---|---|---|---|---|
| CAL6 | CAL5 | CAL4 | CAL3 | CAL2 | CAL1 | CAL0 | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-1 **CAL<6:0>**: Oscillator Calibration bits

0111111 = Maximum frequency
•
•
•
0000001
0000000 = Center frequency
1111111
•
•
•
1000000 =Minimum frequency

bit 0 **Unimplemented**: Read as '0'

## 4.8 Indirect Data Addressing: INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although Status bits may be affected).

The FSR is an 8-bit wide register. It is used in conjunction with the INDF Register to indirectly address the data memory area.

The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

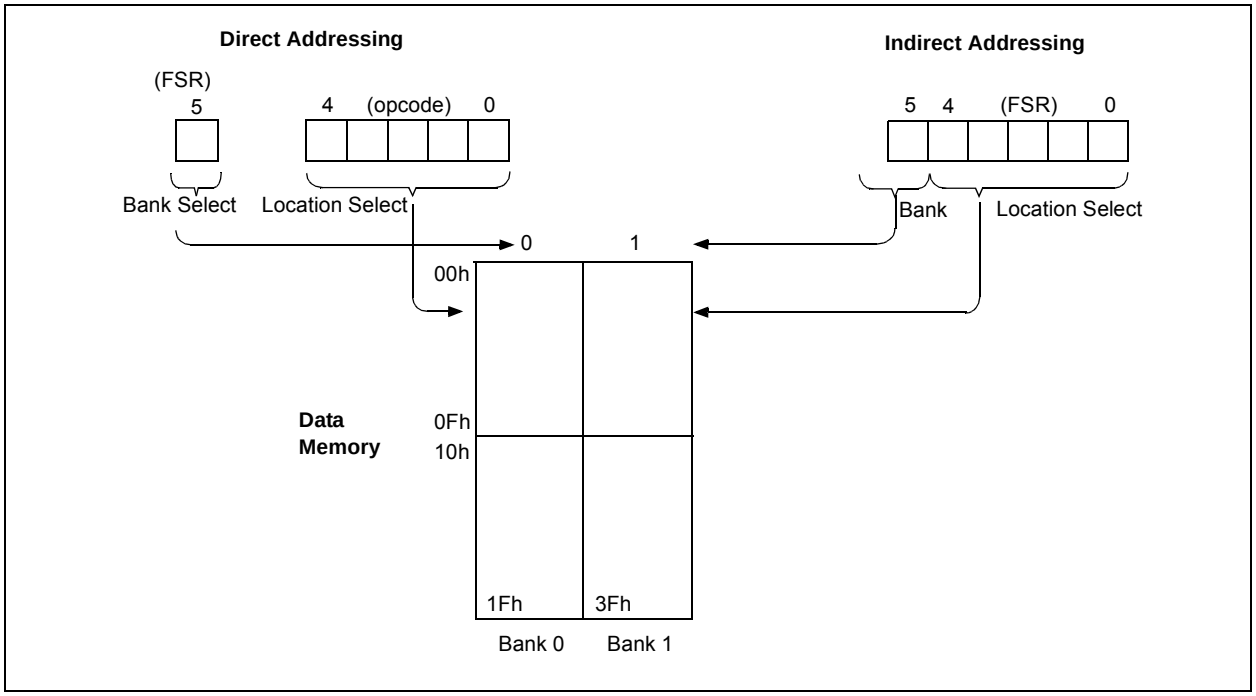
FSR<5> is used to select between banks (0 = Bank 0, 1 = Bank 1).

FSR<7:6> are unimplemented and read as '11'.

**EXAMPLE 4-1: HOW TO CLEAR RAM USING INDIRECT ADDRESSING**

```
          MOVLW  0x10    ;initialize pointer
          MOVWF  FSR     ;to RAM
NEXT      CLRF   INDF    ;clear INDF
                         ;register
          INCF   FSR,F   ;inc pointer
          BTFSC  FSR,4   ;all done?
          GOTO   NEXT    ;NO, clear next
CONTINUE
            :            ;YES, continue
            :
```

**FIGURE 4-4: DIRECT/INDIRECT ADDRESSING**



**REGISTER 8-1: CONFIG: CONFIGURATION WORD REGISTER(1)**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| — | $\overline{\text{CPDF}}$ | IOSCFS | MCLRE | $\overline{\text{CP}}$ | WDTE | FOSC1 | FOSC0 |
| bit 7 | | | | | | | bit 0 |

bit 7 **Unimplemented**: Read as '1'

bit 6 **$\overline{\text{CPDF}}$:** Code Protection bit - Flash Data Memory
1 = Code protection off
0 = Code protection on

bit 5 **IOSCFS:** Internal Oscillator Frequency Select bit
1 = 8 MHz INTOSC frequency
0 = 4 MHz INTOSC frequency

bit 4 **MCLRE:** Master Clear Enable bit
1 = GP3/$\overline{\text{MCLR}}$ pin functions as $\overline{\text{MCLR}}$
0 = GP3/$\overline{\text{MCLR}}$ pin functions as GP3, $\overline{\text{MCLR}}$ internally tied to $V_{DD}$

bit 3 **$\overline{\text{CP}}$:** Code Protection bit - User Program Memory
1 = Code protection off
0 = Code protection on

bit 2 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0 **FOSC<1:0>:** Oscillator Selection bits
00 = LP oscillator with 18 ms DRT(2)
01 = XT oscillator with 18 ms DRT(2)
10 = INTOSC with 1 ms DRT(2)
11 = EXTRC with 1 ms DRT(2)

**Note 1:** Refer to the "*PIC12F519 Memory Programming Specification*", DS41316 to determine how to program/erase the Configuration Word.

**2:** DRT length (18 ms or 1 ms) is a function of clock mode selection. It is the responsibility of the application designer to ensure the use of either 18 ms (nominal) DRT or the 1 ms (nominal) DRT will result in acceptable operation. Refer to Figure 11-1 and Table 11-2 for $V_{DD}$ rise time and stability requirements for this mode of operation.

## 8.2 Oscillator Configurations

### 8.2.1 OSCILLATOR TYPES

The PIC12F519 device can be operated in up to four different oscillator modes. The user can program using the Configuration bits (FOSC<1:0>), to select one of these modes:

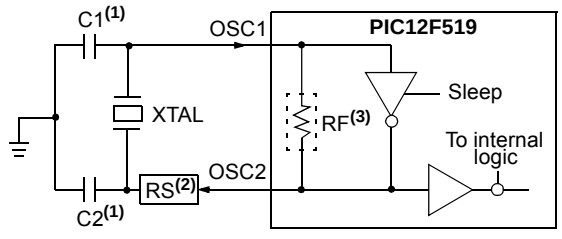
- LP: Low-Power Crystal
- XT: Crystal/Resonator
- INTRC: Internal 4 MHz or 8 MHz Oscillator
- EXTRC: External Resistor/Capacitor

### 8.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In XT or LP modes, a crystal or ceramic resonator is connected to the (GP5)/OSC1/(CLKIN) and (GP4)/OSC2 pins to establish oscillation (Figure 8-1). The PIC12F519 oscillator designs require the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT or LP modes, the device can have an external clock source drive the (GP5)/OSC1/CLKIN pin (Figure 8-2). When the part is used in this fashion, the output drive levels on the OSC2 pin are very weak. This pin should be left open and unloaded. Also when using this mode, the external clock should observe the frequency limits for the clock mode chosen (XT or LP).

| | |
|---|---|
| **Note 1:** | The user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the Oscillator mode may be required. |

**FIGURE 8-1: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (XT OR LP OSC CONFIGURATION)**




**Note 1:** See Capacitor Selection tables for recommended values of C1 and C2.
**2:** A series resistor (RS) may be required for AT strip cut crystals.
**3:** RF approx. value = 10 MΩ.

**FIGURE 8-2: EXTERNAL CLOCK INPUT OPERATION (XT OR LP OSC CONFIGURATION)**

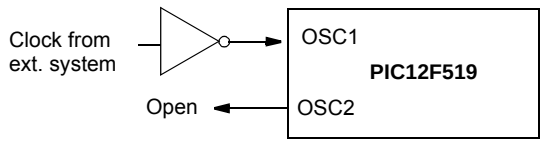



**TABLE 8-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS**

| Osc Type | Resonator Freq. | Cap. Range C1 | Cap. Range C2 |
|---|---|---|---|
| XT | 4.0 MHz | 30 pF | 30 pF |

**Note:** Component values shown are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

**TABLE 8-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR – PIC12F519(2)**

| Osc Type | Resonator Freq. | Cap.Range C1 | Cap. Range C2 |
|---|---|---|---|
| LP | 32 kHz(1) | 15 pF | 15 pF |
| XT | 200 kHz<br>1 MHz<br>4 MHz | 47-68 pF<br>15 pF<br>15 pF | 47-68 pF<br>15 pF<br>15 pF |

**Note 1:** For $V_{DD}$ > 4.5V, C1 = C2 ≈ 30 pF is recommended.
**2:** Component values shown are for design guidance only. Rs may be required to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

**FIGURE 8-7: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT**

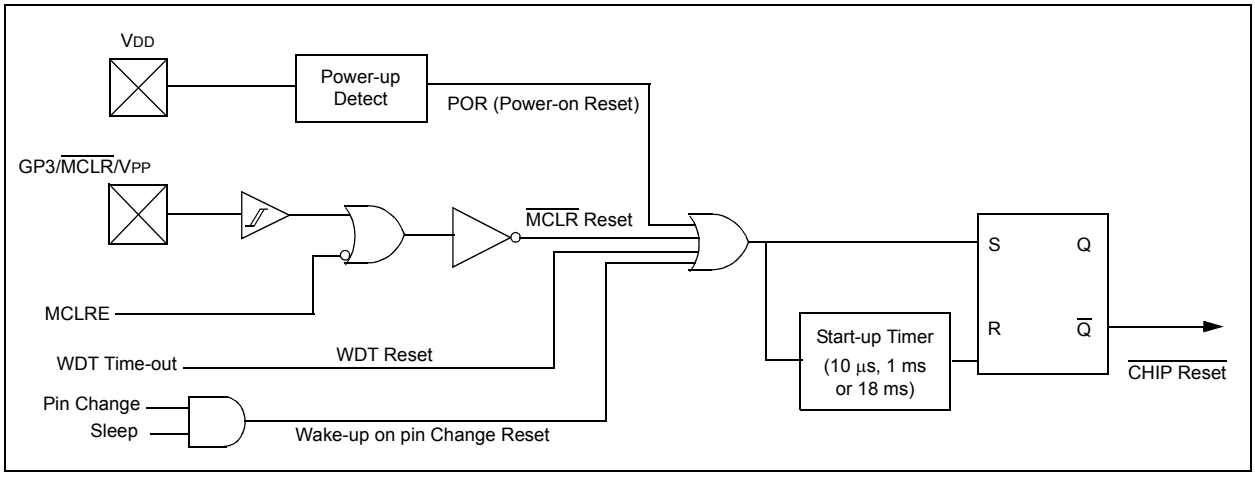



**FIGURE 8-8: TIME-OUT SEQUENCE ON POWER-UP (MCLR PULLED LOW)**

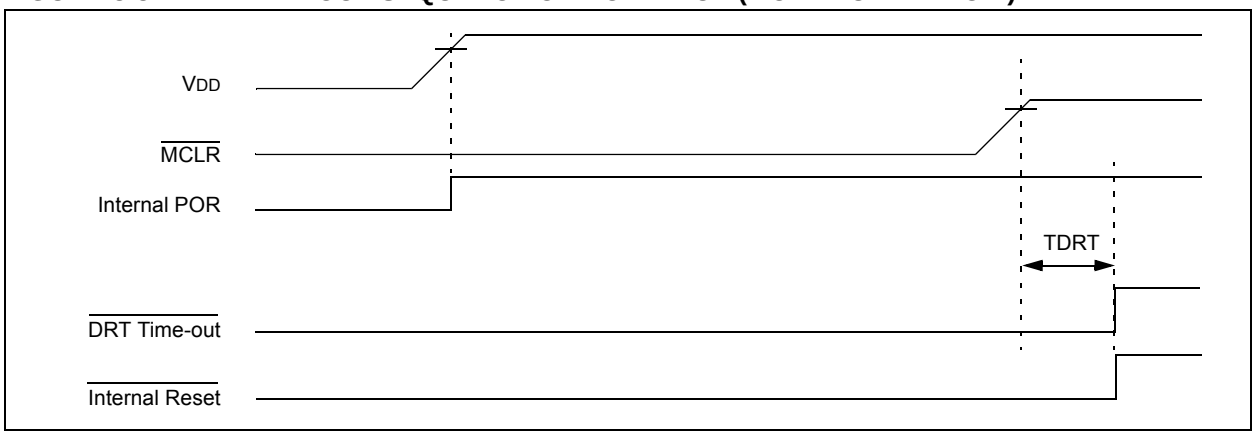
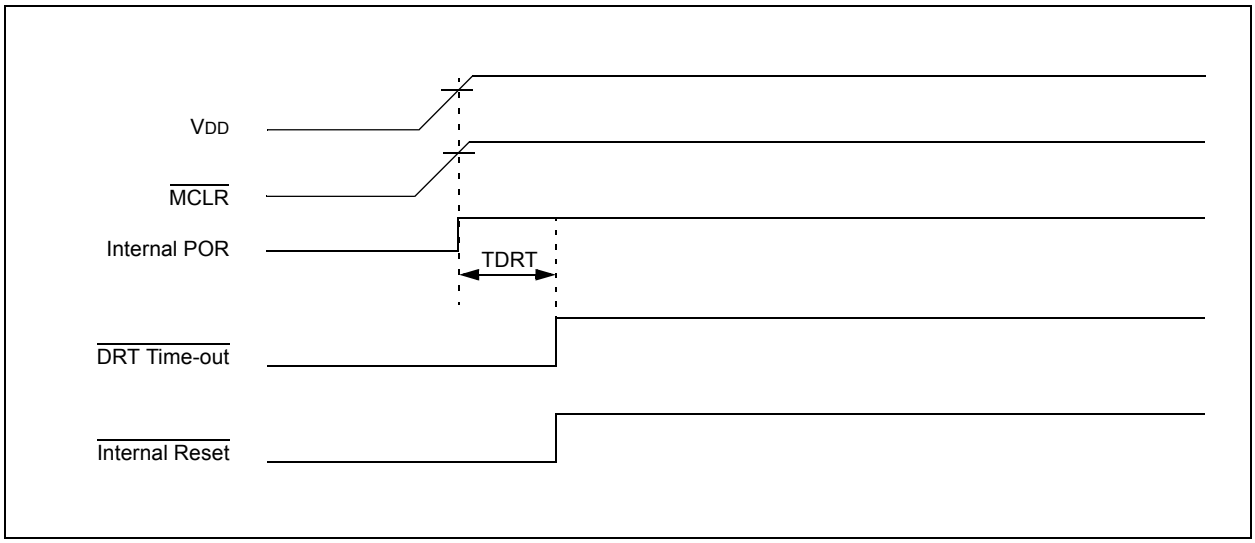



**FIGURE 8-9: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD): FAST VDD RISE TIME**



## 10.7 MPLAB ICE 2000 High-Performance In-Circuit Emulator

The MPLAB ICE 2000 In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers. Software control of the MPLAB ICE 2000 In-Circuit Emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The architecture of the MPLAB ICE 2000 In-Circuit Emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE 2000 In-Circuit Emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft® Windows® 32-bit operating system were chosen to best make these features available in a simple, unified application.

## 10.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC® and MCU devices. It debugs and programs PIC® and dsPIC® Flash microcontrollers with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The MPLAB REAL ICE probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with the popular MPLAB ICD 2 system (RJ11) or with the new high speed, noise tolerant, low-voltage differential signal (LVDS) interconnection (CAT5).

MPLAB REAL ICE is field upgradeable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added, such as software breakpoints and assembly code trace. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, real-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

## 10.9 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low-cost, run-time development tool, connecting to the host PC via an RS-232 or high-speed USB interface. This tool is based on the Flash PIC MCUs and can be used to develop for these and other PIC MCUs and dsPIC DSCs. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the Flash devices. This feature, along with Microchip's In-Circuit Serial Programming™ (ICSP™) protocol, offers cost-effective, in-circuit Flash debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single stepping and watching variables, and CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real time. MPLAB ICD 2 also serves as a development programmer for selected PIC devices.

## 10.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at $V_{DDMIN}$ and $V_{DDMAX}$ for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an SD/MMC card for file storage and secure data applications.

**TABLE 11-2: DC CHARACTERISTICS: PIC12F519 (Extended)**

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature -40°C ≤ TA ≤ +125°C (extended) | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ(1)** | **Max.** | **Units** | **Conditions** |
| D001 | VDD | **Supply Voltage** | 2.0 | | 5.5 | V | See **Figure 11-1** |
| D002 | VDR | **RAM Data Retention Voltage(2)** | — | 1.5* | — | V | Device in Sleep mode |
| D003 | VPOR | **VDD Start Voltage** to ensure Power-on Reset | — | Vss | — | V | See **Section 8.4 "Power-on Reset (POR)"** for details |
| D004 | SVDD | **VDD Rise Rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | See **Section 8.4 "Power-on Reset (POR)"** for details |
| D005 | IDDP | **Supply Current** During Prog/ Erase. | — | 250* | — | μA | |
| D010 | IDD | **Supply Current(3,4)** | —<br>— | 175<br>400 | 250<br>700 | μA<br>mA | FOSC = 4 MHz, VDD = 2.0V<br>FOSC = 4 MHz, VDD = 5.0V |
| | | | —<br>— | 250<br>0.75 | 400<br>1.2 | μA<br>mA | FOSC = 8 MHz, VDD = 2.0V<br>FOSC = 8 MHz, VDD = 5.0V |
| | | | —<br>— | 11<br>38 | 24<br>110 | μA<br>μA | FOSC = 32 kHz, VDD = 2.0V<br>FOSC = 32 kHz, VDD = 5.0V |
| D020 | IPD | **Power-down Current(5)** | —<br>— | 0.1<br>0.35 | 9.0<br>15.0 | μA<br>μA | VDD = 2.0V<br>VDD = 5.0V |
| D022 | IWDT | **WDT Current** | —<br>— | 1.0<br>7.0 | 18<br>22 | μA<br>μA | VDD = 2.0V<br>VDD = 5.0V |

* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**2:** This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

**3:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

**4:** The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail for external clock modes; all I/O pins tri-stated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

**5:** For standby current measurements, the conditions are the same as IDD, except that the device is in Sleep mode. If a module current is listed, the current is for that specific module enabled and the device in Sleep.

**TABLE 11-4: PULL-UP RESISTOR RANGES**

| VDD (Volts) | Temperature (°C) | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **GP0/GP1** | | | | | |
| 2.0 | –40 | 73K | 105K | 186K | Ω |
| | 25 | 73K | 113K | 187K | Ω |
| | 85 | 82K | 123K | 190K | Ω |
| | 125 | 86K | 132K | 190K | Ω |
| 5.5 | –40 | 15K | 21K | 33K | Ω |
| | 25 | 15K | 22K | 34K | Ω |
| | 85 | 19K | 26K | 35K | Ω |
| | 125 | 23K | 29K | 35K | Ω |
| **GP3** | | | | | |
| 2.0 | –40 | 63K | 81K | 96K | Ω |
| | 25 | 77K | 93K | 116K | Ω |
| | 85 | 82K | 96K | 116K | Ω |
| | 125 | 86K | 100K | 119K | Ω |
| 5.5 | –40 | 16K | 20K | 22K | Ω |
| | 25 | 16K | 21K | 23K | Ω |
| | 85 | 24K | 25K | 28K | Ω |
| | 125 | 26K | 27K | 29K | Ω |

**TABLE 11-10: TIMER0 CLOCK REQUIREMENTS**

| AC CHARACTERISTICS | | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature -40°C ≤ TA ≤ +85°C (industrial)<br>-40°C ≤ TA ≤ +125°C (extended)<br>Operating Voltage VDD range is described in<br>***Section TABLE 11-3: "DC CHARACTERISTICS: PIC12F519 (Industrial, Extended)"*** | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | | **Min.** | **Typ(1)** | **Max.** | **Units** | **Conditions** |
| 40 | Tt0H | T0CKI High Pulse Width | No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | | With Prescaler | 10* | — | — | ns | |
| 41 | Tt0L | T0CKI Low Pulse Width | No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | | With Prescaler | 10* | — | — | ns | |
| 42 | Tt0P | T0CKI Period | | 20 or TCY + 40* N | — | — | ns | Whichever is greater. N = Prescale Value (1, 2, 4,..., 256) |

* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**TABLE 11-11: FLASH DATA MEMORY WRITE/ERASE REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature -40°C ≤ TA ≤ +85°C (industrial)<br>-40°C ≤ TA ≤ +125°C (extended)<br>Operating Voltage VDD range is described in<br>**Section TABLE 11-3: "DC CHARACTERISTICS: PIC12F519 (Industrial, Extended)"** | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ(1)** | **Max.** | **Units** | **Conditions** |
| 43 | TDW | Flash Data Memory Write Cycle Time | 2 | 3.5 | 5 | ms | |
| 44 | TDE | Flash Data Memory Erase Cycle Time | 2 | 3 | 4 | ms | |

* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

## 12.0 DC AND AC CHARACTERISTICS GRAPHS AND CHARTS

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified VDD range). This is for **information only** and devices are ensured to operate properly only within the specified range.

| **Note:** | The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range. |
|---|---|

**"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over each temperature range.**

**FIGURE 12-1: TYPICAL IDD vs. FOSC OVER VDD (XT, EXTRC mode)**

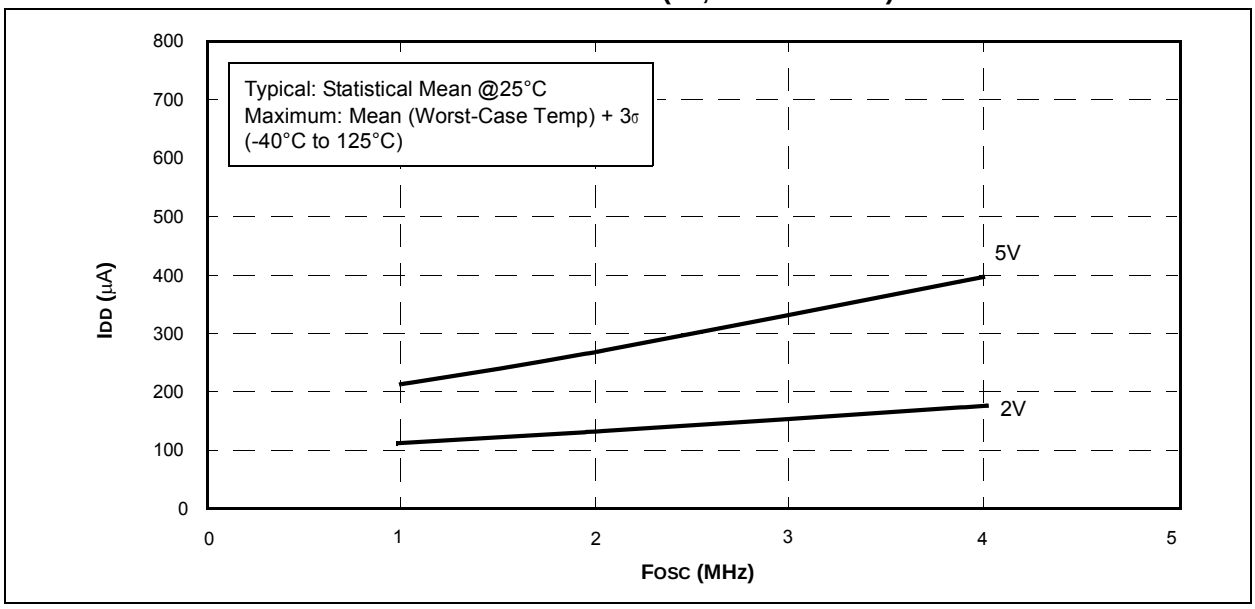



**FIGURE 12-2: MAXIMUM IDD vs. FOSC OVER VDD (XT, EXTRC mode)**

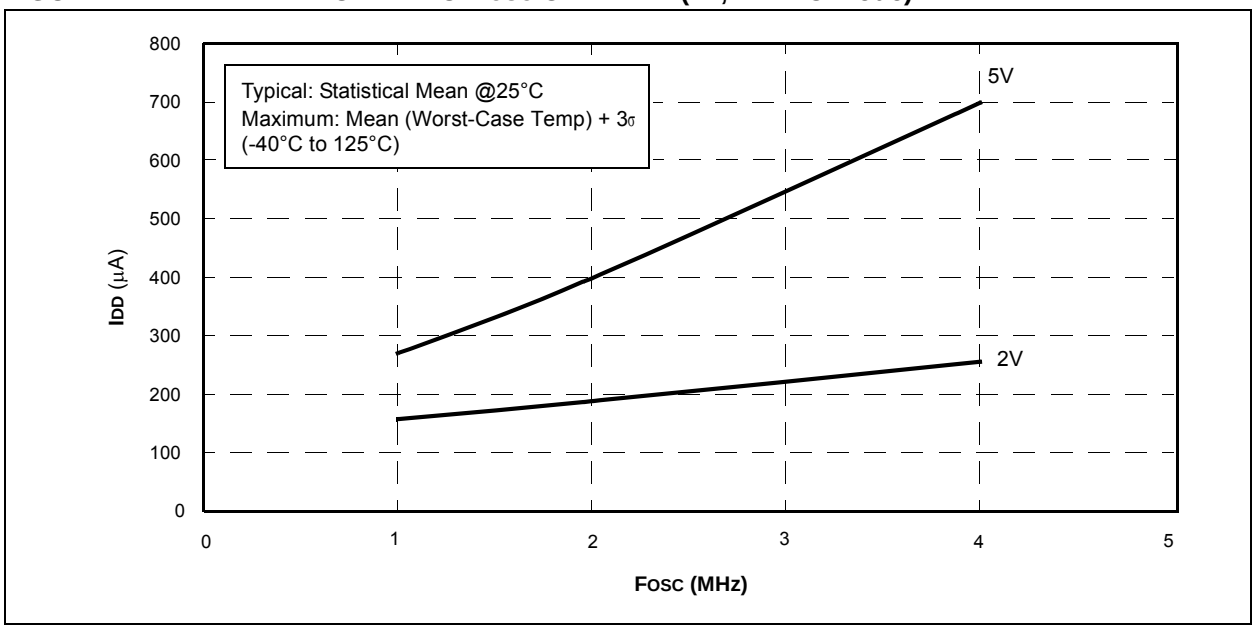


**FIGURE 12-10: $V_{OL}$ vs. $I_{OL}$ OVER TEMPERATURE ($V_{DD}$ = 5.0V)**

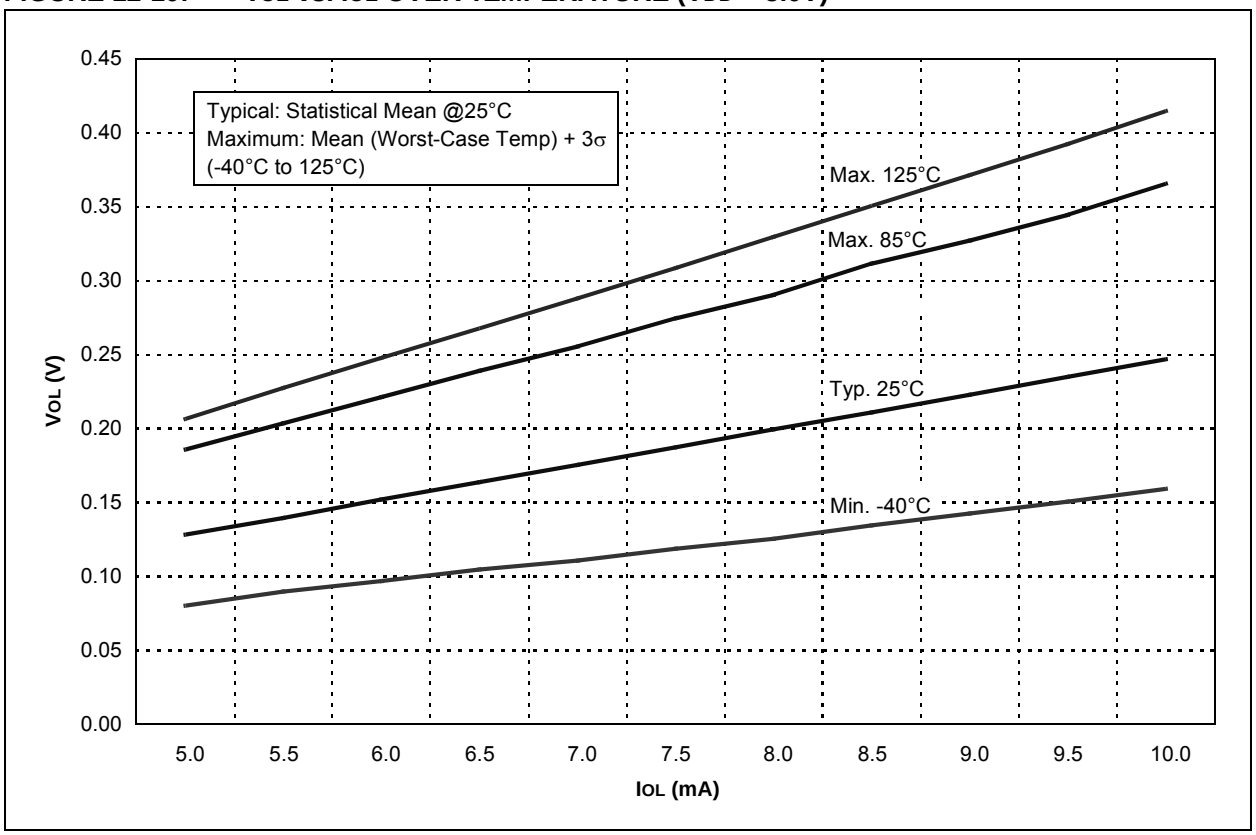
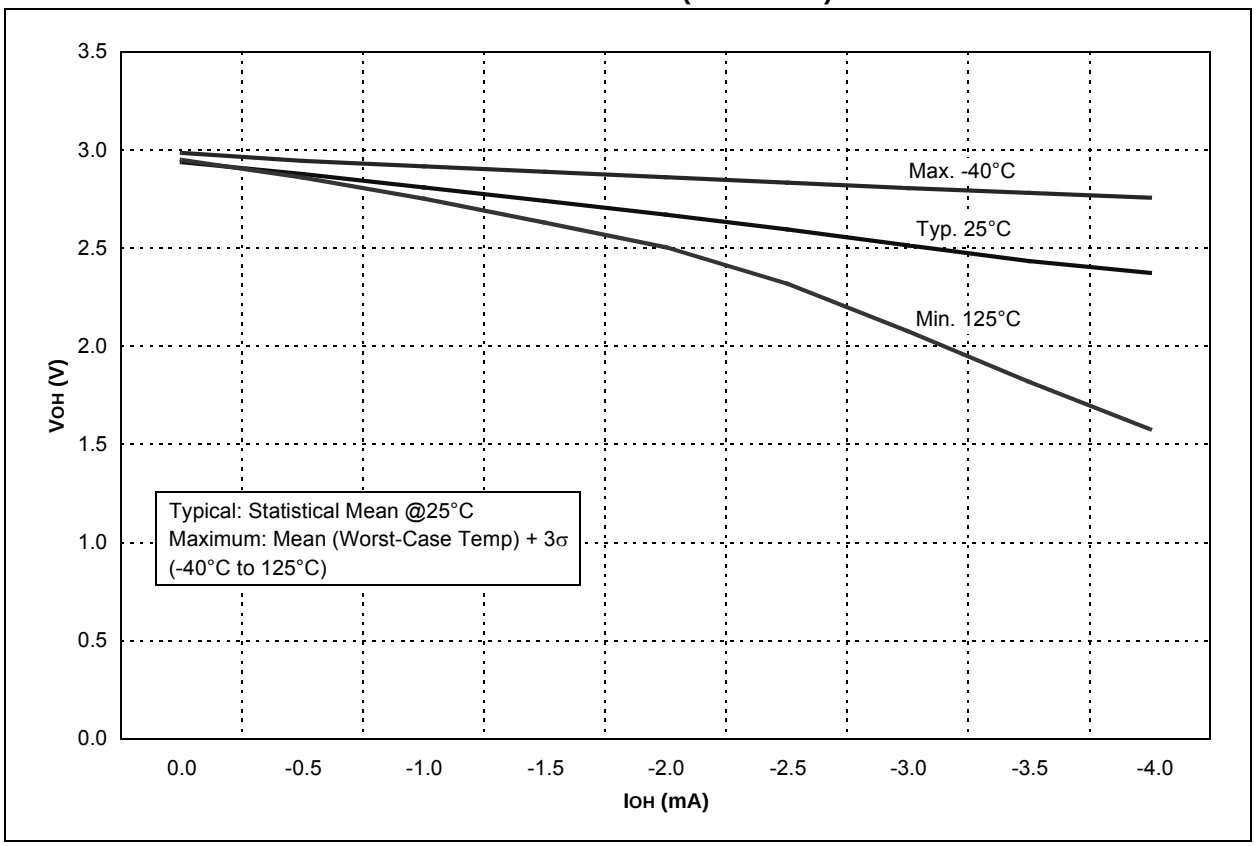
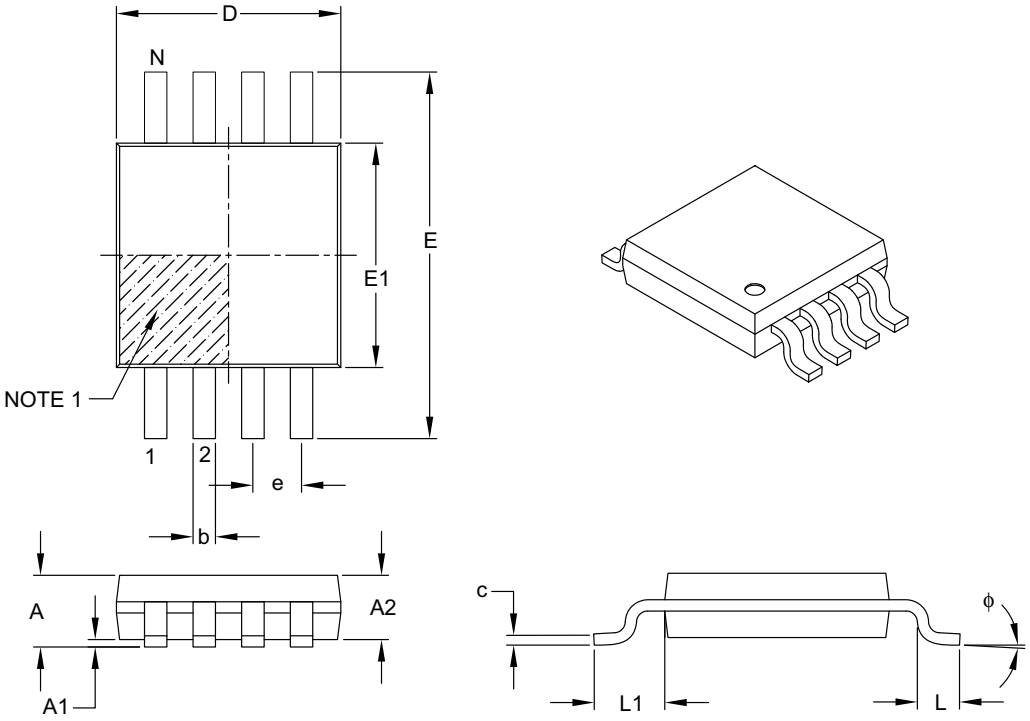



**FIGURE 12-11: $V_{OH}$ vs. $I_{OH}$ OVER TEMPERATURE ($V_{DD}$ = 3.0V)**



## 8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | – | – | 1.10 |
| Molded Package Thickness | A2 | 0.75 | 0.85 | 0.95 |
| Standoff | A1 | 0.00 | – | 0.15 |
| Overall Width | E | | 4.90 BSC | |
| Molded Package Width | E1 | | 3.00 BSC | |
| Overall Length | D | | 3.00 BSC | |
| Foot Length | L | 0.40 | 0.60 | 0.80 |
| Footprint | L1 | | 0.95 REF | |
| Foot Angle | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.08 | – | 0.23 |
| Lead Width | b | 0.22 | – | 0.40 |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

## APPENDIX A: REVISION HISTORY

**Revision A (May 2007)**

Original release of this document.

**Revision B (September 2008)**

Added DC and AC Characteristics graphs; Updated Electrical Characteristics section; Updated Package Drawings and made general edits.

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | /XX | XXX |
|---|---|---|---|
| Device | Temperature Range | Package | Pattern |

| | |
|---|---|
| **Device:** | PIC12F519<br>PIC12F519T (Tape and Reel) |
| **Temperature Range:** | I = -40°C to +85°C (Industrial)<br>E = -40°C to +125°C (Extended) |
| **Package:** | MC = 8L DFN 2x3 (DUAL Flatpack No-Leads)<br>MS = MSOP (Pb-free)<br>P = 300 mil PDIP (Pb-free)<br>SN = 3.90 mm SOIC, 8-LD (Pb-free) |
| **Pattern:** | Special Requirements |

**Note:** Tape and Reel available for only the following packages: SOIC, DFN and MSOP.

**Examples:**

a) PIC12F519-I/P = Industrial temp., PDIP package (Pb-free)

b) PIC12F519T-I/SN = Tape and Reel, Industrial temp., SOIC package

c) PIC12F519 - E/MS 303 = Extended temp., MSOP package, QTP pattern #303