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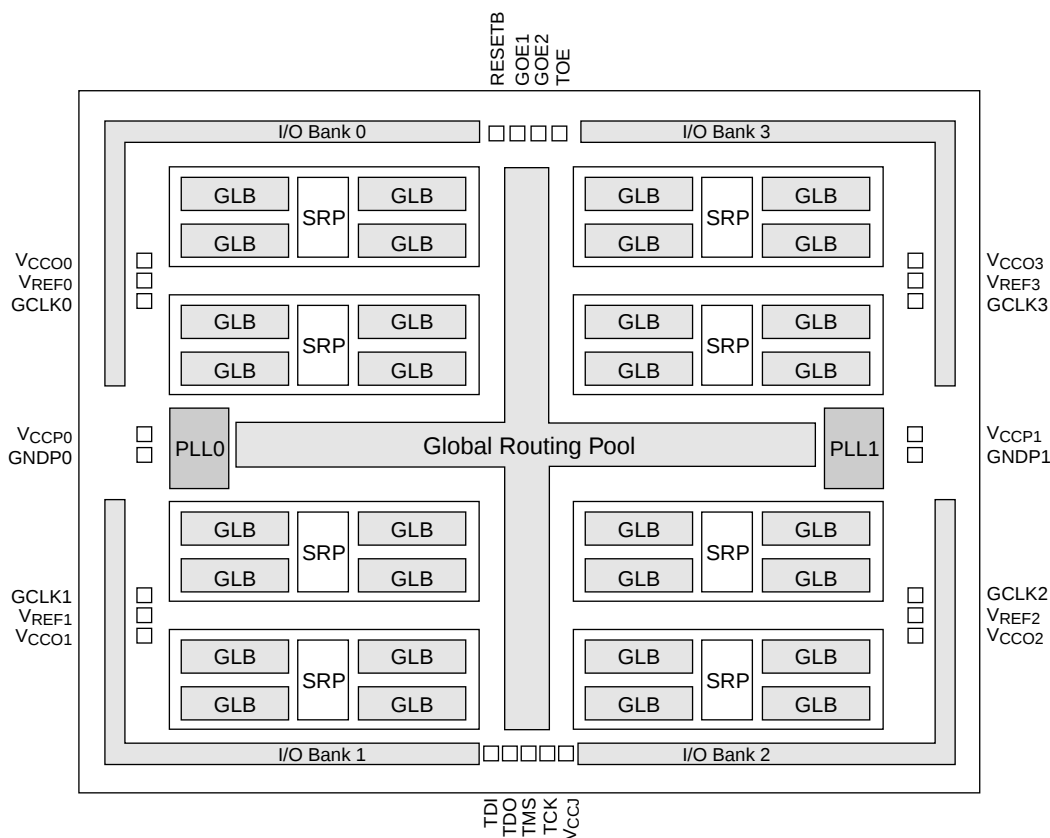
Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	32
Number of Macrocells	1024
Number of Gates	-
Number of I/O	304
Operating Temperature	-40°C ~ 105°C (Tj)
Mounting Type	Surface Mount
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc51024vg-10f484i

Figure 1. Functional Block Diagram

Overview

The ispMACH 5000VG devices consist of multiple SuperWIDE 68-input, 32-macrocell Generic Logic Blocks (GLBs) interconnected by a tiered routing system. Figure 1 shows the functional block diagram of the ispMACH 5000VG. Groups of four GLBs, referred to as segments, are interconnected via a Segment Routing Pool (SRP). Segments are interconnected via the Global Routing Pool (GRP.) Together the GLBs and the routing pools allow designers to create large designs in a single device without compromising performance.

Each GLB has 68 inputs coming from the SRP and contains 163 product terms. These product terms form groups of five product term clusters, which feed the PT sharing array or the macrocell directly. The ispMACH 5000VG allows up to 160 product terms to be connected to a single macrocell via the product term expanders and PT Sharing Array.

The macrocell is designed to provide flexible clocking and control functionality with the capability to select between global, product term and block-level resources. The outputs of the macrocells are fed back into the switch matrices and, if required, the sysIO cell.

All I/Os in the ispMACH 5000VG family are sysIOs, which are split into four banks. Each bank has a separate I/O power supply and reference voltage. The sysIO cells allow operation with a wide range of today's emerging interface standards. Within a bank, inputs can be set to a variety of standards, providing the reference voltage requirements of the chosen standards are compatible. Within a bank, the outputs can be set to differing standards, providing the I/O power supply voltage and the reference voltage requirements of the chosen standard are compatible. Support for this wide range of standards allows designers to achieve significantly higher board-level performance compared to the more traditional LVCMOS standards.

Figure 3. Macrocell Slice

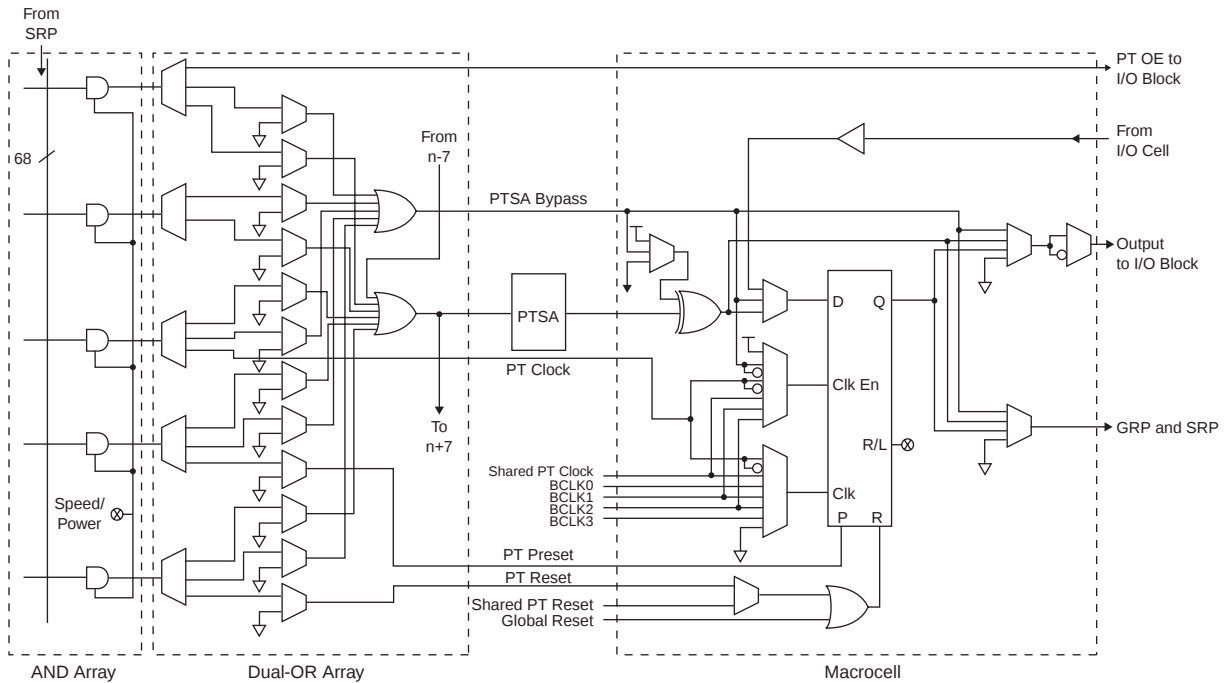
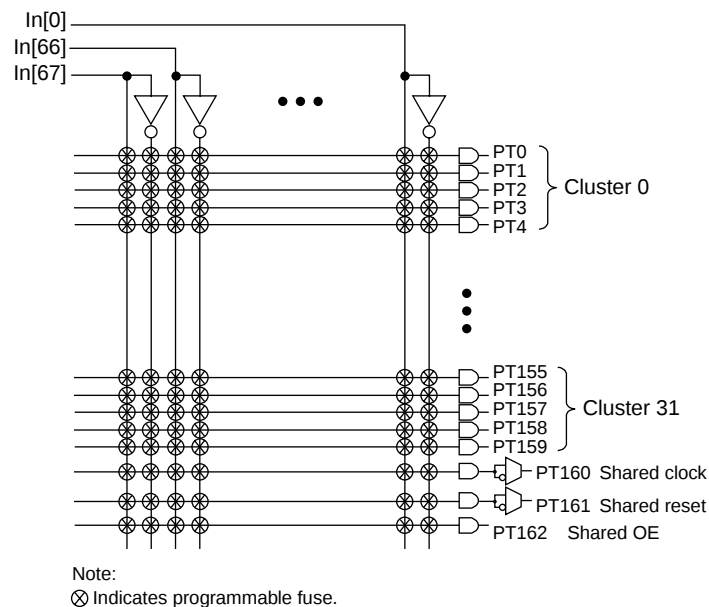


Figure 4. AND-Array



ing with PT0. There is one product term cluster for every macrocell in the GLB. In addition to the three control product terms, the first, third, fourth and fifth product terms of each cluster can be used as a PTOE (output macrocells only), PT Clock, PT Preset and PT Reset, respectively. Figure 4 is a graphical representation of the AND-Array.

Global clock pins have additional capabilities that allow for higher performance applications. Two global clock pins can be paired together to create a single global clock pin that can interface with certain differential signals.

The TOE and JTAG pins of the ispMACH 5000VG device are the only pins that do not have sysIO capabilities. These pins only support the LVTTTL and LVCMOS standards.

There are three classes of I/O interface standards that are implemented in the ispMACH 5000VG devices. The first is the unterminated, single-ended interface. It includes the 3.3V LVTTTL standard along with the 1.8V, 2.5V and 3.3V LVCMOS interface standards. Additionally, PCI 3.3, PCI-X and AGP-1X are all subsets of this type of interface.

The second type of interface implemented is the terminated, single-ended interface standard. This group of interfaces includes different versions of SSTL and HSTL interfaces along with CTT and GTL+. Usage of these particular I/O interfaces requires the use of an additional VREF signal. At the system level, a termination voltage, VTT, is also required. Typically, an output will be terminated to VTT at the receiving end of the transmission line it is driving.

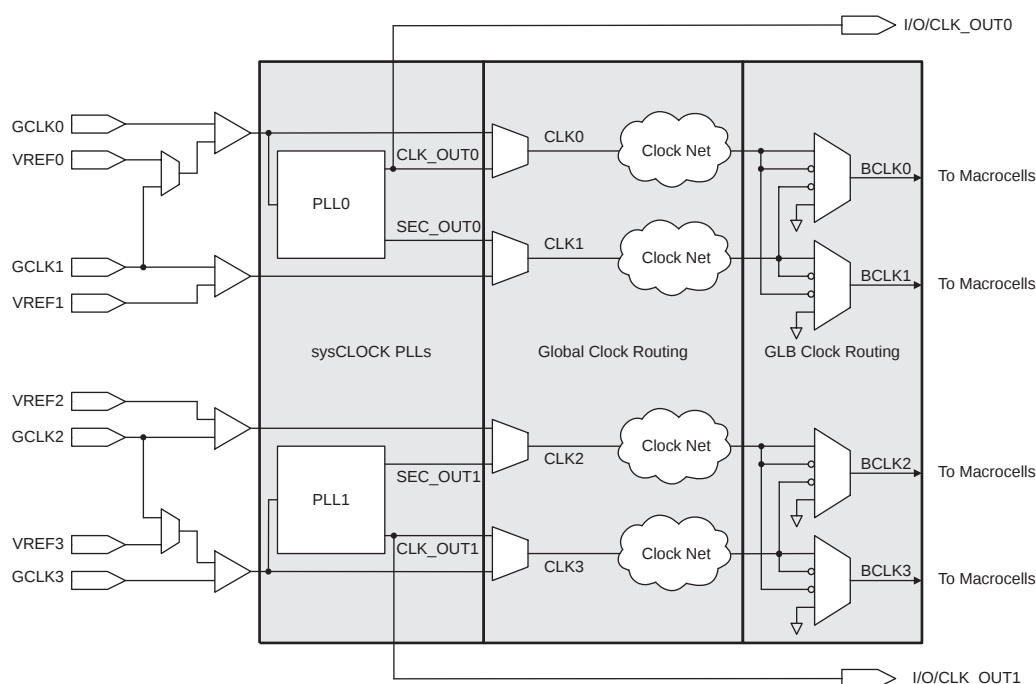
The final types of interfaces implemented are the differential standards LVDS and LVPECL. These interfaces are implemented on clock pins only. When using one of the differential standards, a pair of global clock pins (GCLK0 and GCLK1 or GCLK3 and GCLK2) is combined to create a single clock signal.

For more information on the sysIO capability, please refer to Technical Note TN1000: *ispMACH 5000VG sysIO Design and Usage Guidelines*.

GLB Clock Distribution

The ispMACH 5000VG family has four dedicated clock input pins: GCLK0-GCLK3. GCLK0 and GCLK3 can be routed through a PLL circuit or routed directly to the internal clock nets. The internal clock nets (CLK0-CLK3) are directly related to the dedicated clock pins (see Secondary Clock Divider exception when using the sysCLOCK circuit). These feed the GLB clock multiplexes which generate the GLB clock signals (BCLK0-BCLK3). The GLB clock multiplexer allows a variety of true and complementary versions of the clocks to be used within the GLB. Each block clock can be the true or inverse of its associated global clock or the inverse of the adjacent global clock. Figure 9 shows the clock distribution network.

Figure 9. Clock Distribution Network



Absolute Maximum Ratings^{1, 2, 3}

Supply Voltage (V_{CC}) -0.5 to 5.4V

PLL Supply Voltage (V_{CCP}) -0.5 to 5.4V

Output Supply Voltage (V_{CCO}) -0.5 to 5.4V

Input Voltage Applied⁴ -0.5 to 5.6V

Tri-state Output Voltage Applied -0.5 to 5.6V

Storage Temperature -65 to 150°C

Junction Temperature (T_j) with Power Applied -55 to 130°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Overshoot and Undershoot of -2V to (V_{IH} (MAX)+2) volts is permitted for a duration of < 20ns.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	3.0	3.6	V
V_{CCP}	Supply Voltage for PLL block	3.0	3.6	V
V_{CCJ}	Supply Voltage for IEEE1149.1 Test Access Port	1.65	3.6	V
T_j (Commercial)	Junction Commercial Operation	0	90	C
T_j (Industrial)	Junction Industrial Operation	-40	105	C

Note: V_{CCJ} must be set in appropriate range to be compatible with desired LVCMOS standard.

Erase Reprogram Specifications

Parameter	Min	Max	Units
Erase/Reprogram Cycle	1000	—	Cycles

Hot Socketing Characteristics^{1,2,3}

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DK}	Input or I/O Leakage Current	$0 \leq V_{IN} \leq V_{IH}$ (MAX)	—	—	+/-100	μA
		V_{IH} (MAX) $\leq V_{IN} \leq 5.5V$	—	—	+/-100	μA

1. Insensitive to sequence of V_{CC} and V_{CCO} . However, assumes monotonic rise / fall rates for V_{CC} and V_{CCO} .
2. LVTTTL, LVCMOS only
3. $0 < V_{CC} \leq V_{CC}$ (MAX), $0 < V_{CCO} \leq V_{CCO}$ (MAX)

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units	
I _{IL} , I _{IH} ¹	Input or I/O Leakage Current	0V ≤ V _{IN} ≤ V _{IH} (MAX)	—	—	+/-10	μA	
I _{PU} ²	I/O Weak Pull-up Resistor Current	V _{CCO} = 3.3	-30	—	-150	μA	
		V _{CCO} = 2.5	-20	—	-150	μA	
		V _{CCO} = 1.8	-10	—	-150	μA	
I _{PD} ²	I/O Weak Pull-down Resistor Current	V _{IL} (MAX) ≤ V _{IN} ≤ V _{IH} (MAX)	30	—	150	μA	
I _{BHLS} ²	Bus Hold Low Sustaining Current	V _{IN} = V _{IL} (MAX)	30	—	—	μA	
I _{BHHS} ²	Bus Hold High Sustaining Current	V _{IN} = 0.7 V _{CCO}	V _{CCO} = 3.3	-30	—	—	μA
		V _{CCO} = 2.5	-20	—	—	μA	
		V _{CCO} = 1.8	-10	—	—	μA	
I _{BHLO} ²	Bus Hold Low Overdrive Current	0V ≤ V _{IN} ≤ V _{IH} (MAX)	—	—	150	μA	
I _{BHHO} ²	Bus Hold High Overdrive Current	0V ≤ V _{IN} ≤ V _{IH} (MAX)	—	—	-150	μA	
I _{CC} ^{3, 4, 5}	Operating Power Supply Current	V _{CC} = 3.3V	—	380	—	mA	
V _{BHT}	Bus Hold Trip Points		V _{IL} (MAX)	—	V _{IH} (MIN)	V	
C ₁	I/O Capacitance ³	V _{CC} = 3.3V, V _{IO} = 0 to V _{IH} (MAX)	—	10	—	pf	
		V _{CCO} = 3.3V, 2.5, 1.8, 1.5					
C ₂	Clock Capacitance ³	V _{CC} = 3.3V, V _{IO} = 0 to V _{IH} (MAX)	—	10	—	pf	
		V _{CCO} = 3.3V, 2.5, 1.8, 1.5					
C ₃	Global Input Capacitance ³	V _{CC} = 3.3V, V _{IO} = 0 to V _{IH} (MAX)	—	10	—	pf	
		V _{CCO} = 3.3V, 2.5, 1.8, 1.5					

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. Only available for LVCMOS and LVTTL standards.

3. $T_A = 25^\circ C$, $f = 1.0MHz$.

4. Device configured with 16-bit counters.

5. I_{CC} varies with specific device configuration and operating frequency.

sysIO Recommended Operating Conditions²

Standard	V _{CCO} (V)		V _{REF} (V)	
	Min	Max	Min	Max
LVC MOS 3.3 ¹	3.0	3.6	—	—
LVC MOS 2.5	2.3	2.7	—	—
LVC MOS 1.8	1.65	1.95	—	—
LVTTL	3.0	3.6	—	—
PCI 3.3	3.0	3.6	—	—
PCI-X	3.0	3.6	—	—
AGP-1X	3.15	3.45	—	—
SSTL 2	2.3	2.7	1.15	1.35
SSTL 3	3.0	3.6	1.3	1.7
CTT 3.3	3.0	3.6	1.35	1.65
CTT 2.5	2.3	2.7	1.35	1.65
HSTL	1.4	1.6	0.68	0.9
GTL+	1.4	3.6	0.882	1.122

1. Software default setting.

2. Typical values for V_{CCO} and V_{REF} are the average of the Min and Max values.

ispMACH 5768VG External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description ^{1,2,3}	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Data propagation delay, 5-PT bypass	—	5.0	—	7.5	—	10.0	—	12.0	ns
t_{PD_PTSA}	Data propagation delay, intrasegment path	—	6.0	—	9.0	—	11.5	—	13.5	ns
t_{PD_GLOBAL}	Data propagation delay, intersegment path	—	6.5	—	9.75	—	13.0	—	16.0	ns
t_S	GLB register setup time before clock, 5-PT bypass	3.0	—	5.0	—	7.5	—	9.3	—	ns
t_{S_PTSA}	GLB register setup time before clock	3.0	—	6.0	—	8.5	—	10.0	—	ns
t_{SIR}	GLB register setup time before clock, input register path	2.8	—	3.0	—	4.0	—	5.0	—	ns
t_H	GLB register hold time before clock, 5-PT bypass	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{H_PTSA}	GLB register hold time before clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time before clock, input reg. path	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	4.4	—	5.0	—	6.0	—	7.0	ns
t_R	External reset pin to output delay	—	6.5	—	9.0	—	10.0	—	10.9	ns
t_{RW}	External reset pulse duration	4.0	—	6.0	—	8.0	—	9.5	—	ns
$t_{LPTOE/DIS}$	Input to output local product term output enable/disable	—	7.0	—	9.75	—	11.5	—	13.4	ns
$t_{SPTOE/DIS}$	Input to output segment product term output enable/disable	—	8.0	—	11.25	—	17.5	—	20.4	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	6.2	—	7.5	—	8.85	—	10.0	ns
t_{CW}	Global clock width, high or low	1.6	—	2.75	—	3.6	—	4.3	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{WIR}	Input register clock width, high or low	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{SKEW}	Clock-to-out skew, block level	—	0.25	—	0.35	—	0.45	—	0.55	ns
	Clock-to-out skew, segment level	—	0.4	—	0.5	—	0.6	—	0.7	ns
f_{MAX}^4	Clock frequency with internal feedback	178.6	—	117.0	—	87.0	—	73.0	—	MHz
$f_{MAX} (Ext.)$	Clock frequency with external feedback, $1/(t_{S_PTSA} + t_{CO})$	135.1	—	90.9	—	69.0	—	58.8	—	MHz
$f_{MAX} (Tog.)$	Clock frequency max Toggle	312.5	—	181.0	—	138.0	—	116.0	—	MHz

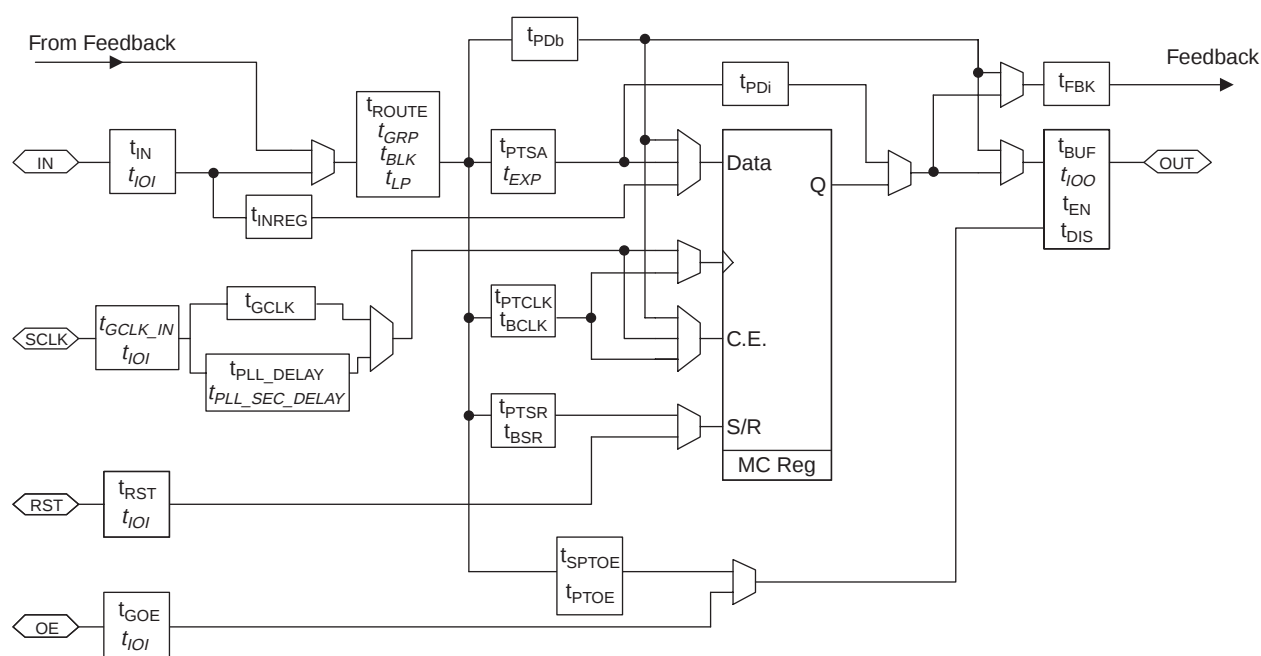
Timing v.1.20

1. Timing numbers are based on default LVCMOS 3.3 I/O Buffers. Use timing adjusters provided to calculate timing for other standards.
2. Measured using standard switching circuit, assuming segment and global routing loading of 1, worst case PTSA loading and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using SRP feedback.

Timing Model

The task of determining the timing through the ispMACH 5000VG family, like any CPLD, is relatively simple. The timing model provided in Figure 11 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, please refer to Technical Note TN1001: *ispMACH 5000VG Timing Model Design and Usage Guidelines*.

Figure 11. ispMACH 5000VG Timing Model



Italicized items are optional delay adders

ispMACH 5768VG Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
In/Out Delays										
t_{IN}	Input Buffer Delay	—	0.65	—	0.95	—	1.25	—	1.40	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	0.65	—	0.95	—	1.25	—	1.40	ns
t_{GOE}	Global OE Pin Delay	—	4.05	—	5.00	—	6.00	—	7.00	ns
t_{BUF}	Delay through Output Buffer	—	1.15	—	1.50	—	1.75	—	1.90	ns
t_{EN}	Output Enable Time	—	2.15	—	2.50	—	2.85	—	3.00	ns
t_{DIS}	Output Disable Time	—	2.15	—	2.50	—	2.85	—	3.00	ns
t_{RSTb}	Global RESETbar Pin Delay	—	4.60	—	6.50	—	7.00	—	7.50	ns
Routing Delays										
t_{ROUTE}	Delay through SRP	—	2.80	—	4.20	—	5.65	—	6.90	ns
t_{PTSA}	Product Term Sharing Array Delay	—	0.40	—	1.85	—	2.35	—	2.50	ns
t_{PDB}	5-PT Bypass Propagation Delay	—	0.40	—	0.85	—	1.35	—	1.80	ns
t_{PDi}	Macrocell Propagation Delay	—	1.00	—	0.50	—	0.50	—	0.80	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	3.00	—	3.05	—	3.50	—	4.40	ns
t_{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t_{GCLK}	Global Clock Tree Delay	—	0.85	—	0.70	—	0.55	—	0.65	ns
t_{PLL_DELAY}	Programmable PLL Delay Increment	—	0.50	—	0.50	—	0.50	—	0.50	ns
$t_{PLL_SEC_DELAY}$	Additional Delay When Using Secondary PLL Output	—	0.60	—	0.60	—	0.60	—	0.60	ns
t_{GRP}	Global Routing Pool Delay	—	1.50	—	2.25	—	3.00	—	4.00	ns
Register/Latch Delays										
t_S	D-Register Setup Time	0.65	—	0.65	—	1.05	—	1.25	—	ns
t_{S_PT}	D-Register Setup Time with PT Clock	0.65	—	0.65	—	1.05	—	1.25	—	ns
t_H	D-Register Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{ST}	T-Register Setup Time	1.15	—	1.15	—	1.55	—	1.75	—	ns
t_{ST_PT}	T-Register Setup Time with PT Clock	1.15	—	1.15	—	1.55	—	1.75	—	ns
t_{HT}	T-Register Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	1.75	—	1.85	—	2.45	—	3.05	ns
t_{CES}	Clock Enable Setup Time	2.60	—	3.90	—	5.05	—	5.95	—	ns
t_{CEH}	Clock Enable Hold Time	0.60	—	0.90	—	1.20	—	1.45	—	ns
t_{SL}	Latch Setup Time	2.80	—	4.20	—	5.50	—	6.60	—	ns
t_{SL_PT}	Latch Setup Time with PT Clock	2.80	—	4.20	—	5.50	—	6.60	—	ns
t_{HL}	Latch Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	1.75	—	2.50	—	3.50	—	4.50	ns
t_{PDLi}	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	2.40	—	3.50	—	4.00	—	4.50	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.75	—	1.00	—	1.25	—	1.50	ns
t_{SRR}	Asynchronous Reset or Set Recovery Delay	—	1.00	—	1.50	—	2.00	—	2.50	ns
Control Delays										
t_{BCLK}	GLB PT Clock Delay	—	3.10	—	4.65	—	6.00	—	7.00	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	3.00	—	4.50	—	6.00	—	7.00	ns

ispMACH 5768VG Internal Timing Parameters (Continued)

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{BSR}	Block PT Set/Reset Delay	—	2.00	—	3.00	—	4.00	—	4.80	ns
t _{PTSR}	Macrocell PT Set/Reset Delay	—	2.00	—	3.00	—	4.00	—	4.80	ns
t _{SPTOE}	Segment PT OE Delay	—	2.40	—	3.60	—	7.75	—	9.10	ns
t _{POTOE}	Macrocell PT OE Delay	—	1.40	—	2.10	—	1.75	—	2.10	ns

Notes:

Timing v.1.20

1. Internal Timing Parameters are not tested and are for reference only. Refer to Timing Model in this data sheet for further details.
2. t_{PLL_DELAY} is the unit increment by which the clock signal can be incremented. The PLL can adjust the clock signal by up to 3.5ns in either direction in units of 0.5ns for each step.

ispMACH 51024VG Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
In/Out Delays										
t _{IN}	Input Buffer Delay	—	0.65	—	0.95	—	1.25	—	1.40	ns
t _{GCLK_IN}	Global Clock Input Buffer Delay	—	0.65	—	0.95	—	1.25	—	1.40	ns
t _{GOE}	Global OE Pin Delay	—	4.05	—	5.00	—	6.00	—	7.00	ns
t _{BUF}	Delay through Output Buffer	—	1.15	—	1.50	—	1.75	—	1.90	ns
t _{EN}	Output Enable Time	—	2.15	—	2.50	—	2.85	—	3.00	ns
t _{DIS}	Output Disable Time	—	2.15	—	2.50	—	2.85	—	3.00	ns
t _{RSTb}	Global RESETbar Pin Delay	—	4.60	—	6.50	—	7.00	—	7.50	ns
Routing Delays										
t _{ROUTE}	Delay through SRP	—	2.80	—	4.20	—	5.65	—	6.90	ns
t _{PTSA}	Product Term Sharing Array Delay	—	0.40	—	1.85	—	2.35	—	2.50	ns
t _{PDB}	5-PT Bypass Propagation Delay	—	0.40	—	0.85	—	1.35	—	1.80	ns
t _{PDi}	Macrocell Propagation Delay	—	1.00	—	0.50	—	0.50	—	0.80	ns
t _{INREG}	Input Buffer to Macrocell Register Delay	—	3.00	—	3.05	—	3.50	—	4.40	ns
t _{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t _{GCLK}	Global Clock Tree Delay	—	0.85	—	0.70	—	0.55	—	0.65	ns
t _{PLL_DELAY}	Programmable PLL Delay Increment	—	0.50	—	0.50	—	0.50	—	0.50	ns
t _{PLL_SEC_DELAY}	Additional Delay When Using Secondary PLL Output	—	0.60	—	0.60	—	0.60	—	0.60	ns
t _{GRP}	Global Routing Pool Delay	—	1.50	—	2.25	—	3.00	—	4.00	ns
Register/Latch Delays										
t _S	D-Register Setup Time	0.65	—	0.65	—	1.05	—	1.25	—	ns
t _{S_PT}	D-Register Setup Time with PT Clock	0.65	—	0.65	—	1.05	—	1.25	—	ns
t _H	D-Register Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t _{ST}	T-Register Setup Time	1.15	—	1.15	—	1.55	—	1.75	—	ns
t _{ST_PT}	T-Register Setup Time with PT Clock	1.15	—	1.15	—	1.55	—	1.75	—	ns
t _{HT}	T-Register Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t _{COi}	Register Clock to Output/Feedback MUX Time	—	1.75	—	1.85	—	2.45	—	3.05	ns

ispMACH 5768VG Timing Adders (Continued)

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
LVC MOS18_12mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 1.8V & 12mA Buffer	—	1.35	—	1.35	—	1.35	—	1.35	ns
LVC MOS25_4mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 2.5V & 4mA Buffer	—	1.50	—	1.50	—	1.50	—	1.50	ns
LVC MOS25_5mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 2.5V & 5.33mA Buffer	—	1.25	—	1.25	—	1.25	—	1.25	ns
LVC MOS25_8mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 2.5V & 8mA Buffer	—	0.70	—	0.70	—	0.70	—	0.70	ns
LVC MOS25_12mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 2.5V & 12mA Buffer	—	0.50	—	0.50	—	0.50	—	0.50	ns
LVC MOS25_16mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 2.5V & 16mA Buffer	—	0.25	—	0.25	—	0.25	—	0.25	ns
LVC MOS33_4mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 3.3V & 4mA Buffer	—	1.50	—	1.50	—	1.50	—	1.50	ns
LVC MOS33_5mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 3.3V & 5.33mA Buffer	—	1.25	—	1.25	—	1.25	—	1.25	ns
LVC MOS33_8mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 3.3V & 8mA Buffer	—	0.40	—	0.40	—	0.40	—	0.40	ns
LVC MOS33_12mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 3.3V & 12mA Buffer	—	0.10	—	0.10	—	0.10	—	0.10	ns
LVC MOS33_16mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 3.3V & 16mA Buffer	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVC MOS33_20mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 3.3V & 20mA Buffer	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVTTL	t_{BUF} , t_{EN} , t_{DIS}	Output configured as LVTTL Buffer	—	0.0	—	0.0	—	0.0	—	0.0	ns
Slow Slew	t_{BUF} , t_{EN}	Output configured for slow slew rate	—	1.50	—	1.50	—	1.50	—	1.50	ns
PCI_out	t_{BUF} , t_{EN} , t_{DIS}	Using PCI standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_X_out	t_{BUF} , t_{EN} , t_{DIS}	Using PCI-X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_out	t_{BUF} , t_{EN} , t_{DIS}	Using AGP-1X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL3_I_out	t_{BUF} , t_{EN} , t_{DIS}	Using SSTL3_I standard	—	-0.25	—	-0.25	—	-0.25	—	-0.25	ns
SSTL3_II_out	t_{BUF} , t_{EN} , t_{DIS}	Using SSTL3_II standard	—	-0.35	—	-0.35	—	-0.35	—	-0.35	ns
SSTL2_I_out	t_{BUF} , t_{EN} , t_{DIS}	Using SSTL2_I standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL2_II_out	t_{BUF} , t_{EN} , t_{DIS}	Using SSTL2_II standard	—	-0.25	—	-0.25	—	-0.25	—	-0.25	ns
CTT33_out	t_{BUF} , t_{EN} , t_{DIS}	Using CCT3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
CTT25_out	t_{BUF} , t_{EN} , t_{DIS}	Using CCT2.5 standard	—	0.25	—	0.25	—	0.25	—	0.25	ns
HSTL_I_out	t_{BUF} , t_{EN} , t_{DIS}	Using HSTL_I standard	—	-0.30	—	-0.30	—	-0.30	—	-0.30	ns

Note: Open drain timing is the same as corresponding LVC MOS timing.

Timing v.1.20

ispMACH 5768VG Timing Adders (Continued)

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
HSTL_III_out	t_{BUF} , t_{EN} , t_{DIS}	Using HSTL_III standard	—	0.00	—	0.00	—	0.00	—	0.00	ns
GTL+_out	t_{BUF} , t_{EN} , t_{DIS}	Using GTL+ standard	—	0.30	—	0.30	—	0.30	—	0.30	ns

Note: Open drain timing is the same as corresponding LVCMOS timing.

Timing v.1.20

ispMACH 51024VG Timing Adders

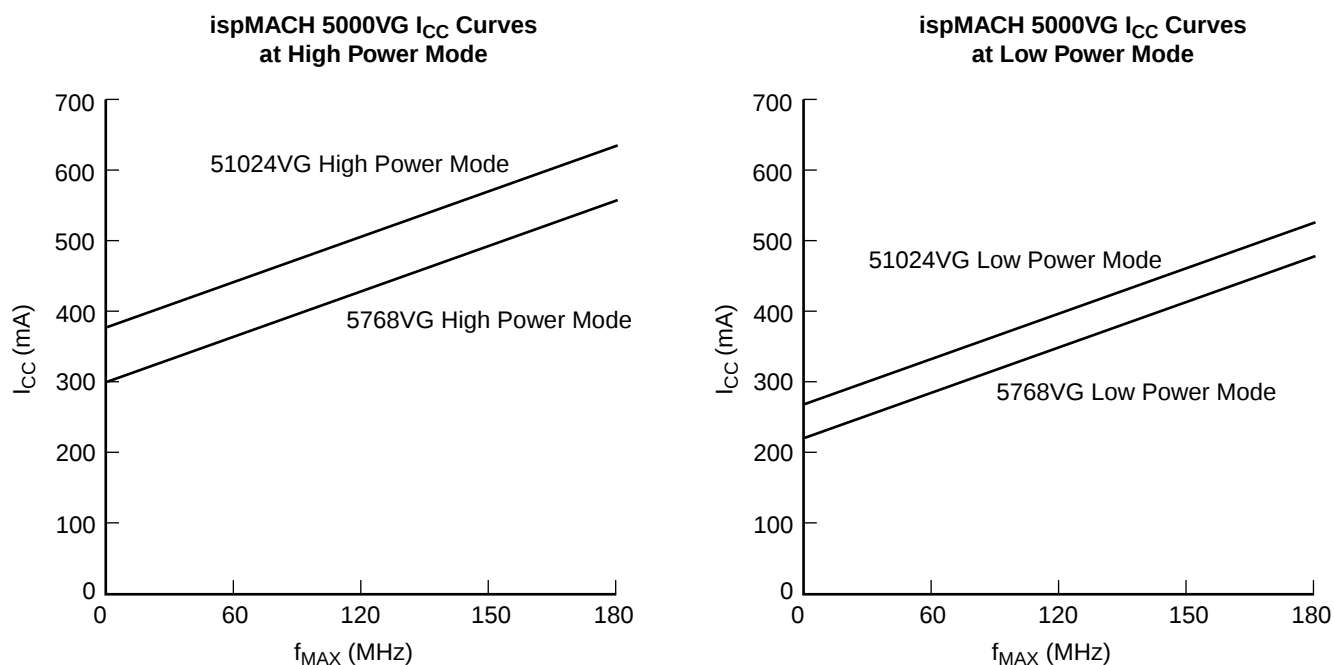
Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{BLA}	t_{ROUTE}	GLB Loading Adder	—	0.0	—	0.0	—	0.0	—	0.0	ns
t_{EXP}	t_{PTSA}	PT Expander Adder	—	1.5	—	2.0	—	2.5	—	2.5	ns
t_{LP}	t_{ROUTE}	Low Power Adder	—	1.5	—	1.5	—	1.5	—	1.5	ns
t_{OI} Input Adders											
LVCMOS18_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using LVCMOS1.8 standard	—	0.90	—	0.90	—	0.90	—	0.90	ns
LVCMOS25_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using LVCMOS2.5 standard	—	0.15	—	0.15	—	0.15	—	0.15	ns
LVCMOS33_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using LVCMOS3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVTTL	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using LVTTL standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using PCI standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_X_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using PCI_X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using AGP-1X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL3_I_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using SSTL3_I standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL3_II_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using SSTL3_II standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL2_I_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using SSTL2_I standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL2_II_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using SSTL2_II standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
CTT33_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using CTT3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
CTT25_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using CTT2.5 standard	—	0.15	—	0.15	—	0.15	—	0.15	ns
HSTL_I_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using HSTL_I standard	—	1.25	—	1.25	—	1.25	—	1.25	ns
HSTL_III_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using HSTL_III standard	—	1.25	—	1.25	—	1.25	—	1.25	ns
GTL+_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using GTL+ standard	—	1.50	—	1.50	—	1.50	—	1.50	ns

Note: Open drain timing is the same as corresponding LVCMOS timing.

Timing v.1.10

Power Consumption

ispMACH 5000VG Typical Power vs. Frequency



Note: The devices are configured with maximum number of 16-bit counters, no PLL, typical current at 3.3V, 25° C.

Power Estimation Coefficients

Device	K0	K1	K2	K3	K4	K5	K6	I_{DC} (mA)	I_{DCO} (mA)
ispMACH 5768VG	0.0014	0.0014	0.054	1.5	0.152	0.105	5.0	65	20
ispMACH 51024VG	0.0014	0.0014	0.054	1.5	0.152	0.105	5.0	80	20

Note: For further information about the use of these coefficients, refer to Technical Note TN1002, *Power Estimation in ispMACH 5000VG Devices*.

K0 = average current per product term in high power/MHz

K1 = average current per product term in low power/MHz

K2 = average current per GRP line/MHz

K3 = average current per PLL/MHz

K4 = DC current per product terms in high power

K5 = DC current per product terms in low power

K6 = Static DC current per PLL

I_{DC} = Static device current with all product terms powered off

I_{DCO} = Static I/O bank current

I_{CC} estimates are based on typical conditions ($V_{CC} = 3.3V$, room temperature) and an assumption of one GLB load on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

Signal Descriptions

Signal Names	Description
TMS	Input - This pin is the Test Mode Select input, which is used to control the 1149.1 state machine.
TCK	Input - This pin is the Test Clock input pin, used to clock the 1149.1 state machine.
TDI	Input - This pin is the 1149.1 Test Data In pin, used to load data.
TDO	Output - This pin is the 1149.1 Test Data Out pin used to shift data out.
TOE	Input - Test Output Enable pin. TOE tristates all I/O pins when a logic low is driven.
GOE0, GOE1	Input - These two pins are the Global Output Enable input pins.
RESETB	Dedicated Reset Input - This pin resets all registers in the devices. The global polarity (active high or low input) for this pin is selectable.
xyzz (e.g. 0A16)	Input/Output - These are the general purpose I/O used by the logic array. x is segment reference (numeric), y is GLB reference (alpha) and z is macrocell reference (numeric). x: 0-7 (1024) x: 0-5 (768) y: A-D z: 0-31
GND	Ground
NC	No connect
V _{CC}	V _{CC} - These are the power supply pins for the logic core.
GCLK0, GCLK3	Input - These pins are configured to be either dedicated CLK input or PLL input.
GCLK1, GCLK2	Input - These pins are dedicated CLK input.
CLK_OUT0, CLK_OUT1	Output - These pins are the PLL output pins.
PLL_RST0, PLL_RST1	Input - These pins are for resetting the PLL, input clock (M) divider.
VREF0, VREF1, VREF2, VREF3	Input - These are the reference supplies for the I/O banks.
PLL_FBK0, PLL_FBK1	Input - These PLL feedback inputs allow optional external PLL feedback.
V _{CCP0} , V _{CCP1}	V _{CC} - These are the V _{CC} supplies for the PLLs.
V _{CCO0} , V _{CCO1} , V _{CCO2} , V _{CCO3}	V _{CC} - These are the V _{CC} supplies for each I/O bank.
GNDP0, GNDP1	GND - These are the separate ground connections for the PLLs.
V _{CCJ}	V _{CC} - This pin is for the 1149.1 test access port.

Note: For above, signal CLK_OUT0 connects to PLL0, and signal CLK_OUT1 connects to PLL1.

ispMACH 51024 Power Supply and NC Connections¹

Signal	484-Ball fpBGA ²	676-Ball fpBGA ²
V _{CC}	B17, B2, B21, B6, C14, C9, E18, E5, F2, F21, J20, J3, P20, P3, U2, U21, Y14, Y9, AA17, AA2, AA21, AA6	B29, D6, D10, D12, D19, D21, D25, F4, F27, K4, K27, M4, M27, W4, W27, AA4, AA27, AE4, AE27, AG6, AG10, AG12, AG19, AG21, AG25, AJ2
V _{CCO0}	B5, D7, E2, E6, E9, F5, G4, J5	E5, E7, E9, E11, F10, G5, J5, K6, L5
V _{CCO1}	P5, U5, V6, V9, Y3	Y5, AA6, AB5, AD5, AE10, AF5, AF7, AF9, AF11
V _{CCO2}	P18, U18, V14, V17, Y20	Y26, AA25, AB26, AD26, AE21, AF20, AF22, AF24, AF26
V _{CCO3}	B18, D16, E14, E17, E21, F18, G19, J18	E20, E22, E24, E26, F21, G26, J26, K25, L26
V _{CCP0}	L7	P5
V _{CCP1}	N18	N26
V _{CCJ}	P4	U6
V _{REF0}	A9	C11
V _{REF1}	AA10	AK10
V _{REF2}	AA13	AJ21
V _{REF3}	A15	E19
GND PLL 0	L6	R6
GND PLL 1	L16	P25
GND	A1, A22, C3, C20, D4, D19, E7, E16, G5, G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, G18, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, K7, K8, K9, K10, K11, K12, K13, K14, K15, K16, L8, L9, L10, L11, L12, L13, L14, L15, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, N7, N8, N9, N10, N11, N12, N13, N14, N15, N16, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, T4, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T19, W7, W16, AB1, AB22	A1, A30, B2, C3, C28, D8, D23, F7, F9, F11, F12, F19, F20, F22, F24, G6, G25, H4, H27, J6, J25, L6, L11, L12, L13, L14, L15, L16, L17, L18, L19, L20, L25, M6, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20, M25, N11, N12, N13, N14, N15, N16, N17, N18, N19, N20, P11, P12, P13, P14, P15, P16, P17, P18, P19, P20, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, T11, T12, T13, T14, T15, T16, T17, T18, T19, T20, U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, V11, V12, V13, V14, V15, V16, V17, V18, V19, V20, W6, W11, W12, W13, W14, W15, W16, W17, W18, W19, W20, W25, Y6, Y11, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y20, Y25, AB6, AB25, AC4, AC27, AD6, AD25, AE7, AE9, AE11, AE12, AE19, AE20, AE22, AE24, AG8, AG23, AH3, AH28, AK1, AK30
NC ³	AA1	A14, A15, A16, A17, B14, B15, B16, B17, C13, C14, C15, C16, C17, C18, D13, D14, D15, D16, D17, D18, E13, E14, E15, E16, E17, E18, F13, F14, F15, F16, F17, F18, AE13, AE14, AE15, AE16, AE17, AE18, AF13, AF14, AF15, AF16, AF17, AF18, AG13, AG14, AG15, AG16, AG17, AG18, AH14, AH15, AH16, AH17, AH18, AJ14, AJ15, AJ16, AJ17, AJ18, AK14, AK15, AK16, AK17

1. All grounds must be electrically connected at the board level.
2. Not all grounds internally connected within the device.
3. NC pins are not to be connected to any active signals, VCC or GND.

ispMACH 5768VG Logic Signal Connections (Continued)

Bank No.	Signal	256 fpBGA	484 fpBGA
3	5C-20	C9	A13
3	5C-22	E9	B12
3	5C-24	D9	C13
3	5C-26	B8	A12
3	5C-28	A6	C12
3	5C-30	B7	A11
—	GCLK0	H4	P6
—	GCLK1	J4	R6
—	GCLK2	H14	P17
—	GCLK3	H13	P19
—	GOE0	J15	R18
—	GOE1	H15	R17
—	RESETB	J14	R19
—	TCK	J3	R3
—	TDI	H3	R2
—	TDO	J2	R4
—	TMS	H2	T1
—	TOE	J13	T18

ispMACH 51024VG Logic Signal Connections (Continued)

Bank No.	Signal	484 fpBGA	676 fpBGA
1	3A-4	V4	AJ4
1	3A-2	U7	AK3
1	3A-0	AB2	AK4
1	3D-0	V7	AJ5
1	3D-2	AA5	AH6
1	GNDIO1	GND	GND
1	3D-4	AB3	AF8
1	3D-6	Y6	AG7
1	3D-8	AB4	AK5
1	3D-10	Y7	AJ6
1	3D-12	AB5	AH7
1	3D-14	V8	AK6
1	3D-16	AA7	AJ7
1	3D-18	Y8	AH8
1	3D-20	AB6	AG9
1	3D-22	W8	AK7
1	3D-24	AA8	AF10
1	3D-26	Y10	AJ8
1	GNDIO1	GND	GND
1	3D-28	U8	AH9
1	3D-30	AB7	AK8
1	3C-0	U9	AJ9
1	3C-2	AA9	AH10
1	3C-4	W9	AK9
1	3C-6	AB8	AG11
1	3C-8	U10	AJ10
1	3C-10	AB9	AF12
1	3C-12	V11	AH11
1	3C-14/VREF1	AA10	AK10
1	3C-16	V10	AJ11
1	3C-18	AB10	AK11
1	GNDIO1	GND	GND
1	3C-20	W10	AH12
1	3C-22	W11	AJ12
1	3C-24	U11	AK12
1	3C-26	AA11	AH13
1	3C-28	V12	AJ13
1	3C-30	AB11	AK13
2	4C-30	W12	AK18
2	4C-28	Y11	AK19
2	4C-26	Y12	AJ19
2	4C-24	AB12	AH19
2	4C-22	U12	AK20

Bank No.	Signal	484 fpBGA	676 fpBGA
2	4C-20	AA12	AJ20
2	GNDIO2	GND	GND
2	4C-18	Y13	AK21
2	4C-16	AB13	AH20
2	4C-14	W13	AF19
2	4C-12/VREF2	AA13	AJ21
2	4C-10	U13	AG20
2	4C-8	AB14	AK22
2	4C-6	V13	AH21
2	4C-4	AA14	AJ22
2	4C-2	U14	AK23
2	4C-0	AB15	AH22
2	4D-30	Y15	AJ23
2	4D-28	AB16	AK24
2	GNDIO2	GND	GND
2	4D-26	AA15	AF21
2	4D-24	W14	AG22
2	4D-22	AB17	AH23
2	4D-20	Y16	AJ24
2	4D-18	AA16	AK25
2	4D-16	Y17	AH24
2	4D-14	AB18	AJ25
2	4D-12	V15	AK26
2	4D-10	AB19	AJ26
2	4D-8	W15	AH25
2	4D-6	AB20	AG24
2	4D-4	AA18	AF23
2	GNDIO2	GND	GND
2	4D-2	U15	AK27
2	4D-0	W17	AK28
2	4A-0	U16	AJ27
2	4A-2	AA19	AH26
2	4A-4	V16	AE23
2	4A-6	AB21	AK29
2	4A-8	NC	AJ28
2	4A-10	NC	AH27
2	GNDIO2	GND	GND
2	4A-12	NC	AG26
2	4A-14	NC	AF25
2	4A-16	Y18	AJ29
2	4A-18	W18	AG27
2	4A-20	AA20	AJ30
2	4A-22	W19	AH29

ispMACH 51024VG Logic Signal Connections (Continued)

Bank No.	Signal	484 fpBGA	676 fpBGA
2	4A-24	Y19	AE25
2	4A-26	V19	AG28
2	GNDIO2	GND	GND
2	4A-28	Y21	AF27
2	4A-30	W20	AE26
2	4B-30	AA22	AH30
2	4B-28	W21	AG29
2	4B-26	Y22	AF28
2	4B-24	V20	AG30
2	4B-22	V21	AF29
2	4B-20	W22	AC25
2	4B-18	V18	AE28
2	4B-16	U20	AF30
2	4B-14	V22	AD27
2	4B-12	U19	AE29
2	GNDIO2	GND	GND
2	4B-10	U17	AC26
2	4B-8	U22	AD28
2	4B-6	T20	AE30
2	4B-4	T21	AD29
2	4B-2	T17	AC28
2	4B-0	R20	AD30
2	5A-0	NC	AC29
2	5A-2	NC	AB27
2	5A-4	NC	AC30
2	5A-6	NC	AB28
2	5A-8	NC	AA26
2	5A-10	NC	AB29
2	GNDIO2	GND	GND
2	5A-12	NC	AB30
2	5A-14	NC	AA28
2	5A-16	NC	AA29
2	5A-18	NC	AA30
2	5A-20	NC	Y27
2	5A-22	NC	Y28
2	5A-24	NC	Y29
2	5A-26	NC	W26
2	5A-28	NC	Y30
2	5A-30	NC	W28
2	GNDIO2	GND	GND
2	5B-30	NC	W29
2	5B-28	NC	W30
2	5B-26	NC	V25

Bank No.	Signal	484 fpBGA	676 fpBGA
2	5B-24	NC	V26
2	5B-22	NC	V27
2	5B-20	NC	V28
2	5B-18	NC	V29
2	5B-16	NC	V30
2	5B-14	NC	U25
2	5B-12	NC	U27
2	GNDIO2	GND	GND
2	5B-10	NC	U28
2	5B-8	NC	U29
2	5B-6	NC	U30
2	5B-4	NC	T27
2	5B-2	NC	T28
2	5B-0	NC	T29
3	6B-0	R21	T30
3	6B-2	T22	R29
3	6B4/PLL_FBK1	P21	R27
3	6B6/PLL_RST1	N20	R28
3	6B-8	R22	R30
3	6B-10	N21	P30
3	GNDIO3	GND	GND
3	6B-12	M18	P29
3	6B-14	N19	P28
3	6B-16	P22	P27
3	6B-18	M20	N30
3	6B-20	N22	N29
3	6B-22	N17	N28
3	6B-24	M19	N27
3	6B-26	M21	N25
3	6B-28	L19	M30
3	6B-30/CLK_OUT1	L20	M29
3	GNDIO3	GND	GND
3	6A-30	M17	M28
3	6A-28	M22	L30
3	6A-26	K20	M26
3	6A-24	L18	L29
3	6A-22	L21	L28
3	6A-20	K19	L27
3	6A-18	L22	K30
3	6A-16	K17	K29
3	6A-14	K22	K28
3	6A-12	L17	J30
3	GNDIO3	GND	GND

Signal Configuration

ispMACH 51024VG 676-ball fpBGA

	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
A	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC ¹	NC ¹	NC ¹	NC ¹	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	A	
B	I/O	VCC	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC ¹	NC ¹	NC ¹	NC ¹	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	I/O	B	
C	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	I/O	I/O/VREF0	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	I/O	I/O	C	
D	I/O	I/O	I/O	I/O	I/O	VCC	I/O	GND	I/O	VCC	I/O	VCC	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	VCC	I/O	VCC	I/O	GND	I/O	VCC	I/O	I/O	I/O	I/O	I/O	D	
E	I/O	I/O	I/O	I/O	VCC03	I/O	VCC03	I/O	VCC03	I/O	VCC03	I/O/VREF3	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	I/O	VCC00	I/O	VCC00	I/O	VCC00	I/O	VCC00	I/O	I/O	I/O	I/O	I/O	E
F	I/O	I/O	I/O	VCC	I/O	I/O	GND	I/O	GND	VCC03	GND	GND	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	GND	GND	VCC00	GND	I/O	GND	I/O	I/O	VCC	I/O	I/O	I/O	F	
G	I/O	I/O	I/O	I/O	VCC03	GND																	GND	VCC00	I/O	I/O	I/O	I/O	G			
H	I/O	I/O	I/O	GND	I/O	I/O																	I/O	I/O	GND	I/O	I/O	I/O	H			
J	I/O	I/O	I/O	I/O	VCC03	GND																	GND	VCC00	I/O	I/O	I/O	I/O	J			
K	I/O	I/O	I/O	VCC	I/O	VCC03																	VCC00	I/O	VCC	I/O	I/O	I/O	K			
L	I/O	I/O	I/O	I/O	VCC03	GND																	GND	VCC00	I/O	I/O	I/O	I/O	L			
M	I/O	I/O/CLK_OUT1	I/O	VCC	I/O	GND																	GND	I/O	VCC	I/O	I/O/CLK_OUT0	I/O	M			
N	I/O	I/O	I/O	I/O	VCCP1	I/O																	I/O	I/O	I/O	I/O	I/O	I/O	N			
P	I/O	I/O	I/O	I/O	GCLK3	GNDP1																	I/O	VCCP0	I/O	I/O	I/O	I/O/PLL_RST0	P			
R	I/O	I/O	I/O/PLL_RST1	I/O/PLL_FBK1	GOE1	GCLK2																	GNDP0	GCLK0	I/O/PLL_FBK0	I/O	I/O	I/O	R			
T	I/O	I/O	I/O	I/O	GOE0	RESETB																	GCLK1	TDI	TMS	I/O	I/O	I/O	T			
U	I/O	I/O	I/O	I/O	TOE	I/O																	VCCJ	TCK	I/O	I/O	I/O	I/O	U			
V	I/O	I/O	I/O	I/O	I/O	I/O																	I/O	TDO	I/O	I/O	I/O	I/O	V			
W	I/O	I/O	I/O	VCC	I/O	GND																	GND	I/O	VCC	I/O	I/O	I/O	W			
Y	I/O	I/O	I/O	I/O	VCC02	GND																	GND	VCC01	I/O	I/O	I/O	I/O	Y			
AA	I/O	I/O	I/O	VCC	I/O	VCC02																	VCC01	I/O	VCC	I/O	I/O	I/O	AA			
AB	I/O	I/O	I/O	I/O	VCC02	GND																	GND	VCC01	I/O	I/O	I/O	I/O	AB			
AC	I/O	I/O	I/O	GND	I/O	I/O																	I/O	I/O	GND	I/O	I/O	I/O	AC			
AD	I/O	I/O	I/O	I/O	VCC02	GND																	GND	VCC01	I/O	I/O	I/O	I/O	AD			
AE	I/O	I/O	I/O	VCC	I/O	I/O	GND	I/O	GND	VCC02	GND	GND	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	GND	GND	VCC01	GND	I/O	GND	I/O	I/O	VCC	I/O	I/O	I/O	AE	
AF	I/O	I/O	I/O	I/O	VCC02	I/O	VCC02	I/O	VCC02	I/O	VCC02	I/O	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	I/O	VCC01	I/O	VCC01	I/O	VCC01	I/O	VCC01	I/O	I/O	I/O	I/O	AF	
AG	I/O	I/O	I/O	I/O	I/O	VCC	I/O	GND	I/O	VCC	I/O	VCC	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	VCC	I/O	VCC	I/O	GND	I/O	VCC	I/O	I/O	I/O	I/O	I/O	AG	
AH	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	I/O	I/O	AH	
AJ	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O/VREF2	I/O	I/O	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCC	I/O	AJ	
AK	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC ¹	NC ¹	NC ¹	NC ¹	I/O	I/O	I/O	I/O/VREF1	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	AK	
	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		

ispMACH 51024VG

Bottom View

ispMACH 51024VG

Bottom View

676BGA/51024VG

1. NCs are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.

Industrial

Part Number	Package	Pin Count	Macrocells	Tpd	Voltage
LC51024VG-75F484I	fpBGA	484	1024	7.5	3.3
LC51024VG-10F484I	fpBGA	484	1024	10	3.3
LC51024VG-12F484I	fpBGA	484	1024	12	3.3
LC51024VG-75F676I	fpBGA	676	1024	7.5	3.3
LC51024VG-10F676I	fpBGA	676	1024	10	3.3
LC51024VG-12F676I	fpBGA	676	1024	12	3.3
LC5768VG-75F256I	fpBGA	256	768	7.5	3.3
LC5768VG-10F256I	fpBGA	256	768	10	3.3
LC5768VG-12F256I	fpBGA	256	768	12	3.3
LC5768VG-75F484I	fpBGA	484	768	7.5	3.3
LC5768VG-10F484I	fpBGA	484	768	10	3.3
LC5768VG-12F484I	fpBGA	484	768	12	3.3

Note: the ispMACH 5000VG family is dual-marked with both Commercial and Industrial grades. The Commercial speed grade is one speed grade faster (i.e. LC51024VG-75F484C) than the Industrial speed grade (i.e. LC51024VG-10F484I).

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 5000VG family:

- *ispMACH 5000VG sysIO Design and Usage Guidelines* (TN1000)
- *ispMACH 5000VG Timing Model Design and Usage Guidelines* (TN1001)
- *Power Estimation in ispMACH 5000VG Devices* (TN1002)
- *ispMACH 5000VG PLL Usage Guidelines* (TN1003)