Lattice Semiconductor Corporation - LC51024VG-10F676C Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	32
Number of Macrocells	1024
Number of Gates	-
Number of I/O	384
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	676-BBGA
Supplier Device Package	676-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc51024vg-10f676c

Email: info@E-XFL.COM Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Figure 3. Macrocell Slice

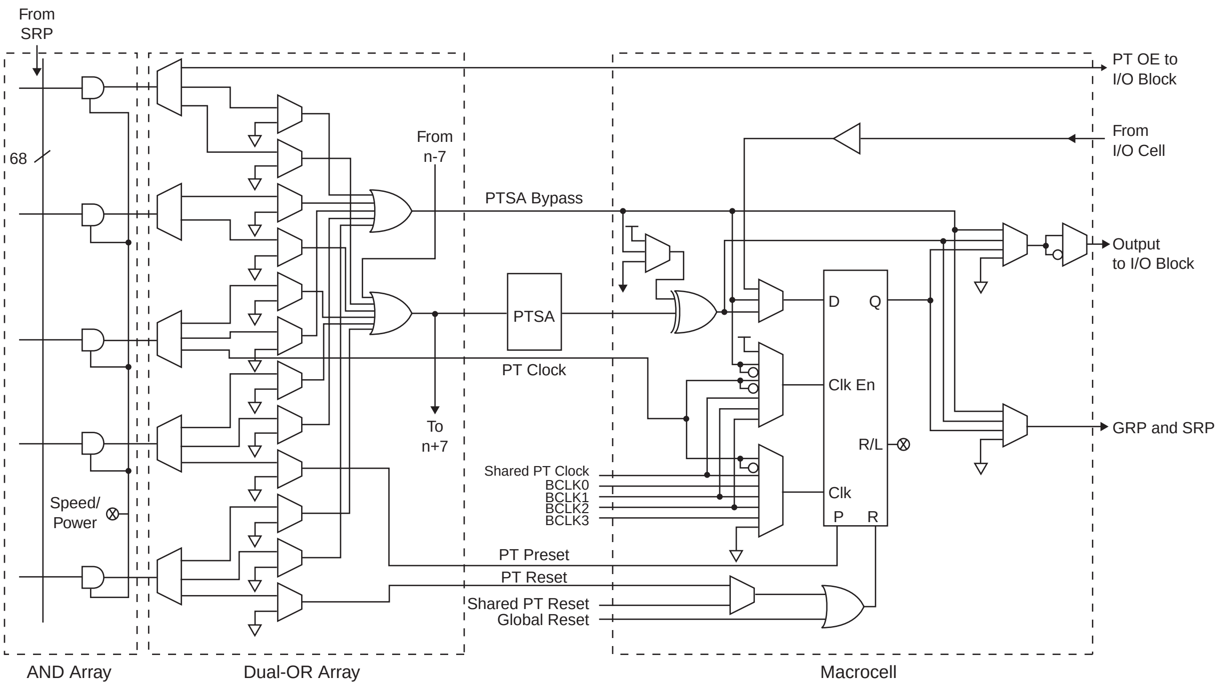
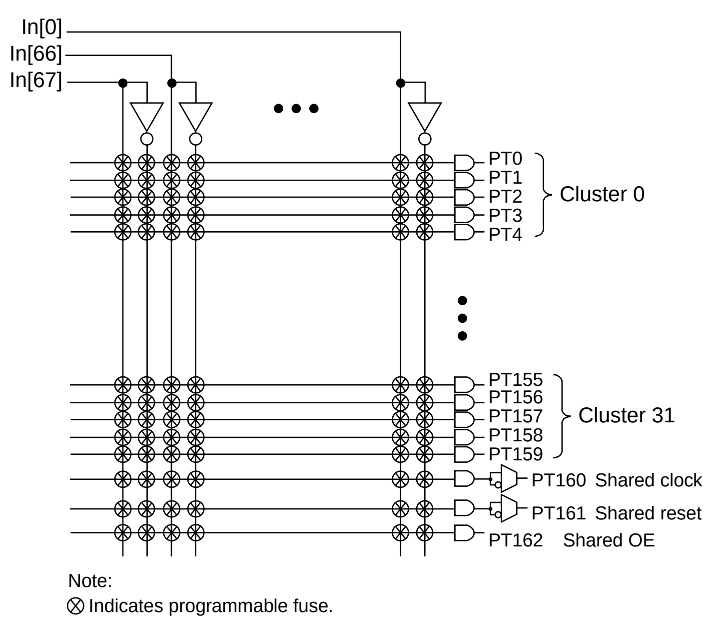
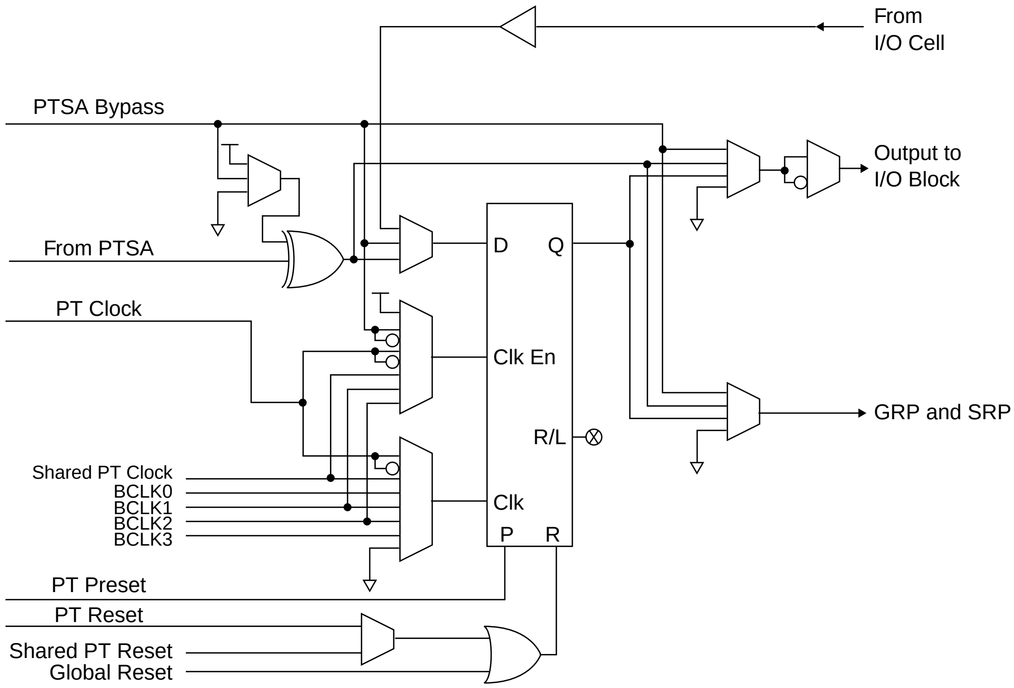


Figure 4. AND-Array



ing with PT0. There is one product term cluster for every macrocell in the GLB. In addition to the three control product terms, the first, third, fourth and fifth product terms of each cluster can be used as a PTOE (output macrocells only), PT Clock, PT Preset and PT Reset, respectively. Figure 4 is a graphical representation of the AND-Array.

Figure 7. Macrocell



I/O Cell

The I/O cell of the ispMACH 5000VG device provides a high degree of flexibility. It includes the sysIO feature and an enhanced output enable MUX for optimal performance both on- and off-chip. The sysIO feature allows I/O cells to be configured to different I/O standards, drive strengths and slew rates. The enhanced output enable MUX provides up to 14 different output enable choices per I/O cell.

The I/O cell contains an output enable (OE) MUX, a programmable tri-state output buffer, a programmable input buffer, a programmable pull-up resistor, a programmable pull-down resistor and a programmable bus-keeper latch. The I/O cell receives its input from its associated macrocell. The I/O cell has a feedback line to its associated macrocell and a direct path to the GRP and SRP.

The output enable (OE) MUX selects the OE signal per I/O cell. The inputs to the OE MUX are the four Shared PTOE signals, PTOE and the two GOE signals. The OE MUX also has the ability to choose either the true or inverse of each of these signals. The output of the OE MUX goes through a logical AND with the TOE signal to allow easy tri-stating of the outputs for testing purposes.

The four shared PTOE signals are derived from PT163 of each GLB in the segment. The PTOE signal is derived from the first product term in each macrocell cluster, which is directly routed to the OE MUX. Therefore, every I/O cell can have a different OE signal. Figure 8 is a graphical representation of the I/O cell.

Global clock pins have additional capabilities that allow for higher performance applications. Two global clock pins can be paired together to create a single global clock pin that can interface with certain differential signals.

The TOE and JTAG pins of the ispMACH 5000VG device are the only pins that do not have sysIO capabilities. These pins only support the LVTTL and LVCMOS standards.

There are three classes of I/O interface standards that are implemented in the ispMACH 5000VG devices. The first is the unterminated, single-ended interface. It includes the 3.3V LVTTL standard along with the 1.8V, 2.5V and 3.3V LVCMOS interface standards. Additionally, PCI 3.3, PCI-X and AGP-1X are all subsets of this type of interface.

The second type of interface implemented is the terminated, single-ended interface standard. This group of interfaces includes different versions of SSTL and HSTL interfaces along with CTT and GTL+. Usage of these particular I/O interfaces requires the use of an additional VREF signal. At the system level, a termination voltage, VTT, is also required. Typically, an output will be terminated to VTT at the receiving end of the transmission line it is driving.

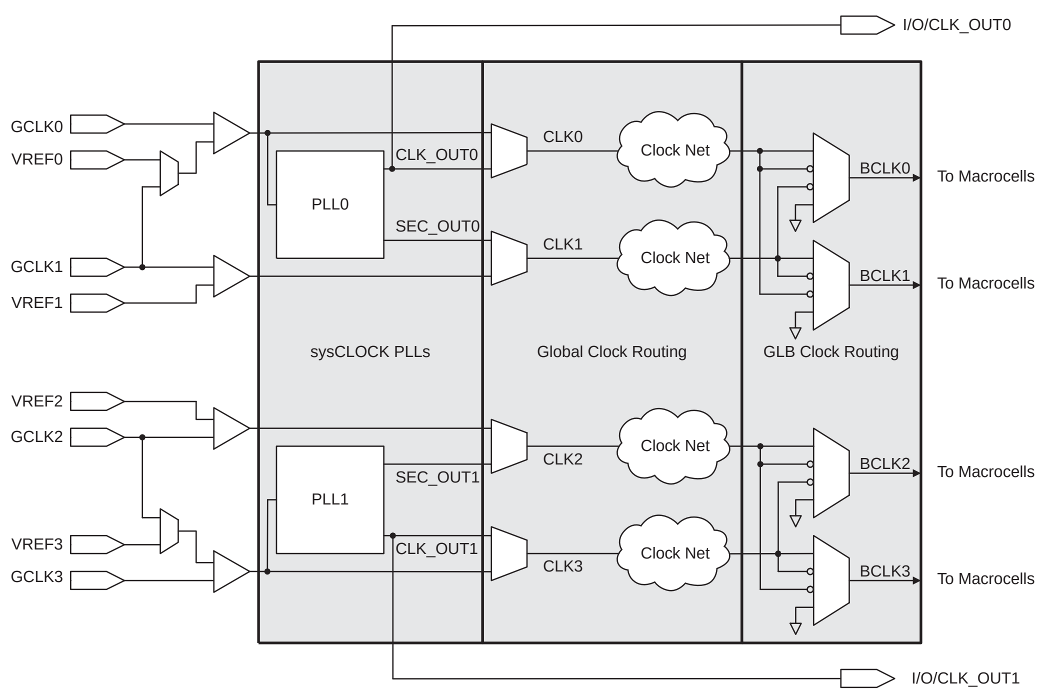
The final types of interfaces implemented are the differential standards LVDS and LVPECL. These interfaces are implemented on clock pins only. When using one of the differential standards, a pair of global clock pins (GCLK0 and GCLK1 or GCLK3 and GCLK2) is combined to create a single clock signal.

For more information on the sysIO capability, please refer to Technical Note TN1000: *ispMACH 5000VG sysIO Design and Usage Guidelines* .

GLB Clock Distribution

The ispMACH 5000VG family has four dedicated clock input pins: GCLK0-GCLK3. GLCK0 and GCLK3 can be routed through a PLL circuit or routed directly to the internal clock nets. The internal clock nets (CLK0-CLK3) are directly related to the dedicated clock pins (see Secondary Clock Divider exception when using the sysCLOCK circuit). These feed the GLB clock multiplexes which generate the GLB clock signals (BCLK0-BCLK3). The GLB clock multiplexer allows a variety of true and complementary versions of the clocks to be used within the GLB. Each block clock can be the true or inverse of its associated global clock or the inverse of the adjacent global clock. Figure 9 shows the clock distribution network.

Figure 9. Clock Distribution Network

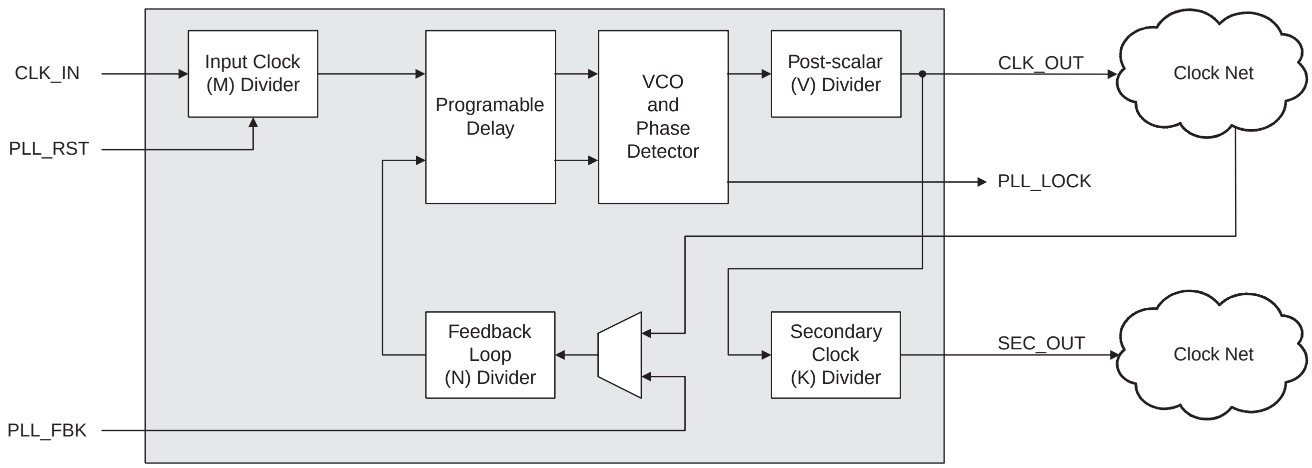


sysCLOCK PLL

The sysCLOCK PLL circuitry consists of Phase-Lock Loops (PLLs) and the various dividers, reset and feedback signals associated with the PLLs. This feature gives the user the ability to synthesize clock frequencies and generate multiple clock signals for routing within the device. Furthermore, it can generate clock signals that are deskewed either at the board level or the device level.

The ispMACH 5000VG devices provide two PLL circuits. PLL0 receives its clock inputs from GCLK 0 and provides outputs to CLK 0 (CLK 1 when using the secondary clock). PLL1 operates with signals from GCLK 3 and CLK 3 (CLK 2 when using the secondary clock). The PLL outputs (CLK_OUT) are routed via a dedicated net to a dedicated pad. Further the buffers at these dedicated pads are regular I/O buffers that can select either the I/O macrocell or the CLK_OUT (CLK_OUT0/CLK_OUT1) signal. The CLK_OUT nets are not routed through the GRP. Additionally, there are two sets of signals used for external control. Each PLL has a set of PLL_RST, PLL_FBK and PLL_LOCK signals. Figure 10 shows the ispMACH 5000VG PLL block diagram.

Figure 10. PLL Block Diagram



In order to facilitate the multiply and divide capabilities of the PLL, each PLL has dividers associated with it: M, N and K. The M divider is used to divide the clock signal, while the N divider is used to multiply the clock signal. The K divider is only used when a secondary clock output is needed. This divider divides the primary clock output and feeds to a separate global clock net. The V divider is used to provide lower frequency output clocks, while maintaining a stable, high frequency output from the PLL's VCO circuit.

The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. This operates by inserting delay on the input or feedback lines in 0.5ns increments from 0 to 3.5ns. For more information on the PLL, please refer to Technical Note TN1003: *ispMACH 5000VG PLL Usage Guidelines* .

Power Management

The ispMACH 5000VG devices provide unique power management controls. The devices have two power settings, high power and low power, on a per node basis. Low power consumption is approximately 50% of high power consumption with a timing delay adder (tLP) to the routing delay of the low power node. Each node can be configured as either high power or low power. However, care should be taken when sharing product terms between nodes with different power settings.

The ispMACH 5000VG devices also have a power-off feature for unused product terms. By default, any product term that is not used is configured as such. This allows the device to operate at minimal power consumption without affecting the timing of the design. For more information on power management, please refer to Technical Note TN1002: *Power Estimation in ispMACH 5000VG Devices*.

DC Electrical Characteristics

Over Recommended Operating Conditions

<table>
<tr><th>Symbol</th><th>Parameter</th><th colspan="2">Condition</th><th>Min</th><th>Typ</th><th>Max</th><th>Units</th></tr>
<tr><td>I_{IL}, I_{IH}[1]</td><td>Input or I/O Leakage Current</td><td colspan="2">$0V \le V_{IN} \le V_{IH}$ (MAX)</td><td>—</td><td>—</td><td>+/-10</td><td>µA</td></tr>
<tr><td rowspan="3">I_{PU}[2]</td><td rowspan="3">I/O Weak Pull-up Resistor Current</td><td rowspan="3">$0 \le V_{IN} \le 0.7\ V_{CCO}$</td><td>$V_{CCO}$ = 3.3</td><td>-30</td><td>—</td><td>-150</td><td>µA</td></tr>
<tr><td>V_{CCO} = 2.5</td><td>-20</td><td>—</td><td>-150</td><td>µA</td></tr>
<tr><td>V_{CCO} = 1.8</td><td>-10</td><td>—</td><td>-150</td><td>µA</td></tr>
<tr><td>I_{PD}[2]</td><td>I/O Weak Pull-down Resistor Current</td><td colspan="2">V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)</td><td>30</td><td>—</td><td>150</td><td>µA</td></tr>
<tr><td>I_{BHLS}[2]</td><td>Bus Hold Low Sustaining Current</td><td colspan="2">$V_{IN} = V_{IL}$ (MAX)</td><td>30</td><td>—</td><td>—</td><td>µA</td></tr>
<tr><td rowspan="3">I_{BHHS}[2]</td><td rowspan="3">Bus Hold High Sustaining Current</td><td rowspan="3">$V_{IN} = 0.7\ V_{CCO}$</td><td>V_{CCO} = 3.3</td><td>-30</td><td>—</td><td>—</td><td>µA</td></tr>
<tr><td>V_{CCO} = 2.5</td><td>-20</td><td>—</td><td>—</td><td>µA</td></tr>
<tr><td>V_{CCO} = 1.8</td><td>-10</td><td>—</td><td>—</td><td>µA</td></tr>
<tr><td>I_{BHLO}[2]</td><td>Bus Hold Low Overdrive Current</td><td colspan="2">$0V \le V_{IN} \le V_{IH}$ (MAX)</td><td>—</td><td>—</td><td>150</td><td>µA</td></tr>
<tr><td>I_{BHHO}[2]</td><td>Bus Hold High Overdrive Current</td><td colspan="2">$0V \le V_{IN} \le V_{IH}$ (MAX)</td><td>—</td><td>—</td><td>-150</td><td>µA</td></tr>
<tr><td>I_{CC}[3, 4, 5]</td><td>Operating Power Supply Current</td><td colspan="2">V_{CC} = 3.3V</td><td>—</td><td>380</td><td>—</td><td>mA</td></tr>
<tr><td>V_{BHT}</td><td>Bus Hold Trip Points</td><td colspan="2"></td><td>V_{IL} (MAX)</td><td>—</td><td>V_{IH} (MIN)</td><td>V</td></tr>
<tr><td rowspan="2">C_1</td><td rowspan="2">I/O Capacitance[3]</td><td colspan="2">V_{CC} = 3.3V, V_{IO} = 0 to V_{IH} (MAX)</td><td rowspan="2">—</td><td rowspan="2">10</td><td rowspan="2">—</td><td rowspan="2">pf</td></tr>
<tr><td colspan="2">V_{CCO} = 3.3V, 2.5, 1.8, 1.5</td></tr>
<tr><td rowspan="2">C_2</td><td rowspan="2">Clock Capacitance[3]</td><td colspan="2">V_{CC} = 3.3V, V_{IO} = 0 to V_{IH} (MAX)</td><td rowspan="2">—</td><td rowspan="2">10</td><td rowspan="2">—</td><td rowspan="2">pf</td></tr>
<tr><td colspan="2">V_{CCO} = 3.3V, 2.5, 1.8, 1.5</td></tr>
<tr><td rowspan="2">C_3</td><td rowspan="2">Global Input Capacitance[3]</td><td colspan="2">V_{CC} = 3.3V, V_{IO} = 0 to V_{IH} (MAX)</td><td rowspan="2">—</td><td rowspan="2">10</td><td rowspan="2">—</td><td rowspan="2">pf</td></tr>
<tr><td colspan="2">V_{CCO} = 3.3V, 2.5, 1.8, 1.5</td></tr>
</table>

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. Only available for LVCMOS and LVTTL standards.
3. T_A = 25°C, f = 1.0MHz.
4. Device configured with 16-bit counters.
5. I_{CC} varies with specific device configuration and operating frequency.

sysIO DC Electrical Characteristics

Over Recommended Operating Conditions

Standard	V_{IL} Min (V)	V_{IL} Max (V)	V_{IH} Min (V)	V_{IH} Max (V)	V_{OL} Max (V)	V_{OH} Min (V)	I_{OL} [2] (mA)	I_{OH} [2] (mA)
LVCMOS 3.3[1]	-0.3	0.8	2.0	5.5	0.4	2.4	20	-20
LVCMOS 3.3	-0.3	0.8	2.0	5.5	0.4	2.4	16, 12 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	5.5	0.4	2.4	20	-20
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	16, 12, 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCO}$	$0.65V_{CCO}$	3.6	0.4	V_{CCO}-0.4	12, 8, 5.33, 4	-12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
PCI 3.3	-0.3	$0.3V_{CCO}$	$0.5V_{CCO}$	3.6	$0.1V_{CCO}$	$0.9V_{CCO}$	1.5	-0.5
PCI-X	-0.3	$0.35V_{CCO}$	$0.5V_{CCO}$	3.6	$0.1V_{CCO}$	$0.9V_{CCO}$	1.5	-0.5
AGP-1X	-0.3	$0.3V_{CCO}$	$0.5V_{CCO}$	3.6	$0.1V_{CCO}$	$0.9V_{CCO}$	1.5	-0.5
SSTL3 class I	-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	0.7	V_{CCO}-1.1	8	-8
SSTL3 class II	-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	0.5	V_{CCO}-0.9	16	-16
SSTL2 class I	-0.3	V_{REF}-0.18	V_{REF}+0.18	3.6	0.54	V_{CCO}-0.62	7.6	-7.6
SSTL2 class II	-0.3	V_{REF}-0.18	V_{REF}+0.18	3.6	0.35	V_{CCO}-0.43	15.2	-15.2
CTT 3.3	-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	V_{REF}-0.4	V_{REF}+0.4	8	-8
CTT 2.5	-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	V_{REF}-0.4	V_{REF}+0.4	8	-8
HSTL class I	-0.3	V_{REF}-0.1	V_{REF}+0.1	3.6	0.4	V_{CCO}-0.4	8	-8
HSTL class III	-0.3	V_{REF}-0.1	V_{REF}+0.1	3.6	0.4	V_{CCO}-0.4	24	-8
GTL+	-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	0.6	n/a	36	n/a

1. Software default setting
2. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed 96mA.

sysIO Differential Input DC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max
V_{INP} . V_{INM}	LVDS Input voltage	—	0	2.4
V_{THD}	LVDS Differential input threshold	—	±100mV	—
V_{IL}	LVPECL Input Voltage Low	V_{CC} = 3.0 to 3.6V	V_{CC}-1.81	V_{CC}-1.48
		V_{CC} = 3.3V	1.49V	1.83V
V_{IH}	LVPECL Input Voltage High	V_{CC} = 3.0 to 3.6V	V_{CC}-1.17	V_{CC}-0.88
		V_{CC} = 3.3V	2.14V	2.42V

ispMACH 5768VG External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description[1,2,3]	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Data propagation delay, 5-PT bypass	—	5.0	—	7.5	—	10.0	—	12.0	ns
t_{PD_PTSA}	Data propagation delay, intrasegment path	—	6.0	—	9.0	—	11.5	—	13.5	ns
t_{PD_GLOBAL}	Data propagation delay, intersegment path	—	6.5	—	9.75	—	13.0	—	16.0	ns
t_S	GLB register setup time before clock, 5-PT bypass	3.0	—	5.0	—	7.5	—	9.3	—	ns
t_{S_PTSA}	GLB register setup time before clock	3.0	—	6.0	—	8.5	—	10.0	—	ns
t_{SIR}	GLB register setup time before clock, input register path	2.8	—	3.0	—	4.0	—	5.0	—	ns
t_H	GLB register hold time before clock, 5-PT bypass	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{H_PTSA}	GLB register hold time before clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time before clock, input reg. path	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	4.4	—	5.0	—	6.0	—	7.0	ns
t_R	External reset pin to output delay	—	6.5	—	9.0	—	10.0	—	10.9	ns
t_{RW}	External reset pulse duration	4.0	—	6.0	—	8.0	—	9.5	—	ns
$t_{LPTOE/DIS}$	Input to output local product term output enable/disable	—	7.0	—	9.75	—	11.5	—	13.4	ns
$t_{SPTOE/DIS}$	Input to output segment product term output enable/disable	—	8.0	—	11.25	—	17.5	—	20.4	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	6.2	—	7.5	—	8.85	—	10.0	ns
t_{CW}	Global clock width, high or low	1.6	—	2.75	—	3.6	—	4.3	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{WIR}	Input register clock width, high or low	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{SKEW}	Clock-to-out skew, block level	—	0.25	—	0.35	—	0.45	—	0.55	ns
	Clock-to-out skew, segment level	—	0.4	—	0.5	—	0.6	—	0.7	ns
f_{MAX}[4]	Clock frequency with internal feedback	178.6	—	117.0	—	87.0	—	73.0	—	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, $1/(t_{S\_PTSA} + t_{CO})$	135.1	—	90.9	—	69.0	—	58.8	—	MHz
f_{MAX} (Tog.)	Clock frequency max Toggle	312.5	—	181.0	—	138.0	—	116.0	—	MHz

Timing v.1.20

1. Timing numbers are based on default LVCMOS 3.3 I/O Buffers. Use timing adjusters provided to calculate timing for other standards.
2. Measured using standard switching circuit, assuming segment and global routing loading of 1, worst case PTSA loading and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using SRP feedback.

ispMACH 51024VG External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description[1,2,3]	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Data propagation delay, 5-PT bypass	—	5.0	—	7.5	—	10.0	—	12.0	ns
t_{PD_PTSA}	Data propagation delay, intrasegment path	—	6.0	—	9.0	—	11.5	—	13.5	ns
t_{PD_GLOBAL}	Data propagation delay, intersegment path	—	6.5	—	9.75	—	13.0	—	16.0	ns
t_S	GLB register setup time before clock, 5-PT bypass	3.0	—	5.0	—	7.5	—	9.3	—	ns
t_{S_PTSA}	GLB register setup time before clock	3.0	—	6.0	—	8.5	—	10.0	—	ns
t_{SIR}	GLB register setup time before clock, input register path	2.8	—	3.0	—	4.0	—	5.0	—	ns
t_H	GLB register hold time before clock, 5-PT bypass	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{H_PTSA}	GLB register hold time before clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time before clock, input reg. path	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	4.4	—	5.0	—	6.0	—	7.0	ns
t_R	External reset pin to output delay	—	6.5	—	9.0	—	10.0	—	10.9	ns
t_{RW}	External reset pulse duration	4.0	—	6.0	—	8.0	—	9.5	—	ns
$t_{LPTOE/DIS}$	Input to output local product term output enable/disable	—	7.0	—	9.75	—	11.5	—	13.4	ns
$t_{SPTOE/DIS}$	Input to output segment product term output enable/disable	—	8.0	—	11.25	—	17.5	—	20.4	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	6.2	—	7.5	—	8.85	—	10.0	ns
t_{CW}	Global clock width, high or low	1.6	—	2.75	—	3.6	—	4.3	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{WIR}	Input register clock width, high or low	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{SKEW}	Clock-to-out skew, block level	—	0.25	—	0.35	—	0.45	—	0.55	ns
	Clock-to-out skew, segment level	—	0.4	—	0.5	—	0.6	—	0.7	ns
f_{MAX}[4]	Clock frequency with internal feedback	178.6	—	117.0	—	87.0	—	73.0	—	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, $1/(t_{S\_PTSA} + t_{CO})$	135.1	—	90.9	—	69.0	—	58.8	—	MHz
f_{MAX} (Tog.)	Clock frequency max Toggle	312.5	—	181.0	—	138.0	—	116.0	—	MHz

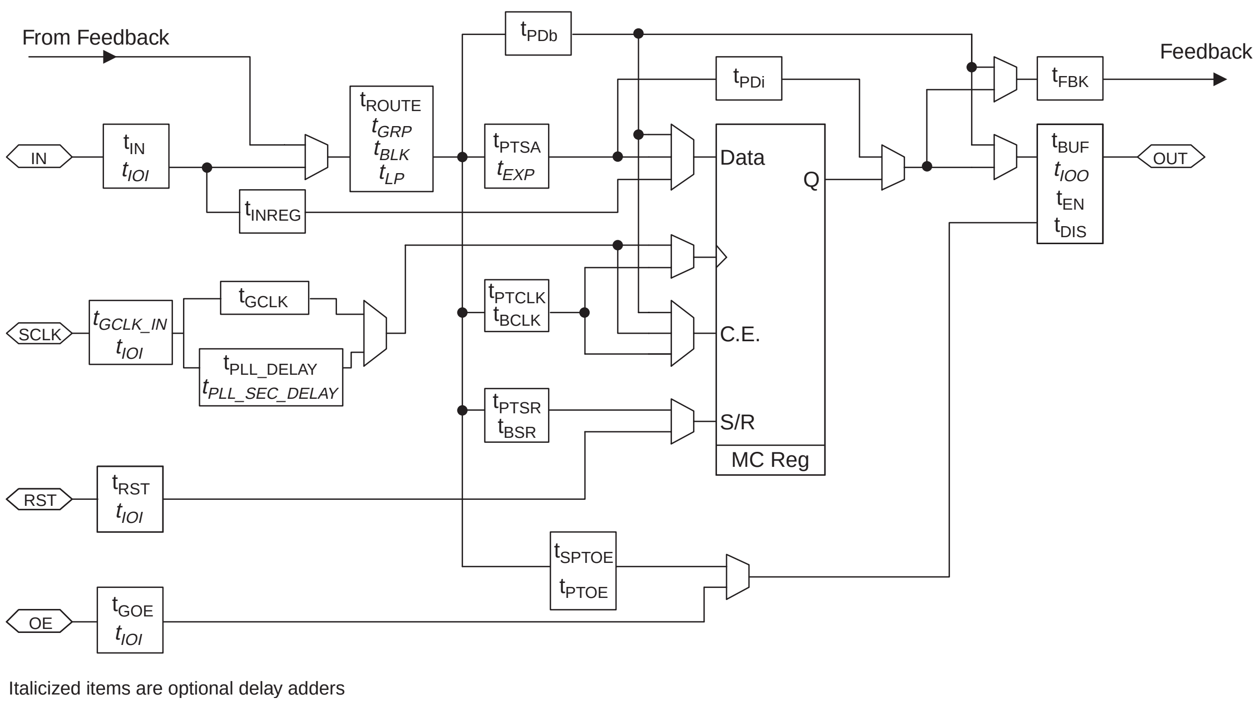
Timing v.1.10

1. Timing numbers are based on default LVCMOS 3.3 I/O Buffers. Use timing adjusters provided to calculate timing for other standards.
2. Measured using standard switching circuit, assuming segment and global routing loading of 1, worst case PTSA loading and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using SRP feedback.

Timing Model

The task of determining the timing through the ispMACH 5000VG family, like any CPLD, is relatively simple. The timing model provided in Figure 11 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, please refer to Technical Note TN1001: *ispMACH 5000VG Timing Model Design and Usage Guidelines.*

Figure 11. ispMACH 5000VG Timing Model



ispMACH 5768VG Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
In/Out Delays										
t_{IN}	Input Buffer Delay	—	0.65	—	0.95	—	1.25	—	1.40	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	0.65	—	0.95	—	1.25	—	1.40	ns
t_{GOE}	Global OE Pin Delay	—	4.05	—	5.00	—	6.00	—	7.00	ns
t_{BUF}	Delay through Output Buffer	—	1.15	—	1.50	—	1.75	—	1.90	ns
t_{EN}	Output Enable Time	—	2.15	—	2.50	—	2.85	—	3.00	ns
t_{DIS}	Output Disable Time	—	2.15	—	2.50	—	2.85	—	3.00	ns
t_{RSTb}	Global RESETbar Pin Delay	—	4.60	—	6.50	—	7.00	—	7.50	ns
Routing Delays										
t_{ROUTE}	Delay through SRP	—	2.80	—	4.20	—	5.65	—	6.90	ns
t_{PTSA}	Product Term Sharing Array Delay	—	0.40	—	1.85	—	2.35	—	2.50	ns
t_{PDB}	5-PT Bypass Propagation Delay	—	0.40	—	0.85	—	1.35	—	1.80	ns
t_{PDi}	Macrocell Propagation Delay	—	1.00	—	0.50	—	0.50	—	0.80	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	3.00	—	3.05	—	3.50	—	4.40	ns
t_{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t_{GCLK}	Global Clock Tree Delay	—	0.85	—	0.70	—	0.55	—	0.65	ns
t_{PLL_DELAY}	Programmable PLL Delay Increment	—	0.50	—	0.50	—	0.50	—	0.50	ns
$t_{PLL\_SEC\_DELAY}$	Additional Delay When Using Secondary PLL Output	—	0.60	—	0.60	—	0.60	—	0.60	ns
t_{GRP}	Global Routing Pool Delay	—	1.50	—	2.25	—	3.00	—	4.00	ns
Register/Latch Delays										
t_S	D-Register Setup Time	0.65	—	0.65	—	1.05	—	1.25	—	ns
t_{S_PT}	D-Register Setup Time with PT Clock	0.65	—	0.65	—	1.05	—	1.25	—	ns
t_H	D-Register Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{ST}	T-Register Setup Time	1.15	—	1.15	—	1.55	—	1.75	—	ns
t_{ST_PT}	T-Register Setup Time with PT Clock	1.15	—	1.15	—	1.55	—	1.75	—	ns
t_{HT}	T-Register Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	1.75	—	1.85	—	2.45	—	3.05	ns
t_{CES}	Clock Enable Setup Time	2.60	—	3.90	—	5.05	—	5.95	—	ns
t_{CEH}	Clock Enable Hold Time	0.60	—	0.90	—	1.20	—	1.45	—	ns
t_{SL}	Latch Setup Time	2.80	—	4.20	—	5.50	—	6.60	—	ns
t_{SL_PT}	Latch Setup Time with PT Clock	2.80	—	4.20	—	5.50	—	6.60	—	ns
t_{HL}	Latch Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	1.75	—	2.50	—	3.50	—	4.50	ns
t_{PDLi}	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	2.40	—	3.50	—	4.00	—	4.50	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.75	—	1.00	—	1.25	—	1.50	ns
t_{SRR}	Asynchronous Reset or Set Recovery Delay	—	1.00	—	1.50	—	2.00	—	2.50	ns
Control Delays										
t_{BCLK}	GLB PT Clock Delay	—	3.10	—	4.65	—	6.00	—	7.00	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	3.00	—	4.50	—	6.00	—	7.00	ns

ispMACH 5768VG Internal Timing Parameters (Continued)

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{BSR}	Block PT Set/Reset Delay	—	2.00	—	3.00	—	4.00	—	4.80	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	2.00	—	3.00	—	4.00	—	4.80	ns
t_{SPTOE}	Segment PT OE Delay	—	2.40	—	3.60	—	7.75	—	9.10	ns
t_{PTOE}	Macrocell PT OE Delay	—	1.40	—	2.10	—	1.75	—	2.10	ns

Notes: Timing v.1.20

1. Internal Timing Parameters are not tested and are for reference only. Refer to Timing Model in this data sheet for further details.
2. t_{PLL_DELAY} is the unit increment by which the clock signal can be incremented. The PLL can adjust the clock signal by up to 3.5ns in either direction in units of 0.5ns for each step.

ispMACH 51024VG Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
In/Out Delays										
t_{IN}	Input Buffer Delay	—	0.65	—	0.95	—	1.25	—	1.40	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	0.65	—	0.95	—	1.25	—	1.40	ns
t_{GOE}	Global OE Pin Delay	—	4.05	—	5.00	—	6.00	—	7.00	ns
t_{BUF}	Delay through Output Buffer	—	1.15	—	1.50	—	1.75	—	1.90	ns
t_{EN}	Output Enable Time	—	2.15	—	2.50	—	2.85	—	3.00	ns
t_{DIS}	Output Disable Time	—	2.15	—	2.50	—	2.85	—	3.00	ns
t_{RSTb}	Global RESETbar Pin Delay	—	4.60	—	6.50	—	7.00	—	7.50	ns
Routing Delays										
t_{ROUTE}	Delay through SRP	—	2.80	—	4.20	—	5.65	—	6.90	ns
t_{PTSA}	Product Term Sharing Array Delay	—	0.40	—	1.85	—	2.35	—	2.50	ns
t_{PDB}	5-PT Bypass Propagation Delay	—	0.40	—	0.85	—	1.35	—	1.80	ns
t_{PDi}	Macrocell Propagation Delay	—	1.00	—	0.50	—	0.50	—	0.80	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	3.00	—	3.05	—	3.50	—	4.40	ns
t_{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t_{GCLK}	Global Clock Tree Delay	—	0.85	—	0.70	—	0.55	—	0.65	ns
t_{PLL_DELAY}	Programmable PLL Delay Increment	—	0.50	—	0.50	—	0.50	—	0.50	ns
$t_{PLL\_SEC\_DELAY}$	Additional Delay When Using Secondary PLL Output	—	0.60	—	0.60	—	0.60	—	0.60	ns
t_{GRP}	Global Routing Pool Delay	—	1.50	—	2.25	—	3.00	—	4.00	ns
Register/Latch Delays										
t_S	D-Register Setup Time	0.65	—	0.65	—	1.05	—	1.25	—	ns
t_{S_PT}	D-Register Setup Time with PT Clock	0.65	—	0.65	—	1.05	—	1.25	—	ns
t_H	D-Register Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{ST}	T-Register Setup Time	1.15	—	1.15	—	1.55	—	1.75	—	ns
t_{ST_PT}	T-Register Setup Time with PT Clock	1.15	—	1.15	—	1.55	—	1.75	—	ns
t_{HT}	T-Register Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	1.75	—	1.85	—	2.45	—	3.05	ns

ispMACH 5768VG Timing Adders

Adder Type	Base Parameter	Description	-5 Min	-5 Max	-75 Min	-75 Max	-10 Min	-10 Max	-12 Min	-12 Max	Units
t_{BLA}	t_{ROUTE}	GLB Loading Adder	—	0.0	—	0.0	—	0.0	—	0.0	ns
t_{EXP}	t_{PTSA}	PT Expander Adder	—	1.5	—	2.0	—	2.5	—	2.5	ns
t_{LP}	t_{ROUTE}	Low Power Adder	—	1.5	—	1.5	—	1.5	—	1.5	ns
t_{IOI} Input Adders											
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS1.8 standard	—	0.90	—	0.90	—	0.90	—	0.90	ns
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS2.5 standard	—	0.15	—	0.15	—	0.15	—	0.15	ns
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVTTL	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVTTL standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using PCI standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_X_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using PCI_X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using AGP-1X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL3_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL3_I standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL3_II_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL3_II standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL2_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL2_I standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL2_II_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL2_II standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
CTT33_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using CTT3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
CTT25_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using CTT2.5 standard	—	0.15	—	0.15	—	0.15	—	0.15	ns
HSTL_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using HSTL_I standard	—	1.25	—	1.25	—	1.25	—	1.25	ns
HSTL_III_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using HSTL_III standard	—	1.25	—	1.25	—	1.25	—	1.25	ns
GTL+_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using GTL+ standard	—	1.50	—	1.50	—	1.50	—	1.50	ns
LVDS_in	t_{GCLK_IN}	Using LVDS standard	—	1.70	—	1.70	—	1.70	—	1.70	ns
LVPECL_in	t_{GCLK_IN}	Using LVPECL standard	—	2.10	—	2.10	—	2.10	—	2.10	ns
t_{IOO} Output Adders											
LVCMOS18_4mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V & 4mA Buffer	—	3.00	—	3.00	—	3.00	—	3.00	ns
LVCMOS18_5mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V & 5.33mA Buffer	—	2.50	—	2.50	—	2.50	—	2.50	ns
LVCMOS18_8mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V & 8mA Buffer	—	1.85	—	1.85	—	1.85	—	1.85	ns

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.1.20

ispMACH 5768VG Timing Adders (Continued)

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
LVCMOS18_12mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V & 12mA Buffer	—	1.35	—	1.35	—	1.35	—	1.35	ns
LVCMOS25_4mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 4mA Buffer	—	1.50	—	1.50	—	1.50	—	1.50	ns
LVCMOS25_5mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 5.33mA Buffer	—	1.25	—	1.25	—	1.25	—	1.25	ns
LVCMOS25_8mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 8mA Buffer	—	0.70	—	0.70	—	0.70	—	0.70	ns
LVCMOS25_12mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 12mA Buffer	—	0.50	—	0.50	—	0.50	—	0.50	ns
LVCMOS25_16mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 16mA Buffer	—	0.25	—	0.25	—	0.25	—	0.25	ns
LVCMOS33_4mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 4mA Buffer	—	1.50	—	1.50	—	1.50	—	1.50	ns
LVCMOS33_5mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 5.33mA Buffer	—	1.25	—	1.25	—	1.25	—	1.25	ns
LVCMOS33_8mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 8mA Buffer	—	0.40	—	0.40	—	0.40	—	0.40	ns
LVCMOS33_12mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 12mA Buffer	—	0.10	—	0.10	—	0.10	—	0.10	ns
LVCMOS33_16mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 16mA Buffer	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS33_20mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 20mA Buffer	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVTTL	t_{BUF}, t_{EN}, t_{DIS}	Output configured as LVTTL Buffer	—	0.0	—	0.0	—	0.0	—	0.0	ns
Slow Slew	t_{BUF}, t_{EN}	Output configured for slow slew rate	—	1.50	—	1.50	—	1.50	—	1.50	ns
PCI_out	t_{BUF}, t_{EN}, t_{DIS}	Using PCI standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_X_out	t_{BUF}, t_{EN}, t_{DIS}	Using PCI-X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_out	t_{BUF}, t_{EN}, t_{DIS}	Using AGP-1X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL3_I_out	t_{BUF}, t_{EN}, t_{DIS}	Using SSTL3_I standard	—	-0.25	—	-0.25	—	-0.25	—	-0.25	ns
SSTL3_II_out	t_{BUF}, t_{EN}, t_{DIS}	Using SSTL3_II standard	—	-0.35	—	-0.35	—	-0.35	—	-0.35	ns
SSTL2_I_out	t_{BUF}, t_{EN}, t_{DIS}	Using SSTL2_I standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL2_II_out	t_{BUF}, t_{EN}, t_{DIS}	Using SSTL2_II standard	—	-0.25	—	-0.25	—	-0.25	—	-0.25	ns
CTT33_out	t_{BUF}, t_{EN}, t_{DIS}	Using CCT3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
CTT25_out	t_{BUF}, t_{EN}, t_{DIS}	Using CCT2.5 standard	—	0.25	—	0.25	—	0.25	—	0.25	ns
HSTL_I_out	t_{BUF}, t_{EN}, t_{DIS}	Using HSTL_I standard	—	-0.30	—	-0.30	—	-0.30	—	-0.30	ns

Note: Open drain timing is the same as corresponding LVCMOS timing.

Timing v.1.20

ispMACH 5768VG Logic Signal Connections

Bank No.	Signal	256 fpBGA	484 fpBGA
0	0C-30	C8	D11
0	0C-28	B6	B11
0	0C-26	A5	E12
0	0C-24	D8	C11
0	0C-22	E8	F12
0	0C-20	B5	B10
0	GNDIO0	GND	GND
0	0C-18	A4	A10
0	0C-16	D7	D10
0	0C-14/VREF0	E7	A9
0	0C-12	C6	E11
0	0C-10	B4	B9
0	0C-8	A3	F11
0	0C-6	NC	A8
0	0C-4	NC	C10
0	0C-2	NC	A7
0	0C-0	NC	E10
0	0D-30	NC	B8
0	0D-28	NC	C8
0	GNDIO0	GND	GND
0	0D-26	NC	F10
0	0D-24	NC	A6
0	0D-22	NC	F9
0	0D-20	NC	C7
0	0D-18	NC	D9
0	0D-16	NC	B7
0	0D-14	D6	E8
0	0D-12	E6	A5
0	0D-10	A2	F8
0	0D-8	B3	C6
0	0D-6	C4	D8
0	0D-4	D5	A3
0	GNDIO0	GND	GND
0	0D-2	NC	A2
0	0D-0	NC	A4
0	0A-0	NC	F7
0	0A-2	NC	C5
0	0A-4	NC	F6
0	0A-6	NC	B3
0	0A-8	NC	NC
0	0A-10	NC	NC
0	GNDIO0	GND	GND
0	0A-12	NC	NC

Bank No.	Signal	256 fpBGA	484 fpBGA
0	0A-14	NC	NC
0	0A-16	NC	B4
0	0A-18	NC	D5
0	0A-20	NC	B1
0	0A-22	NC	D6
0	0A-24	NC	C4
0	0A-26	NC	E4
0	GNDIO0	GND	GND
0	0A-28	B2	C2
0	0A-30	B1	C1
0	0B-30	C2	D1
0	0B-28	C1	D2
0	0B-26	NC	D3
0	0B-24	NC	E1
0	0B-22	NC	E3
0	0B-20	NC	F4
0	0B-18	NC	F1
0	0B-16	NC	F3
0	0B-14	NC	G6
0	0B-12	NC	G1
0	GNDIO0	GND	GND
0	0B-10	NC	G2
0	0B-8	NC	H1
0	0B-6	NC	G3
0	0B-4	NC	H2
0	0B-2	NC	H5
0	0B-0	NC	H6
0	1A-0	F7	J1
0	1A-2	F6	K1
0	1A-4	E5	H3
0	1A-6	D4	J2
0	1A-8	D3	H4
0	1A-10	D2	K2
0	GNDIO0	GND	GND
0	1A-12	D1	J6
0	1A-14	E4	L1
0	1A-16	NC	K3
0	1A-18	NC	J4
0	1A-20	NC	L2
0	1A-22	NC	M1
0	1A-24	NC	K6
0	1A-26	NC	K4
0	1A-28	NC	L3

ispMACH 5768VG Logic Signal Connections (Continued)

Bank No.	Signal	256 fpBGA	484 fpBGA
3	4B-24	G11	M19
3	4B-26	F11	M21
3	4B-28	F10	L19
3	4B-30/CLK_OUT1	B11	L20
3	GNDIO3	GND	GND
3	4A-30	NC	M17
3	4A-28	NC	M22
3	4A-26	NC	K20
3	4A-24	NC	L18
3	4A-22	NC	L21
3	4A-20	NC	K19
3	4A-18	NC	L22
3	4A-16	NC	K17
3	4A-14	E13	K22
3	4A-12	B12	L17
3	GNDIO3	GND	GND
3	4A-10	E15	K21
3	4A-8	D15	K18
3	4A-6	NC	J17
3	4A-4	NC	J19
3	4A-2	D16	J22
3	4A-0	E12	J21
3	5B-0	NC	H19
3	5B-2	NC	H20
3	5B-4	NC	H17
3	5B-6	NC	H18
3	5B-8	NC	H22
3	5B-10	NC	H21
3	GNDIO3	GND	GND
3	5B-12	NC	G20
3	5B-14	NC	G22
3	5B-16	NC	G17
3	5B-18	NC	G21
3	5B-20	NC	F19
3	5B-22	NC	F20
3	5B-24	A16	F22
3	5B-26	B15	E22
3	5B-28	A15	E19
3	5B-30	D13	E20
3	5A-30	B14	D22
3	5A-28	B16	D21
3	GNDIO3	GND	GND
3	5A-26	C16	D20

Bank No.	Signal	256 fpBGA	484 fpBGA
3	5A-24	C15	C22
3	5A-22	D14	C18
3	5A-20	A14	C19
3	5A-18	C13	D17
3	5A-16	B13	C21
3	5A-14	NC	NC
3	5A-12	NC	NC
3	GNDIO3	GND	GND
3	5A-10	NC	NC
3	5A-8	NC	NC
3	5A-6	NC	B22
3	5A-4	NC	D18
3	5A-2	NC	B20
3	5A-0	NC	F17
3	5D-0	NC	B19
3	5D-2	NC	C17
3	GNDIO3	GND	GND
3	5D-4	NC	A21
3	5D-6	NC	D15
3	5D-8	NC	A20
3	5D-10	NC	C16
3	5D-12	NC	A19
3	5D-14	NC	F16
3	5D-16	NC	B16
3	5D-18	NC	D14
3	5D-20	NC	A18
3	5D-22	A13	F15
3	5D-24	A12	A17
3	5D-26	A11	B15
3	GNDIO3	GND	GND
3	5D-28	A10	A16
3	5D-30	C11	F14
3	5C-0	A9	C15
3	5C-2	D12	D13
3	5C-4	D11	E15
3	5C-6	B10	F13
3	5C-8	B9	B14
3	5C-10	E11	E13
3	5C-12/VREF3	A8	A15
3	5C-14	D10	D12
3	5C-16	E10	A14
3	5C-18	A7	B13
3	GNDIO3	GND	GND

ispMACH 51024VG Logic Signal Connections (Continued)

Bank No.	Signal	484 fpBGA	676 fpBGA
1	3A-4	V4	AJ4
1	3A-2	U7	AK3
1	3A-0	AB2	AK4
1	3D-0	V7	AJ5
1	3D-2	AA5	AH6
1	GNDIO1	GND	GND
1	3D-4	AB3	AF8
1	3D-6	Y6	AG7
1	3D-8	AB4	AK5
1	3D-10	Y7	AJ6
1	3D-12	AB5	AH7
1	3D-14	V8	AK6
1	3D-16	AA7	AJ7
1	3D-18	Y8	AH8
1	3D-20	AB6	AG9
1	3D-22	W8	AK7
1	3D-24	AA8	AF10
1	3D-26	Y10	AJ8
1	GNDIO1	GND	GND
1	3D-28	U8	AH9
1	3D-30	AB7	AK8
1	3C-0	U9	AJ9
1	3C-2	AA9	AH10
1	3C-4	W9	AK9
1	3C-6	AB8	AG11
1	3C-8	U10	AJ10
1	3C-10	AB9	AF12
1	3C-12	V11	AH11
1	3C-14/VREF1	AA10	AK10
1	3C-16	V10	AJ11
1	3C-18	AB10	AK11
1	GNDIO1	GND	GND
1	3C-20	W10	AH12
1	3C-22	W11	AJ12
1	3C-24	U11	AK12
1	3C-26	AA11	AH13
1	3C-28	V12	AJ13
1	3C-30	AB11	AK13
2	4C-30	W12	AK18
2	4C-28	Y11	AK19
2	4C-26	Y12	AJ19
2	4C-24	AB12	AH19
2	4C-22	U12	AK20
2	4C-20	AA12	AJ20
2	GNDIO2	GND	GND
2	4C-18	Y13	AK21
2	4C-16	AB13	AH20
2	4C-14	W13	AF19
2	4C-12/VREF2	AA13	AJ21
2	4C-10	U13	AG20
2	4C-8	AB14	AK22
2	4C-6	V13	AH21
2	4C-4	AA14	AJ22
2	4C-2	U14	AK23
2	4C-0	AB15	AH22
2	4D-30	Y15	AJ23
2	4D-28	AB16	AK24
2	GNDIO2	GND	GND
2	4D-26	AA15	AF21
2	4D-24	W14	AG22
2	4D-22	AB17	AH23
2	4D-20	Y16	AJ24
2	4D-18	AA16	AK25
2	4D-16	Y17	AH24
2	4D-14	AB18	AJ25
2	4D-12	V15	AK26
2	4D-10	AB19	AJ26
2	4D-8	W15	AH25
2	4D-6	AB20	AG24
2	4D-4	AA18	AF23
2	GNDIO2	GND	GND
2	4D-2	U15	AK27
2	4D-0	W17	AK28
2	4A-0	U16	AJ27
2	4A-2	AA19	AH26
2	4A-4	V16	AE23
2	4A-6	AB21	AK29
2	4A-8	NC	AJ28
2	4A-10	NC	AH27
2	GNDIO2	GND	GND
2	4A-12	NC	AG26
2	4A-14	NC	AF25
2	4A-16	Y18	AJ29
2	4A-18	W18	AG27
2	4A-20	AA20	AJ30
2	4A-22	W19	AH29

ispMACH 51024VG Logic Signal Connections (Continued)

Bank No.	Signal	484 fpBGA	676 fpBGA
2	4A-24	Y19	AE25
2	4A-26	V19	AG28
2	GNDIO2	GND	GND
2	4A-28	Y21	AF27
2	4A-30	W20	AE26
2	4B-30	AA22	AH30
2	4B-28	W21	AG29
2	4B-26	Y22	AF28
2	4B-24	V20	AG30
2	4B-22	V21	AF29
2	4B-20	W22	AC25
2	4B-18	V18	AE28
2	4B-16	U20	AF30
2	4B-14	V22	AD27
2	4B-12	U19	AE29
2	GNDIO2	GND	GND
2	4B-10	U17	AC26
2	4B-8	U22	AD28
2	4B-6	T20	AE30
2	4B-4	T21	AD29
2	4B-2	T17	AC28
2	4B-0	R20	AD30
2	5A-0	NC	AC29
2	5A-2	NC	AB27
2	5A-4	NC	AC30
2	5A-6	NC	AB28
2	5A-8	NC	AA26
2	5A-10	NC	AB29
2	GNDIO2	GND	GND
2	5A-12	NC	AB30
2	5A-14	NC	AA28
2	5A-16	NC	AA29
2	5A-18	NC	AA30
2	5A-20	NC	Y27
2	5A-22	NC	Y28
2	5A-24	NC	Y29
2	5A-26	NC	W26
2	5A-28	NC	Y30
2	5A-30	NC	W28
2	GNDIO2	GND	GND
2	5B-30	NC	W29
2	5B-28	NC	W30
2	5B-26	NC	V25

Bank No.	Signal	484 fpBGA	676 fpBGA
2	5B-24	NC	V26
2	5B-22	NC	V27
2	5B-20	NC	V28
2	5B-18	NC	V29
2	5B-16	NC	V30
2	5B-14	NC	U25
2	5B-12	NC	U27
2	GNDIO2	GND	GND
2	5B-10	NC	U28
2	5B-8	NC	U29
2	5B-6	NC	U30
2	5B-4	NC	T27
2	5B-2	NC	T28
2	5B-0	NC	T29
3	6B-0	R21	T30
3	6B-2	T22	R29
3	6B4/PLL_FBK1	P21	R27
3	6B6/PLL_RST1	N20	R28
3	6B-8	R22	R30
3	6B-10	N21	P30
3	GNDIO3	GND	GND
3	6B-12	M18	P29
3	6B-14	N19	P28
3	6B-16	P22	P27
3	6B-18	M20	N30
3	6B-20	N22	N29
3	6B-22	N17	N28
3	6B-24	M19	N27
3	6B-26	M21	N25
3	6B-28	L19	M30
3	6B-30/CLK_OUT1	L20	M29
3	GNDIO3	GND	GND
3	6A-30	M17	M28
3	6A-28	M22	L30
3	6A-26	K20	M26
3	6A-24	L18	L29
3	6A-22	L21	L28
3	6A-20	K19	L27
3	6A-18	L22	K30
3	6A-16	K17	K29
3	6A-14	K22	K28
3	6A-12	L17	J30
3	GNDIO3	GND	GND

ispMACH 51024VG Logic Signal Connections (Continued)

Bank No.	Signal	484 fpBGA	676 fpBGA
—	TMS	T1	T4
—	TOE	T18	U26

Signal Configuration

ispMACH 51024VG 676-ball fpBGA

	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC[1]	NC[1]	NC[1]	NC[1]	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	A
B	I/O	VCC	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC[1]	NC[1]	NC[1]	NC[1]	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	I/O	B
C	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	I/O	I/O/ VREF0	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	I/O	I/O	C
D	I/O	I/O	I/O	I/O	I/O	VCC	I/O	GND	I/O	VCC	I/O	VCC	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	VCC	I/O	VCC	I/O	GND	I/O	VCC	I/O	I/O	I/O	I/O	I/O	D
E	I/O	I/O	I/O	I/O	VCCO3	I/O	VCCO3	I/O	VCCO3	I/O	VCCO3	I/O/ VREF3	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	I/O	VCCO0	I/O	VCCO0	I/O	VCCO0	I/O	VCCO0	I/O	I/O	I/O	I/O	E
F	I/O	I/O	I/O	VCC	I/O	I/O	GND	I/O	GND	VCCO3	GND	GND	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	GND	GND	VCCO0	GND	I/O	GND	I/O	I/O	VCC	I/O	I/O	I/O	F
G	I/O	I/O	I/O	I/O	VCCO3	GND																			GND	VCCO0	I/O	I/O	I/O	I/O	G
H	I/O	I/O	I/O	GND	I/O	I/O																			I/O	I/O	GND	I/O	I/O	I/O	H
J	I/O	I/O	I/O	I/O	VCCO3	GND																			GND	VCCO0	I/O	I/O	I/O	I/O	J
K	I/O	I/O	I/O	VCC	I/O	VCCO3																			VCCO0	I/O	VCC	I/O	I/O	I/O	K
L	I/O	I/O	I/O	I/O	VCCO3	GND					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					GND	VCCO0	I/O	I/O	I/O	I/O	L
M	I/O	I/O/ CLK_OUT1	I/O	VCC	I/O	GND					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					GND	I/O	VCC	I/O	I/O/ CLK_OUT0	I/O	M
N	I/O	I/O	I/O	I/O	VCCP1	I/O					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					I/O	I/O	I/O	I/O	I/O	I/O	N
P	I/O	I/O	I/O	I/O	GCLK3	GNDP1					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					I/O	VCCP0	I/O	I/O	I/O	I/O/ PLL_RST0	P
R	I/O	I/O	I/O/ PLL_RST1	I/O/ PLL_FBK1	GOE1	GCLK2					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					GNDP0	GCLK0	I/O/ PLL_FBK0	I/O	I/O	I/O	R
T	I/O	I/O	I/O	I/O	GOE0	RESETB					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					GCLK1	TDI	TMS	I/O	I/O	I/O	T
U	I/O	I/O	I/O	I/O	TOE	I/O					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					VCCJ	TCK	I/O	I/O	I/O	I/O	U
V	I/O	I/O	I/O	I/O	I/O	I/O					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					I/O	TDO	I/O	I/O	I/O	I/O	V
W	I/O	I/O	I/O	VCC	I/O	GND					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					GND	I/O	VCC	I/O	I/O	I/O	W
Y	I/O	I/O	I/O	I/O	VCCO2	GND					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					GND	VCCO1	I/O	I/O	I/O	I/O	Y
AA	I/O	I/O	I/O	VCC	I/O	VCCO2																			VCCO1	I/O	VCC	I/O	I/O	I/O	AA
AB	I/O	I/O	I/O	I/O	VCCO2	GND																			GND	VCCO1	I/O	I/O	I/O	I/O	AB
AC	I/O	I/O	I/O	GND	I/O	I/O																			I/O	I/O	GND	I/O	I/O	I/O	AC
AD	I/O	I/O	I/O	I/O	VCCO2	GND																			GND	VCCO1	I/O	I/O	I/O	I/O	AD
AE	I/O	I/O	I/O	VCC	I/O	I/O	GND	I/O	GND	VCCO2	GND	GND	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	GND	GND	VCCO1	GND	I/O	GND	I/O	I/O	VCC	I/O	I/O	I/O	AE
AF	I/O	I/O	I/O	I/O	VCCO2	I/O	VCCO2	I/O	VCCO2	I/O	VCCO2	I/O	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	I/O	VCCO1	I/O	VCCO1	I/O	VCCO1	I/O	VCCO1	I/O	I/O	I/O	I/O	AF
AG	I/O	I/O	I/O	I/O	I/O	VCC	I/O	GND	I/O	VCC	I/O	VCC	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	VCC	I/O	VCC	I/O	GND	I/O	VCC	I/O	I/O	I/O	I/O	I/O	AG
AH	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	I/O	I/O	AH
AJ	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O/ VREF2	I/O	I/O	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCC	I/O	AJ
AK	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC[1]	NC[1]	NC[1]	NC[1]	I/O	I/O	I/O	I/O/ VREF1	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	AK
	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

ispMACH 51024VG

Bottom View

676BGA/51024VG

1. NCs are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.

Industrial

Part Number	Package	Pin Count	Macrocells	Tpd	Voltage
LC51024VG-75F484I	fpBGA	484	1024	7.5	3.3
LC51024VG-10F484I	fpBGA	484	1024	10	3.3
LC51024VG-12F484I	fpBGA	484	1024	12	3.3
LC51024VG-75F676I	fpBGA	676	1024	7.5	3.3
LC51024VG-10F676I	fpBGA	676	1024	10	3.3
LC51024VG-12F676I	fpBGA	676	1024	12	3.3
LC5768VG-75F256I	fpBGA	256	768	7.5	3.3
LC5768VG-10F256I	fpBGA	256	768	10	3.3
LC5768VG-12F256I	fpBGA	256	768	12	3.3
LC5768VG-75F484I	fpBGA	484	768	7.5	3.3
LC5768VG-10F484I	fpBGA	484	768	10	3.3
LC5768VG-12F484I	fpBGA	484	768	12	3.3

Note: the ispMACH 5000VG family is dual-marked with both Commercial and Industrial grades. The Commercial speed grade is one speed grade faster (i.e. LC51024VG-75F484C) than the Industrial speed grade (i.e. LC51024VG-10F484I).

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 5000VG family:

- *ispMACH 5000VG sysIO Design and Usage Guidelines* (TN1000)
- *ispMACH 5000VG Timing Model Design and Usage Guidelines* (TN1001)
- *Power Estimation in ispMACH 5000VG Devices* (TN1002)
- *ispMACH 5000VG PLL Usage Guidelines* (TN1003)