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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	12 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	32
Number of Macrocells	1024
Number of Gates	-
Number of I/O	384
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	676-BBGA
Supplier Device Package	676-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc51024vg-12f676i

The ispMACH5000VG devices also contain sysCLOCK Phase Locked Loops (PLLs) that provide designers with increased clocking flexibility. The PLLs can be used to synthesize new clocks for use on-chip or elsewhere within the system. They can also be used to deskew clocks, again both at the chip and system levels. A variable delay line capability further improves this and allows designers to retard or advance the clock in order to tune set-up and clock-to-out times for optimal results. The ispMACH 5000VG Family Selection Guide (Table 1) details the key attributes and packages for the ispMACH 5000VG devices.

ispMACH 5000VG Architecture

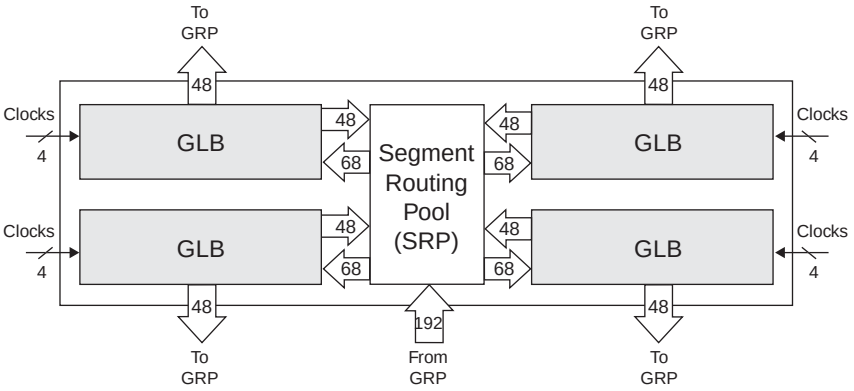
The ispMACH 5000VG Family of In-System Programmable High Density Logic Devices is based on segments containing four Generic Logic Blocks (GLBs) and a hierarchical routing pool (GRP) structure interconnecting the segments. A segment routing pool (SRP) connects each GLB in a segment allowing the maximum flexibility and speed.

Outputs from the GLBs drive the Segment Routing Pool (SRP) and the Global Routing Pool (GRP). Enhanced switching resources are provided to allow signals in the Segment Routing Pool to drive any or all the GLBs in the segment. Optimal switching is provided to allow all signals in the Global Routing Pool to be routed to any or all SRPs. This mechanism allows fast, efficient connections across the entire device.

Segment

Each segment contains four GLBs and a segment routing pool (SRP). Each GLB has 32 internal feedback outputs and 16 external feedback outputs, for a total of 48 outputs from each GLB feeding the SRP. The SRP contains up to 384 signals, 48 from each GLB and 192 from the GRP, with full routing capability. This routing scheme maximizes the flexibility and speed of the device without sacrificing the routing.

Figure 2. Segment



Generic Logic Block

Each GLB contains 32 macrocells and a fully populated, programmable AND-array with 160 logic product terms and three control product terms. The GLB has 68 inputs from the Segment Routing Pool, which are available in both true and complement form for every product term. The three control product terms are used for shared reset, clock and output enable functions. Figure 3 shows the structure of the GLB from the macrocell perspective. This is referred to as a macrocell slice. There are 32 macrocell slices per GLB.

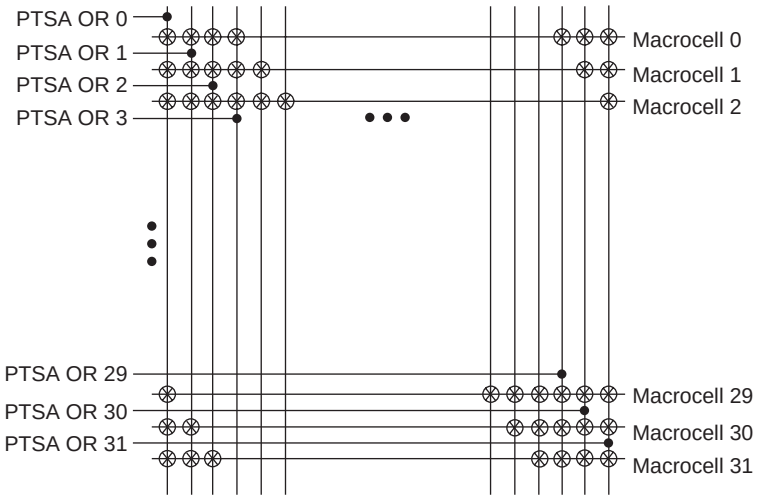
AND-Array

The programmable AND-Array consists of 68 inputs and 163 output product terms. The 68 inputs from the SRP are used to form 136 lines in the AND-Array (true and complement of the inputs). Each line in the array can be connected to any of the 163 output product terms via a wired AND. Each of the 160 logic product terms feed the Dual-OR Array with the remaining three control product terms feeding the Shared PT Clock, Shared PT Reset and Shared PT OE. Every set of five product terms from the 160 logic product terms forms a product term cluster start-

Product Term Sharing Array

The Product Term Sharing Array (PTSA) consists of 32 inputs from the Dual-OR Array (Expandable PTSA OR) and 32 outputs directly to the macrocells. Each output is the OR term of any combination of the seven Expandable PTSA OR terms connected to that output. Every Nth macrocell is connected to N-3, N-2, N-1, N, N+1, N+2 and N+3 PTSA OR terms via a programmable connection. This wraps around the logic, Macrocell 0 gets its logic from 29, 30, 31, 0, 1, 2, 3. The Expandable PTSA OR used in conjunction with the PTSA allows wide functions to be implemented easily and efficiently. Without using the Expandable PTSA OR capability, the greatest number of product terms that can be included in a single function with one pass of delay is 35. Figure 6 shows the graphical representation of the PTSA.

Figure 6. Product Term Sharing Array



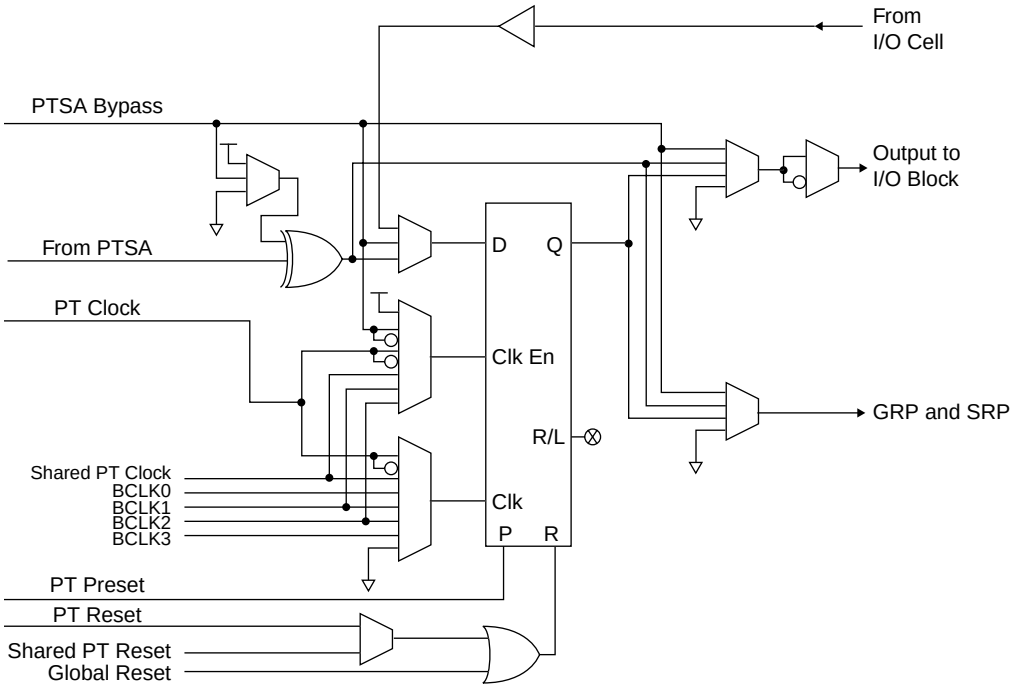
Macrocell

The 32 registered macrocells in the GLB are driven by the 32 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation.

The macrocells each have two outputs, which can be fed to the SRP, GRP and I/O cell. This dual or concurrent output capability from the macrocell gives efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function. A direct register input from the I/O cell facilitates efficient use of the macrocell to construct high-speed input registers.

Macrocell registers can be clocked from one of several global or product term clocks available on the device. A global and product term clock enable is also provided, eliminating the need to gate the clock to the macrocell registers directly. Reset and preset for the macrocell register is provided from both global and product term signals. The macrocell register can be programmed to operate as a D-type register or a D-type latch. Figure 7 is a graphical representation of the ispMACH 5000VG macrocell.

Figure 7. Macrocell



I/O Cell

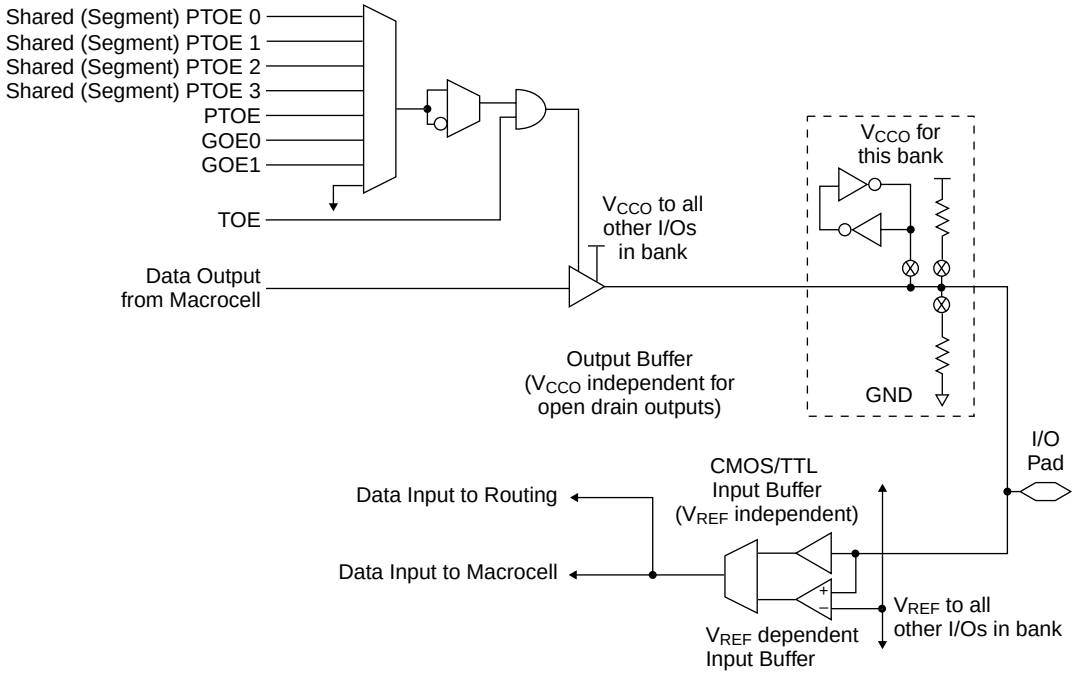
The I/O cell of the ispMACH 5000VG device provides a high degree of flexibility. It includes the sysIO feature and an enhanced output enable MUX for optimal performance both on- and off-chip. The sysIO feature allows I/O cells to be configured to different I/O standards, drive strengths and slew rates. The enhanced output enable MUX provides up to 14 different output enable choices per I/O cell.

The I/O cell contains an output enable (OE) MUX, a programmable tri-state output buffer, a programmable input buffer, a programmable pull-up resistor, a programmable pull-down resistor and a programmable bus-keeper latch. The I/O cell receives its input from its associated macrocell. The I/O cell has a feedback line to its associated macrocell and a direct path to the GRP and SRP.

The output enable (OE) MUX selects the OE signal per I/O cell. The inputs to the OE MUX are the four Shared PTOE signals, PTOE and the two GOE signals. The OE MUX also has the ability to choose either the true or inverse of each of these signals. The output of the OE MUX goes through a logical AND with the TOE signal to allow easy tri-stating of the outputs for testing purposes.

The four shared PTOE signals are derived from PT163 of each GLB in the segment. The PTOE signal is derived from the first product term in each macrocell cluster, which is directly routed to the OE MUX. Therefore, every I/O cell can have a different OE signal. Figure 8 is a graphical representation of the I/O cell.

Figure 8. I/O Cell



sysIO Capability

The ispMACH 5000VG devices are divided into four sysIO banks, where each bank is capable of supporting 14 different I/O standards. Each sysIO bank has its own I/O supply voltage (V_{CCO}) and reference voltage (V_{REF}) resources allowing each bank complete independence from the others. Each I/O within a bank is individually configurable based on the V_{CCO} and V_{REF} settings. Table 2 lists the sysIO standards with the typical values for V_{CCO}, V_{REF} and V_{TT}.

Table 2. ispMACH 5000VG Supported I/O Standards

sysIO Standard	V_{CCO}	V_{REF}	V_{TT}
LVTTL	3.3V	N/A	N/A
LVCMOS-3.3	3.3V	N/A	N/A
LVCMOS-2.5	2.5V	N/A	N/A
LVCMOS-1.8	1.8V	N/A	N/A
PCI 3.3	3.3V	N/A	N/A
PCI-X	3.3V	N/A	N/A
AGP-1X	3.3V	N/A	N/A
SSTL3, Class I & II	3.3V	1.5V	1.5V
SSTL2, Class I & II	2.5V	1.25V	1.25V
CTT 3.3	3.3V	1.5V	1.5V
CTT 2.5	2.5V	1.25V	1.25V
HSTL, Class I	1.5V	0.75V	0.75V
HSTL, Class III	1.5V	0.9V	1.5V
GTL+	N/A	1.0V	1.5V
LVPECL, Differential[1]	N/A	N/A	N/A
LVDS[1]	N/A	N/A	N/A

1. LVDS and LVPECL are only supported on the dedicated clock pins.

Global clock pins have additional capabilities that allow for higher performance applications. Two global clock pins can be paired together to create a single global clock pin that can interface with certain differential signals.

The TOE and JTAG pins of the ispMACH 5000VG device are the only pins that do not have sysIO capabilities. These pins only support the LVTTL and LVCMOS standards.

There are three classes of I/O interface standards that are implemented in the ispMACH 5000VG devices. The first is the unterminated, single-ended interface. It includes the 3.3V LVTTL standard along with the 1.8V, 2.5V and 3.3V LVCMOS interface standards. Additionally, PCI 3.3, PCI-X and AGP-1X are all subsets of this type of interface.

The second type of interface implemented is the terminated, single-ended interface standard. This group of interfaces includes different versions of SSTL and HSTL interfaces along with CTT and GTL+. Usage of these particular I/O interfaces requires the use of an additional VREF signal. At the system level, a termination voltage, VTT, is also required. Typically, an output will be terminated to VTT at the receiving end of the transmission line it is driving.

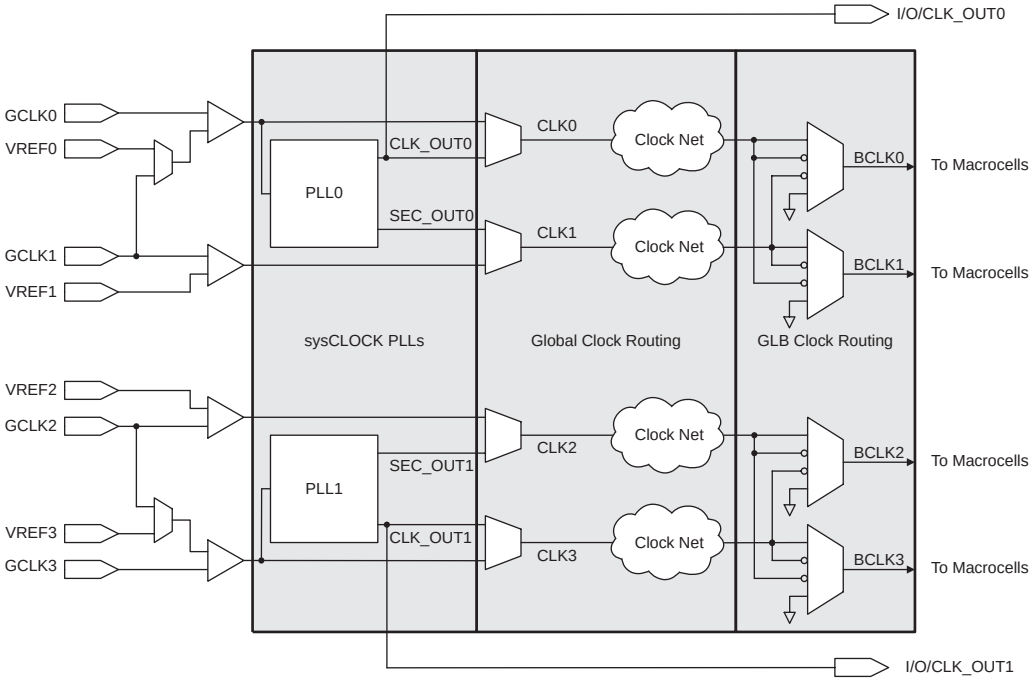
The final types of interfaces implemented are the differential standards LVDS and LVPECL. These interfaces are implemented on clock pins only. When using one of the differential standards, a pair of global clock pins (GCLK0 and GCLK1 or GCLK3 and GCLK2) is combined to create a single clock signal.

For more information on the sysIO capability, please refer to Technical Note TN1000: *ispMACH 5000VG sysIO Design and Usage Guidelines* .

GLB Clock Distribution

The ispMACH 5000VG family has four dedicated clock input pins: GCLK0-GCLK3. GLCK0 and GCLK3 can be routed through a PLL circuit or routed directly to the internal clock nets. The internal clock nets (CLK0-CLK3) are directly related to the dedicated clock pins (see Secondary Clock Divider exception when using the sysCLOCK circuit). These feed the GLB clock multiplexes which generate the GLB clock signals (BCLK0-BCLK3). The GLB clock multiplexer allows a variety of true and complementary versions of the clocks to be used within the GLB. Each block clock can be the true or inverse of its associated global clock or the inverse of the adjacent global clock. Figure 9 shows the clock distribution network.

Figure 9. Clock Distribution Network

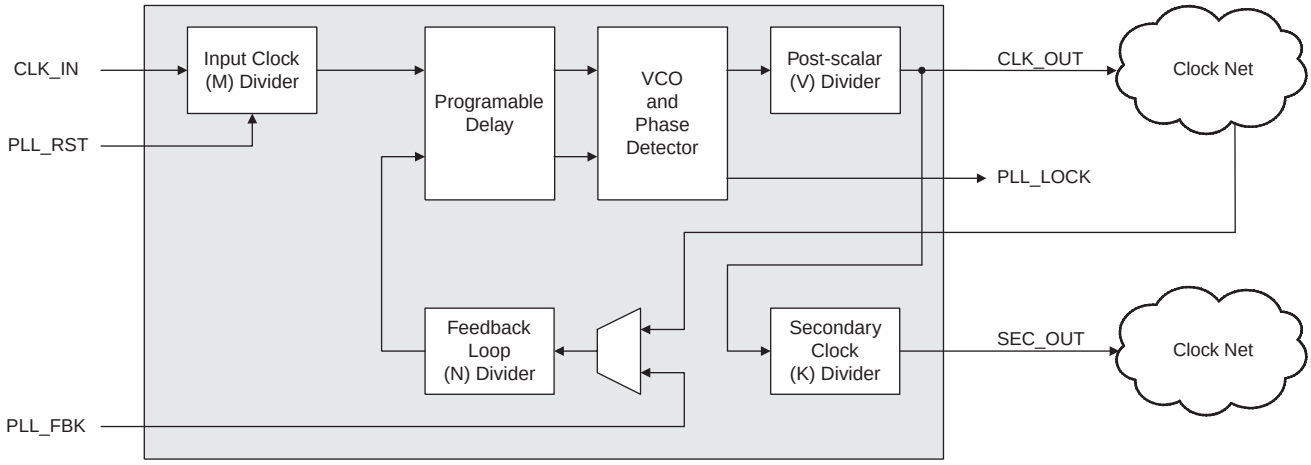


sysCLOCK PLL

The sysCLOCK PLL circuitry consists of Phase-Lock Loops (PLLs) and the various dividers, reset and feedback signals associated with the PLLs. This feature gives the user the ability to synthesize clock frequencies and generate multiple clock signals for routing within the device. Furthermore, it can generate clock signals that are deskewed either at the board level or the device level.

The ispMACH 5000VG devices provide two PLL circuits. PLL0 receives its clock inputs from GCLK 0 and provides outputs to CLK 0 (CLK 1 when using the secondary clock). PLL1 operates with signals from GCLK 3 and CLK 3 (CLK 2 when using the secondary clock). The PLL outputs (CLK_OUT) are routed via a dedicated net to a dedicated pad. Further the buffers at these dedicated pads are regular I/O buffers that can select either the I/O macrocell or the CLK_OUT (CLK_OUT0/CLK_OUT1) signal. The CLK_OUT nets are not routed through the GRP. Additionally, there are two sets of signals used for external control. Each PLL has a set of PLL_RST, PLL_FBK and PLL_LOCK signals. Figure 10 shows the ispMACH 5000VG PLL block diagram.

Figure 10. PLL Block Diagram



In order to facilitate the multiply and divide capabilities of the PLL, each PLL has dividers associated with it: M, N and K. The M divider is used to divide the clock signal, while the N divider is used to multiply the clock signal. The K divider is only used when a secondary clock output is needed. This divider divides the primary clock output and feeds to a separate global clock net. The V divider is used to provide lower frequency output clocks, while maintaining a stable, high frequency output from the PLL's VCO circuit.

The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. This operates by inserting delay on the input or feedback lines in 0.5ns increments from 0 to 3.5ns. For more information on the PLL, please refer to Technical Note TN1003: *ispMACH 5000VG PLL Usage Guidelines* .

Power Management

The ispMACH 5000VG devices provide unique power management controls. The devices have two power settings, high power and low power, on a per node basis. Low power consumption is approximately 50% of high power consumption with a timing delay adder (tLP) to the routing delay of the low power node. Each node can be configured as either high power or low power. However, care should be taken when sharing product terms between nodes with different power settings.

The ispMACH 5000VG devices also have a power-off feature for unused product terms. By default, any product term that is not used is configured as such. This allows the device to operate at minimal power consumption without affecting the timing of the design. For more information on power management, please refer to Technical Note TN1002: *Power Estimation in ispMACH 5000VG Devices*.

Absolute Maximum Ratings[1, 2, 3]

Supply Voltage (V_{CC}) . . . . . -0.5 to 5.4V

PLL Supply Voltage (V_{CCP}) . . . . . -0.5 to 5.4V

Output Supply Voltage (V_{CCO}) . . . . . -0.5 to 5.4V

Input Voltage Applied[4] . . . . . -0.5 to 5.6V

Tri-state Output Voltage Applied. . . . . -0.5 to 5.6V

Storage Temperature . . . . . -65 to 150°C

Junction Temperature (Tj) with Power Applied . . . . . -55 to 130°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Overshoot and Undershoot of -2V to (V_{IH} (MAX)+2) volts is permitted for a duration of < 20ns.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	3.0	3.6	V
V_{CCP}	Supply Voltage for PLL block	3.0	3.6	V
V_{CCJ}	Supply Voltage for IEEE1149.1 Test Access Port	1.65	3.6	V
Tj (Commercial)	Junction Commercial Operation	0	90	C
Tj (Industrial)	Junction Industrial Operation	-40	105	C

Note: V_{CCJ} must be set in appropriate range to be compatible with desired LVCMOS standard.

Erase Reprogram Specifications

Parameter	Min	Max	Units
Erase/Reprogram Cycle	1000	—	Cycles

Hot Socketing Characteristics[1,2,3]

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DK}	Input or I/O Leakage Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	+/-100	µA
		V_{IH} (MAX) $\le V_{IN} \le$ 5.5V	—	—	+/-100	µA

1. Insensitive to sequence of V_{CC} and V_{CCO}. However, assumes monotonic rise / fall rates for V_{CC} and V_{CCO}.
2. LVTTL, LVCMOS only
3. $0 < V_{CC} \le V_{CC}$ (MAX), $0 < V_{CCO} \le V_{CCO}$ (MAX)

ispMACH 5768VG External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description[1,2,3]	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Data propagation delay, 5-PT bypass	—	5.0	—	7.5	—	10.0	—	12.0	ns
t_{PD_PTSA}	Data propagation delay, intrasegment path	—	6.0	—	9.0	—	11.5	—	13.5	ns
t_{PD_GLOBAL}	Data propagation delay, intersegment path	—	6.5	—	9.75	—	13.0	—	16.0	ns
t_S	GLB register setup time before clock, 5-PT bypass	3.0	—	5.0	—	7.5	—	9.3	—	ns
t_{S_PTSA}	GLB register setup time before clock	3.0	—	6.0	—	8.5	—	10.0	—	ns
t_{SIR}	GLB register setup time before clock, input register path	2.8	—	3.0	—	4.0	—	5.0	—	ns
t_H	GLB register hold time before clock, 5-PT bypass	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{H_PTSA}	GLB register hold time before clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time before clock, input reg. path	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	4.4	—	5.0	—	6.0	—	7.0	ns
t_R	External reset pin to output delay	—	6.5	—	9.0	—	10.0	—	10.9	ns
t_{RW}	External reset pulse duration	4.0	—	6.0	—	8.0	—	9.5	—	ns
$t_{LPTOE/DIS}$	Input to output local product term output enable/disable	—	7.0	—	9.75	—	11.5	—	13.4	ns
$t_{SPTOE/DIS}$	Input to output segment product term output enable/disable	—	8.0	—	11.25	—	17.5	—	20.4	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	6.2	—	7.5	—	8.85	—	10.0	ns
t_{CW}	Global clock width, high or low	1.6	—	2.75	—	3.6	—	4.3	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{WIR}	Input register clock width, high or low	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{SKEW}	Clock-to-out skew, block level	—	0.25	—	0.35	—	0.45	—	0.55	ns
	Clock-to-out skew, segment level	—	0.4	—	0.5	—	0.6	—	0.7	ns
f_{MAX}[4]	Clock frequency with internal feedback	178.6	—	117.0	—	87.0	—	73.0	—	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, $1/ (t_{S\_PTSA} + t_{CO})$	135.1	—	90.9	—	69.0	—	58.8	—	MHz
f_{MAX} (Tog.)	Clock frequency max Toggle	312.5	—	181.0	—	138.0	—	116.0	—	MHz

Timing v.1.20

1. Timing numbers are based on default LVCMOS 3.3 I/O Buffers. Use timing adjusters provided to calculate timing for other standards.
2. Measured using standard switching circuit, assuming segment and global routing loading of 1, worst case PTSA loading and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using SRP feedback.

ispMACH 51024VG External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description[1,2,3]	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Data propagation delay, 5-PT bypass	—	5.0	—	7.5	—	10.0	—	12.0	ns
t_{PD_PTSA}	Data propagation delay, intrasegment path	—	6.0	—	9.0	—	11.5	—	13.5	ns
t_{PD_GLOBAL}	Data propagation delay, intersegment path	—	6.5	—	9.75	—	13.0	—	16.0	ns
t_S	GLB register setup time before clock, 5-PT bypass	3.0	—	5.0	—	7.5	—	9.3	—	ns
t_{S_PTSA}	GLB register setup time before clock	3.0	—	6.0	—	8.5	—	10.0	—	ns
t_{SIR}	GLB register setup time before clock, input register path	2.8	—	3.0	—	4.0	—	5.0	—	ns
t_H	GLB register hold time before clock, 5-PT bypass	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{H_PTSA}	GLB register hold time before clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time before clock, input reg. path	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	4.4	—	5.0	—	6.0	—	7.0	ns
t_R	External reset pin to output delay	—	6.5	—	9.0	—	10.0	—	10.9	ns
t_{RW}	External reset pulse duration	4.0	—	6.0	—	8.0	—	9.5	—	ns
$t_{LPTOE/DIS}$	Input to output local product term output enable/disable	—	7.0	—	9.75	—	11.5	—	13.4	ns
$t_{SPTOE/DIS}$	Input to output segment product term output enable/disable	—	8.0	—	11.25	—	17.5	—	20.4	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	6.2	—	7.5	—	8.85	—	10.0	ns
t_{CW}	Global clock width, high or low	1.6	—	2.75	—	3.6	—	4.3	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{WIR}	Input register clock width, high or low	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{SKEW}	Clock-to-out skew, block level	—	0.25	—	0.35	—	0.45	—	0.55	ns
	Clock-to-out skew, segment level	—	0.4	—	0.5	—	0.6	—	0.7	ns
f_{MAX}[4]	Clock frequency with internal feedback	178.6	—	117.0	—	87.0	—	73.0	—	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, $1/ (t_{S\_PTSA} + t_{CO})$	135.1	—	90.9	—	69.0	—	58.8	—	MHz
f_{MAX} (Tog.)	Clock frequency max Toggle	312.5	—	181.0	—	138.0	—	116.0	—	MHz

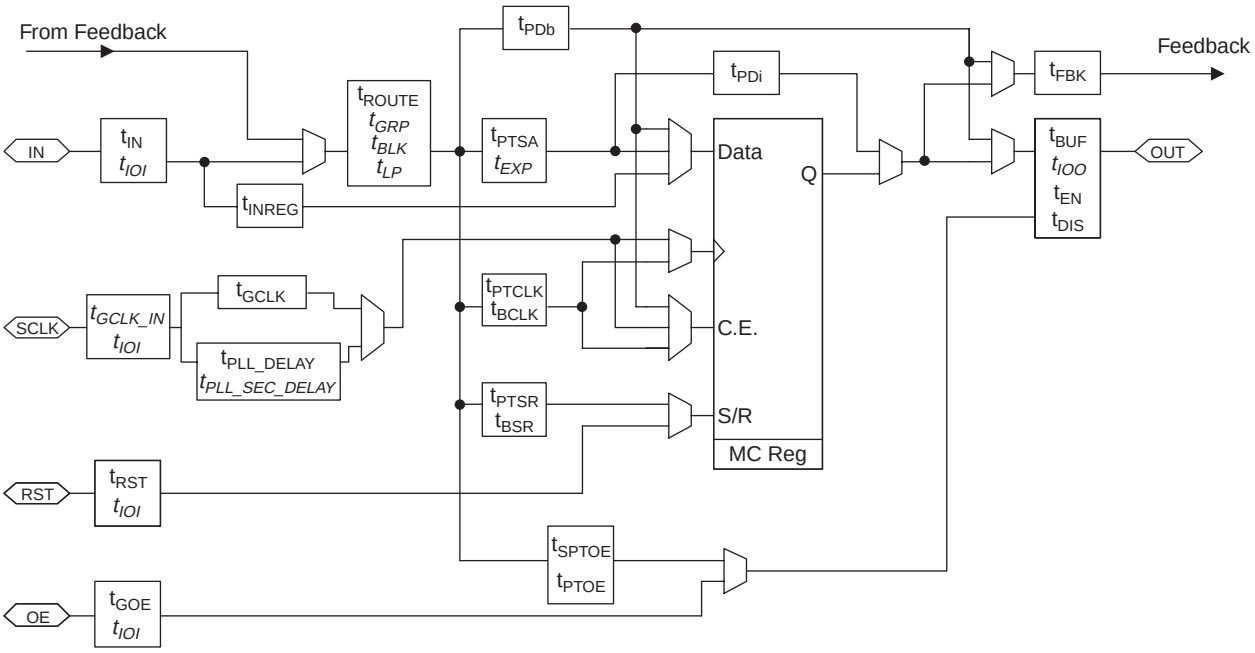
Timing v.1.10

1. Timing numbers are based on default LVCMOS 3.3 I/O Buffers. Use timing adjusters provided to calculate timing for other standards.
2. Measured using standard switching circuit, assuming segment and global routing loading of 1, worst case PTSA loading and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using SRP feedback.

Timing Model

The task of determining the timing through the ispMACH 5000VG family, like any CPLD, is relatively simple. The timing model provided in Figure 11 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, please refer to Technical Note TN1001: *ispMACH 5000VG Timing Model Design and Usage Guidelines.*

Figure 11. ispMACH 5000VG Timing Model



Italicized items are optional delay adders

ispMACH 5768VG Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
In/Out Delays										
t_{IN}	Input Buffer Delay	—	0.65	—	0.95	—	1.25	—	1.40	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	0.65	—	0.95	—	1.25	—	1.40	ns
t_{GOE}	Global OE Pin Delay	—	4.05	—	5.00	—	6.00	—	7.00	ns
t_{BUF}	Delay through Output Buffer	—	1.15	—	1.50	—	1.75	—	1.90	ns
t_{EN}	Output Enable Time	—	2.15	—	2.50	—	2.85	—	3.00	ns
t_{DIS}	Output Disable Time	—	2.15	—	2.50	—	2.85	—	3.00	ns
t_{RSTb}	Global RESETbar Pin Delay	—	4.60	—	6.50	—	7.00	—	7.50	ns
Routing Delays										
t_{ROUTE}	Delay through SRP	—	2.80	—	4.20	—	5.65	—	6.90	ns
t_{PTSA}	Product Term Sharing Array Delay	—	0.40	—	1.85	—	2.35	—	2.50	ns
t_{PDB}	5-PT Bypass Propagation Delay	—	0.40	—	0.85	—	1.35	—	1.80	ns
t_{PDi}	Macrocell Propagation Delay	—	1.00	—	0.50	—	0.50	—	0.80	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	3.00	—	3.05	—	3.50	—	4.40	ns
t_{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t_{GCLK}	Global Clock Tree Delay	—	0.85	—	0.70	—	0.55	—	0.65	ns
t_{PLL_DELAY}	Programmable PLL Delay Increment	—	0.50	—	0.50	—	0.50	—	0.50	ns
$t_{PLL\_SEC\_DELAY}$	Additional Delay When Using Secondary PLL Output	—	0.60	—	0.60	—	0.60	—	0.60	ns
t_{GRP}	Global Routing Pool Delay	—	1.50	—	2.25	—	3.00	—	4.00	ns
Register/Latch Delays										
t_{S}	D-Register Setup Time	0.65	—	0.65	—	1.05	—	1.25	—	ns
t_{S_PT}	D-Register Setup Time with PT Clock	0.65	—	0.65	—	1.05	—	1.25	—	ns
t_{H}	D-Register Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{ST}	T-Register Setup Time	1.15	—	1.15	—	1.55	—	1.75	—	ns
t_{ST_PT}	T-Register Setup Time with PT Clock	1.15	—	1.15	—	1.55	—	1.75	—	ns
t_{HT}	T-Register Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	1.75	—	1.85	—	2.45	—	3.05	ns
t_{CES}	Clock Enable Setup Time	2.60	—	3.90	—	5.05	—	5.95	—	ns
t_{CEH}	Clock Enable Hold Time	0.60	—	0.90	—	1.20	—	1.45	—	ns
t_{SL}	Latch Setup Time	2.80	—	4.20	—	5.50	—	6.60	—	ns
t_{SL_PT}	Latch Setup Time with PT Clock	2.80	—	4.20	—	5.50	—	6.60	—	ns
t_{HL}	Latch Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	1.75	—	2.50	—	3.50	—	4.50	ns
t_{PDLi}	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	2.40	—	3.50	—	4.00	—	4.50	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.75	—	1.00	—	1.25	—	1.50	ns
t_{SRR}	Asynchronous Reset or Set Recovery Delay	—	1.00	—	1.50	—	2.00	—	2.50	ns
Control Delays										
t_{BCLK}	GLB PT Clock Delay	—	3.10	—	4.65	—	6.00	—	7.00	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	3.00	—	4.50	—	6.00	—	7.00	ns

sysCLOCK PLL Timing

Over Recommended Operating Conditions[1]

Symbol	Parameter	Conditions	Min	Max	Units
t_R,t_F	Input clock, rise and fall time	20% to 80%	—	3.0	ns
t_{INSTB}	Input clock stability, period jitter (peak)[1]	—	—	+/- 200	ps
t_{PWH}	Input clock, high time	—	1.6	—	ns
t_{PWL}	Input clock, low time	—	1.6	—	ns
f_{MDIVIN}	M Divider input, frequency range	—	5	180	MHz
$f_{MDIVOUT}$	M Divider output, frequency range	—	5	180	MHz
f_{VDIVIN}	V Divider input, frequency range	—	60	200	MHz
$f_{VDIVOUT}$	V Divider output, frequency range	—	5	180	MHz
$t_{OUTDUTY}$	Output clock, duty cycle	—	40	60	%
$t_{JIT(CC)}$	Output clock, cycle to cycle jitter (peak)	Clean Reference, 5MHz ≤ $f_{MDIVOUT}$ < 80MHz	—	+/- 200	ps
		Clean Reference, 80MHz ≤ $f_{MDIVOUT}$ ≤ 180MHz	—	+/- 100	ps
$t_{JIT(\phi)}$	Output clock, accumulated phase jitter (peak)[2]	Clean Reference, 5MHz ≤ $f_{MDIVOUT}$ < 80MHz	—	+/- 200	ps
		Clean Reference, 80MHz ≤ $f_{MDIVOUT}$ ≤ 180MHz	—	+/- 100	ps
$t_{CLK\_OUT\_DLY}$	Input clock to CLK_OUT delay	Internal feedback	—	1	ns
t_ϕ	Input clock to external feedback delta	External feedback	—	500	ps
t_{LOCK}	Time to acquire phase lock after input stable	—	—	30	µs
t_{PLL_DELAY}	Delay increment	—	+/- 0.35	+/- 0.65	ns
t_{RANGE}	Total output delay range	—	+/- 2.45	+/- 4.55	ns
t_{PLL_RSTR}	Reset recovery time of the M-divider	—	11.0	—	ns
t_{PLL_RSTW}	Minimum reset pulse width	—	6.0	—	ns

1. This condition assures that the output phase jitter ($t_{JIT(\phi)}$) will remain within specification.
2. Accumulated jitter measured over 10,000 waveform samples.

Boundary Scan Timing Specifications

Symbol	Parameter	Min.	Max.	Units
t_{BTCP}	TCK [BSCAN test] clock cycle	40	—	ns
t_{BTCH}	TCK [BSCAN test] pulse width high	20	—	ns
t_{BTCL}	TCK [BSCAN test] pulse width low	20	—	ns
t_{BTSU}	TCK [BSCAN test] setup time	8	—	ns
t_{BTH}	TCK [BSCAN test] hold time	10	—	ns
t_{BRF}	TCK [BSCAN test] rise and fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
t_{BTOZ}	TAP controller falling edge of clock to data output disable	—	10	ns
t_{BTVO}	TAP controller falling edge of clock to data output enable	—	10	ns
$t_{BVTCPSU}$	BSCAN test Capture register setup time	8	—	ns
t_{BTCPH}	BSCAN test Capture register hold time	10	—	ns
t_{BTUCO}	BSCAN test Update reg, falling edge of clock to valid output	—	25	ns
t_{BTUOZ}	BSCAN test Update reg, falling edge of clock to output disable	—	25	ns
t_{BTUOV}	BSCAN test Update reg, falling edge of clock to output enable	—	25	ns

ispMACH 51024 Power Supply and NC Connections[1]

Signal	484-Ball fpBGA[2]	676-Ball fpBGA[2]
V_{CC}	B17, B2, B21, B6, C14, C9, E18, E5, F2, F21, J20, J3, P20, P3, U2, U21, Y14, Y9, AA17, AA2, AA21, AA6	B29, D6, D10, D12, D19, D21, D25, F4, F27, K4, K27, M4, M27, W4, W27, AA4, AA27, AE4, AE27, AG6, AG10, AG12, AG19, AG21,AG25, AJ2
V_{CCO0}	B5, D7, E2, E6, E9, F5, G4, J5	E5, E7, E9, E11, F10, G5, J5, K6, L5
V_{CCO1}	P5, U5, V6, V9, Y3	Y5, AA6, AB5, AD5, AE10, AF5, AF7, AF9, AF11
V_{CCO2}	P18, U18, V14, V17, Y20	Y26, AA25, AB26, AD26, AE21, AF20, AF22, AF24, AF26
V_{CCO3}	B18, D16, E14, E17, E21, F18, G19, J18	E20, E22, E24, E26, F21, G26, J26, K25, L26
V_{CCP0}	L7	P5
V_{CCP1}	N18	N26
V_{CCJ}	P4	U6
V_{REF0}	A9	C11
V_{REF1}	AA10	AK10
V_{REF2}	AA13	AJ21
V_{REF3}	A15	E19
GND PLL 0	L6	R6
GND PLL 1	L16	P25
GND	A1, A22, C3, C20, D4, D19, E7, E16, G5, G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, G18, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, K7, K8, K9, K10, K11, K12, K13, K14, K15, K16, L8, L9, L10, L11, L12, L13, L14, L15, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, N7, N8, N9, N10, N11, N12, N13, N14, N15, N16, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, T4, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T19, W7, W16, AB1, AB22	A1, A30, B2,C3, C28, D8, D23, F7, F9, F11, F12, F19, F20, F22, F24, G6, G25, H4, H27, J6, J25, L6, L11, L12, L13, L14, L15, L16, L17, L18, L19, L20, L25, M6, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20, M25, N11, N12, N13, N14, N15, N16, N17, N18, N19, N20, P11, P12, P13, P14, P15, P16, P17, P18, P19, P20, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, T11, T12, T13, T14, T15, T16, T17, T18, T19, T20, U11, U12, U13, U14,U15, U16, U17, U18, U19, U20, V11, V12, V13, V14, V15, V16, V17, V18, V19, V20, W6, W11, W12, W13, W14, W15, W16, W17, W18, W19, W20, W25, Y6, Y11, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y20, Y25, AB6, AB25, AC4, AC27, AD6, AD25, AE7, AE9, AE11, AE12, AE19, AE20, AE22, AE24, AG8, AG23, AH3, AH28, AK1, AK30
NC[3]	AA1	A14, A15, A16, A17, B14, B15, B16, B17, C13, C14, C15, C16, C17, C18, D13, D14, D15, D16, D17, D18, E13, E14, E15, E16, E17, E18, F13, F14, F15, F16, F17, F18, AE13, AE14, AE15, AE16, AE17, AE18, AF13, AF14, AF15, AF16, AF17, AF18, AG13, AG14, AG15, AG16, AG17, AG18, AH14, AH15, AH16, AH17, AH18, AJ14, AJ15, AJ16, AJ17, AJ18, AK14, AK15, AK16, AK17

1. All grounds must be electrically connected at the board level.
2. Not all grounds internally connected within the device.
3. NC pins are not to be connected to any active signals, VCC or GND.

ispMACH 5768VG Logic Signal Connections

Bank No.	Signal	256 fpBGA	484 fpBGA
0	0C-30	C8	D11
0	0C-28	B6	B11
0	0C-26	A5	E12
0	0C-24	D8	C11
0	0C-22	E8	F12
0	0C-20	B5	B10
0	GNDIO0	GND	GND
0	0C-18	A4	A10
0	0C-16	D7	D10
0	0C-14/VREF0	E7	A9
0	0C-12	C6	E11
0	0C-10	B4	B9
0	0C-8	A3	F11
0	0C-6	NC	A8
0	0C-4	NC	C10
0	0C-2	NC	A7
0	0C-0	NC	E10
0	0D-30	NC	B8
0	0D-28	NC	C8
0	GNDIO0	GND	GND
0	0D-26	NC	F10
0	0D-24	NC	A6
0	0D-22	NC	F9
0	0D-20	NC	C7
0	0D-18	NC	D9
0	0D-16	NC	B7
0	0D-14	D6	E8
0	0D-12	E6	A5
0	0D-10	A2	F8
0	0D-8	B3	C6
0	0D-6	C4	D8
0	0D-4	D5	A3
0	GNDIO0	GND	GND
0	0D-2	NC	A2
0	0D-0	NC	A4
0	0A-0	NC	F7
0	0A-2	NC	C5
0	0A-4	NC	F6
0	0A-6	NC	B3
0	0A-8	NC	NC
0	0A-10	NC	NC
0	GNDIO0	GND	GND
0	0A-12	NC	NC

Bank No.	Signal	256 fpBGA	484 fpBGA
0	0A-14	NC	NC
0	0A-16	NC	B4
0	0A-18	NC	D5
0	0A-20	NC	B1
0	0A-22	NC	D6
0	0A-24	NC	C4
0	0A-26	NC	E4
0	GNDIO0	GND	GND
0	0A-28	B2	C2
0	0A-30	B1	C1
0	0B-30	C2	D1
0	0B-28	C1	D2
0	0B-26	NC	D3
0	0B-24	NC	E1
0	0B-22	NC	E3
0	0B-20	NC	F4
0	0B-18	NC	F1
0	0B-16	NC	F3
0	0B-14	NC	G6
0	0B-12	NC	G1
0	GNDIO0	GND	GND
0	0B-10	NC	G2
0	0B-8	NC	H1
0	0B-6	NC	G3
0	0B-4	NC	H2
0	0B-2	NC	H5
0	0B-0	NC	H6
0	1A-0	F7	J1
0	1A-2	F6	K1
0	1A-4	E5	H3
0	1A-6	D4	J2
0	1A-8	D3	H4
0	1A-10	D2	K2
0	GNDIO0	GND	GND
0	1A-12	D1	J6
0	1A-14	E4	L1
0	1A-16	NC	K3
0	1A-18	NC	J4
0	1A-20	NC	L2
0	1A-22	NC	M1
0	1A-24	NC	K6
0	1A-26	NC	K4
0	1A-28	NC	L3

ispMACH 5768VG Logic Signal Connections (Continued)

Bank No.	Signal	256 fpBGA	484 fpBGA
3	4B-24	G11	M19
3	4B-26	F11	M21
3	4B-28	F10	L19
3	4B-30/CLK_OUT1	B11	L20
3	GNDIO3	GND	GND
3	4A-30	NC	M17
3	4A-28	NC	M22
3	4A-26	NC	K20
3	4A-24	NC	L18
3	4A-22	NC	L21
3	4A-20	NC	K19
3	4A-18	NC	L22
3	4A-16	NC	K17
3	4A-14	E13	K22
3	4A-12	B12	L17
3	GNDIO3	GND	GND
3	4A-10	E15	K21
3	4A-8	D15	K18
3	4A-6	NC	J17
3	4A-4	NC	J19
3	4A-2	D16	J22
3	4A-0	E12	J21
3	5B-0	NC	H19
3	5B-2	NC	H20
3	5B-4	NC	H17
3	5B-6	NC	H18
3	5B-8	NC	H22
3	5B-10	NC	H21
3	GNDIO3	GND	GND
3	5B-12	NC	G20
3	5B-14	NC	G22
3	5B-16	NC	G17
3	5B-18	NC	G21
3	5B-20	NC	F19
3	5B-22	NC	F20
3	5B-24	A16	F22
3	5B-26	B15	E22
3	5B-28	A15	E19
3	5B-30	D13	E20
3	5A-30	B14	D22
3	5A-28	B16	D21
3	GNDIO3	GND	GND
3	5A-26	C16	D20

Bank No.	Signal	256 fpBGA	484 fpBGA
3	5A-24	C15	C22
3	5A-22	D14	C18
3	5A-20	A14	C19
3	5A-18	C13	D17
3	5A-16	B13	C21
3	5A-14	NC	NC
3	5A-12	NC	NC
3	GNDIO3	GND	GND
3	5A-10	NC	NC
3	5A-8	NC	NC
3	5A-6	NC	B22
3	5A-4	NC	D18
3	5A-2	NC	B20
3	5A-0	NC	F17
3	5D-0	NC	B19
3	5D-2	NC	C17
3	GNDIO3	GND	GND
3	5D-4	NC	A21
3	5D-6	NC	D15
3	5D-8	NC	A20
3	5D-10	NC	C16
3	5D-12	NC	A19
3	5D-14	NC	F16
3	5D-16	NC	B16
3	5D-18	NC	D14
3	5D-20	NC	A18
3	5D-22	A13	F15
3	5D-24	A12	A17
3	5D-26	A11	B15
3	GNDIO3	GND	GND
3	5D-28	A10	A16
3	5D-30	C11	F14
3	5C-0	A9	C15
3	5C-2	D12	D13
3	5C-4	D11	E15
3	5C-6	B10	F13
3	5C-8	B9	B14
3	5C-10	E11	E13
3	5C-12/VREF3	A8	A15
3	5C-14	D10	D12
3	5C-16	E10	A14
3	5C-18	A7	B13
3	GNDIO3	GND	GND

ispMACH 51024VG Logic Signal Connections

Bank No.	Signal	484 fpBGA	676 fpBGA
0	0C-30	D11	A13
0	0C-28	B11	B13
0	0C-26	E12	A12
0	0C-24	C11	B12
0	0C-22	F12	C12
0	0C-20	B10	A11
0	GNDIO0	GND	GND
0	0C-18	A10	B11
0	0C-16	D10	A10
0	0C-14/VREF0	A9	C11
0	0C-12	E11	E12
0	0C-10	B9	B10
0	0C-8	F11	D11
0	0C-6	A8	A9
0	0C-4	C10	C10
0	0C-2	A7	B9
0	0C-0	E10	A8
0	0D-30	B8	C9
0	0D-28	C8	B8
0	GNDIO0	GND	GND
0	0D-26	F10	E10
0	0D-24	A6	A7
0	0D-22	F9	D9
0	0D-20	C7	C8
0	0D-18	D9	B7
0	0D-16	B7	A6
0	0D-14	E8	C7
0	0D-12	A5	B6
0	0D-10	F8	A5
0	0D-8	C6	C6
0	0D-6	D8	D7
0	0D-4	A3	E8
0	GNDIO0	GND	GND
0	0D-2	A2	B5
0	0D-0	A4	A4
0	0A-0	F7	A3
0	0A-2	C5	B4
0	0A-4	F6	C5
0	0A-6	B3	F8
0	0A-8	NC	A2
0	0A-10	NC	B3
0	GNDIO0	GND	GND
0	0A-12	NC	C4

Bank No.	Signal	484 fpBGA	676 fpBGA
0	0A-14	NC	D5
0	0A-16	B4	E6
0	0A-18	D5	D4
0	0A-20	B1	B1
0	0A-22	D6	C2
0	0A-24	C4	F6
0	0A-26	E4	D3
0	GNDIO0	GND	GND
0	0A-28	C2	E4
0	0A-30	C1	F5
0	0B-30	D1	C1
0	0B-28	D2	D2
0	0B-26	D3	E3
0	0B-24	E1	D1
0	0B-22	E3	E2
0	0B-20	F4	H6
0	0B-18	F1	F3
0	0B-16	F3	E1
0	0B-14	G6	G4
0	0B-12	G1	F2
0	GNDIO0	GND	GND
0	0B-10	G2	H5
0	0B-8	H1	G3
0	0B-6	G3	F1
0	0B-4	H2	G2
0	0B-2	H5	H3
0	0B-0	H6	G1
0	1A-0	J1	H2
0	1A-2	K1	J4
0	1A-4	H3	H1
0	1A-6	J2	J3
0	1A-8	H4	K5
0	1A-10	K2	J2
0	GNDIO0	GND	GND
0	1A-12	J6	J1
0	1A-14	L1	K3
0	1A-16	K3	K2
0	1A-18	J4	K1
0	1A-20	L2	L4
0	1A-22	M1	L3
0	1A-24	K6	L2
0	1A-26	K4	M5
0	1A-28	L3	L1

ispMACH 51024VG Logic Signal Connections (Continued)

Bank No.	Signal	484 fpBGA	676 fpBGA
0	1A-30	K5	M3
0	GNDIO0	GND	GND
0	1B-30/CLK_OUT0	N1	M2
0	1B-28	M2	M1
0	1B-26	P1	N6
0	1B-24	L4	N5
0	1B-22	N2	N4
0	1B-20	M3	N3
0	1B-18	L5	N2
0	1B-16	R1	N1
0	1B-14	P2	P6
0	1B-12	N3	P4
0	GNDIO0	GND	GND
0	1B-10	M6	P3
0	1B-8	M5	P2
0	1B-6/PLL_RST0	M4	P1
0	1B-4/PLL_FBK0	N4	R4
0	1B-2	N6	R3
0	1B-0	N5	R2
1	2B-0	NC	R1
1	2B-2	NC	T1
1	2B-4	NC	T3
1	2B-6	NC	T2
1	2B-8	NC	U1
1	2B-10	NC	U2
1	GNDIO1	GND	GND
1	2B-12	NC	U3
1	2B-14	NC	U4
1	2B-16	NC	V1
1	2B-18	NC	V2
1	2B-20	NC	V3
1	2B-22	NC	V4
1	2B-24	NC	W1
1	2B-26	NC	V6
1	2B-28	NC	W2
1	2B-30	NC	W3
1	GNDIO1	GND	GND
1	2A-30	NC	Y1
1	2A-28	NC	W5
1	2A-26	NC	Y2
1	2A-24	NC	Y3
1	2A-22	NC	AA1
1	2A-20	NC	Y4

Bank No.	Signal	484 fpBGA	676 fpBGA
1	2A-18	NC	AA2
1	2A-16	NC	AA3
1	2A-14	NC	AB1
1	2A-12	NC	AB2
1	GNDIO1	GND	GND
1	2A-10	NC	AA5
1	2A-8	NC	AB3
1	2A-6	NC	AC1
1	2A-4	NC	AB4
1	2A-2	NC	AC2
1	2A-0	NC	AD1
1	3B-0	R5	AC3
1	3B-2	T2	AD2
1	3B-4	T5	AE1
1	3B-6	T3	AD3
1	3B-8	U1	AE2
1	3B-10	U4	AC5
1	GNDIO1	GND	GND
1	3B-12	V1	AF1
1	3B-14	U3	AD4
1	3B-16	V5	AE3
1	3B-18	V2	AC6
1	3B-20	W1	AF2
1	3B-22	V3	AG1
1	3B-24	W2	AF3
1	3B-26	Y1	AG2
1	3B-28	Y2	AH1
1	3B-30	W3	AE5
1	3A-30	AA3	AF4
1	3A-28	W4	AG3
1	GNDIO1	GND	GND
1	3A-26	W5	AE6
1	3A-24	Y4	AH2
1	3A-22	T6	AJ1
1	3A-20	Y5	AG4
1	3A-18	U6	AF6
1	3A-16	AA4	AG5
1	3A-14	NC	AH4
1	3A-12	NC	AJ3
1	GNDIO1	GND	GND
1	3A-10	NC	AK2
1	3A-8	NC	AE8
1	3A-6	W6	AH5

ispMACH 51024VG Logic Signal Connections (Continued)

Bank No.	Signal	484 fpBGA	676 fpBGA
—	TMS	T1	T4
—	TOE	T18	U26

Signal Configuration

ispMACH 5768VG and 51024VG 484-ball fpBGA

	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O / VREF3	I/O	I/O	I/O	I/O	I/O	I/O/ VREF0	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	**A**
B	I/O	VCC	I/O	I/O	VCCO3	VCC	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCC	VCCO0	I/O	I/O	VCC	I/O	**B**
C	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O	I/O	GND	I/O	I/O	**C**
D	I/O	I/O	I/O	GND	I/O	I/O	VCCO3	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCCO0	I/O	I/O	GND	I/O	I/O	I/O	**D**
E	I/O	VCCO3	I/O	I/O	VCC	VCCO3	GND	I/O	VCCO3	I/O	I/O	I/O	I/O	VCCO0	I/O	GND	VCCO0	VCC	I/O	I/O	VCCO0	I/O	**E**
F	I/O	VCC	I/O	I/O	VCCO3	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCCO0	I/O	I/O	VCC	I/O	**F**
G	I/O	I/O	I/O	VCCO3	GND	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	GND	VCCO0	I/O	I/O	I/O	**G**
H	I/O	I/O	I/O	I/O	I/O	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	I/O	I/O	I/O	I/O	I/O	**H**
J	I/O	I/O	VCC	I/O	VCCO3	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	VCCO0	I/O	VCC	I/O	I/O	**J**
K	I/O	I/O	I/O	I/O	I/O	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	I/O	I/O	I/O	I/O	I/O	**K**
L	I/O	I/O	I/O/ CLK_OUT1	I/O	I/O	I/O	GNDP1	GND	GND	GND	GND	GND	GND	GND	GND	VCCP0	GNDP0	I/O	I/O	I/O	I/O	I/O	**L**
M	I/O	I/O	I/O	I/O	I/O	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	I/O	I/O/ PLL_RST0	I/O	I/O	I/O	**M**
N	I/O	I/O	I/O/ PLL_RST1	I/O	VCCP1	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	I/O	I/O/ PLL_FBK0	I/O	I/O	I/O/ CLK_OUT0	**N**
P	I/O	I/O/ PLL_FBK1	VCC	GCLK3	VCCO2	GCLK2	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GCLK0	VCCO1	VCCJ	VCC	I/O	I/O	**P**
R	I/O	I/O	I/O	RESETB	GOE0	GOE1	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GCLK1	I/O	TDO	TCK	TDI	I/O	**R**
T	I/O	I/O	I/O	GND	TOE	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	I/O	GND	I/O	I/O	TMS	**T**
U	I/O	VCC	I/O	I/O	VCCO2	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCCO1	I/O	I/O	VCC	I/O	**U**
V	I/O	I/O	I/O	I/O	I/O	VCCO2	I/O	I/O	VCCO2	I/O	I/O	I/O	I/O	VCCO1	I/O	I/O	VCCO1	I/O	I/O	I/O	I/O	I/O	**V**
W	I/O	I/O	I/O	I/O	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	**W**
Y	I/O	I/O	VCCO2	I/O	I/O	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O	I/O	VCCO1	I/O	I/O	**Y**
AA	I/O	VCC	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O/ VREF2	I/O	I/O	I/O/ VREF1	I/O	I/O	I/O	VCC	I/O	I/O	I/O	VCC	NC[1]	**AA**
AB	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	**AB**
	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

ispMACH 5768VG and 51024VG 484BGA/51024VG

Bottom View

1. NCs are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.

Signal Configuration

ispMACH 51024VG 676-ball fpBGA

	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC[1]	NC[1]	NC[1]	NC[1]	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	A
B	I/O	VCC	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC[1]	NC[1]	NC[1]	NC[1]	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	I/O	B
C	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	I/O	I/O/ VREF0	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	I/O	I/O	C
D	I/O	I/O	I/O	I/O	I/O	VCC	I/O	GND	I/O	VCC	I/O	VCC	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	VCC	I/O	VCC	I/O	GND	I/O	VCC	I/O	I/O	I/O	I/O	I/O	D
E	I/O	I/O	I/O	I/O	VCCO3	I/O	VCCO3	I/O	VCCO3	I/O	VCCO3	I/O/ VREF3	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	I/O	VCCO0	I/O	VCCO0	I/O	VCCO0	I/O	VCCO0	I/O	I/O	I/O	I/O	E
F	I/O	I/O	I/O	VCC	I/O	I/O	GND	I/O	GND	VCCO3	GND	GND	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	GND	GND	VCCO0	GND	I/O	GND	I/O	I/O	VCC	I/O	I/O	I/O	F
G	I/O	I/O	I/O	I/O	VCCO3	GND																			GND	VCCO0	I/O	I/O	I/O	I/O	G
H	I/O	I/O	I/O	GND	I/O	I/O																			I/O	I/O	GND	I/O	I/O	I/O	H
J	I/O	I/O	I/O	I/O	VCCO3	GND																			GND	VCCO0	I/O	I/O	I/O	I/O	J
K	I/O	I/O	I/O	VCC	I/O	VCCO3																			VCCO0	I/O	VCC	I/O	I/O	I/O	K
L	I/O	I/O	I/O	I/O	VCCO3	GND					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					GND	VCCO0	I/O	I/O	I/O	I/O	L
M	I/O	I/O/ CLK_OUT1	I/O	VCC	I/O	GND					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					GND	I/O	VCC	I/O	I/O/ CLK_OUT0	I/O	M
N	I/O	I/O	I/O	I/O	VCCP1	I/O					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					I/O	I/O	I/O	I/O	I/O	I/O	N
P	I/O	I/O	I/O	I/O	GCLK3	GNDP1					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					I/O	VCCP0	I/O	I/O	I/O	I/O/ PLL_RST0	P
R	I/O	I/O	I/O/ PLL_RST1	I/O/ PLL_FBK1	GOE1	GCLK2					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					GNDP0	GCLK0	I/O/ PLL_FBK0	I/O	I/O	I/O	R
T	I/O	I/O	I/O	I/O	GOE0	RESETB					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					GCLK1	TDI	TMS	I/O	I/O	I/O	T
U	I/O	I/O	I/O	I/O	TOE	I/O					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					VCCJ	TCK	I/O	I/O	I/O	I/O	U
V	I/O	I/O	I/O	I/O	I/O	I/O					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					I/O	TDO	I/O	I/O	I/O	I/O	V
W	I/O	I/O	I/O	VCC	I/O	GND					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					GND	I/O	VCC	I/O	I/O	I/O	W
Y	I/O	I/O	I/O	I/O	VCCO2	GND					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					GND	VCCO1	I/O	I/O	I/O	I/O	Y
AA	I/O	I/O	I/O	VCC	I/O	VCCO2																			VCCO1	I/O	VCC	I/O	I/O	I/O	AA
AB	I/O	I/O	I/O	I/O	VCCO2	GND																			GND	VCCO1	I/O	I/O	I/O	I/O	AB
AC	I/O	I/O	I/O	GND	I/O	I/O																			I/O	I/O	GND	I/O	I/O	I/O	AC
AD	I/O	I/O	I/O	I/O	VCCO2	GND																			GND	VCCO1	I/O	I/O	I/O	I/O	AD
AE	I/O	I/O	I/O	VCC	I/O	I/O	GND	I/O	GND	VCCO2	GND	GND	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	GND	GND	VCCO1	GND	I/O	GND	I/O	I/O	VCC	I/O	I/O	I/O	AE
AF	I/O	I/O	I/O	I/O	VCCO2	I/O	VCCO2	I/O	VCCO2	I/O	VCCO2	I/O	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	I/O	VCCO1	I/O	VCCO1	I/O	VCCO1	I/O	VCCO1	I/O	I/O	I/O	I/O	AF
AG	I/O	I/O	I/O	I/O	I/O	VCC	I/O	GND	I/O	VCC	I/O	VCC	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	VCC	I/O	VCC	I/O	GND	I/O	VCC	I/O	I/O	I/O	I/O	I/O	AG
AH	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	I/O	I/O	AH
AJ	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O/ VREF2	I/O	I/O	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCC	I/O	AJ
AK	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC[1]	NC[1]	NC[1]	NC[1]	I/O	I/O	I/O	I/O/ VREF1	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	AK
	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

ispMACH 51024VG

Bottom View

676BGA/51024VG

1. NCs are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.